RIGHT IOs for this signals to Gate & Source EPD

Gate: Selects ROW to write pixels

EP_MODE
EP_STV
CKV

Source: Gives signal to FETs in row to apply +15 or −15 to pixels

EP_OE
XCL
LEH
XSTL

SIGNALS according to:
http://essentialscrap.com/eink/waveforms.html

U1
Pico

Raspberry Pi Pico

TPS_WAKEUP	1	GPIO0	VBUS	40	5V
TPS_nINT	2	GPIO1	VSYS	39	
	3	GND	GND	38	GND
TPS_VCOM_CTRL	4	GPIO2	3V3_EN	37	R1 5K 5V
TPS_PWRUP	5	GPIO3	3V3	36	3.3V
SDA	6	GPIO4	ADC_VREF	35	
SCL	7	GPIO5	GPIO28_ADC2	34	
	8	GND	AGND	33	
TPS_PWR_GOOD	9	GPIO6	GPIO27_ADC1	32	
EP_MODE	10	GPIO7	GPIO26_ADC0	31	
EP_STV	11	GPIO8	RUN	30	
CKV	12	GPIO9	GPIO22	29	LEH
	13	GND	GND	28	
EP_OE	14	GPIO10	GPIO21	27	XSTL
XCL	15	GPIO11	GPIO20	26	
D0	16	GPIO12	GPIO19	25	D7
D1	17	GPIO13	GPIO18	24	D6
	18	GND	GND	23	
D2	19	GPIO14	GPIO17	22	D5
D3	20	GPIO15	GPIO16	21	D4

SWCLK 41, GND 42, SWDIO 43

RIGHT IOs for this signals from P-Mic

TPS_WAKEUP	OUT Wake up pin. Pull this pin high to wake up from sleep mode.
TPS_nINT	INPUT Open drain interrupt pin (active low)
TPS_VCOM_CTRL	OUT VCOM enable. Pull this pin high to enable the VCOM amplifier.
TPS_PWRUP	OUT Power-up pin. Pull this pin high to power up all output rails.
TPS_PWR_GOOD	INPUT Open-drain power good output pin. HIGH when all power rails OK

EPD Power

U2
TPS651851RSLR

	1	VREF	EPAD	49	VNEG_IN
TPS_nINT	2	NINT	AGND2	48	R6 43k, TH1 10k/3380K, C24 4.7uF GND, 15V
−15V	3	VNEG	TS	47	
VNEG_IN	4	VNEG_IN	V3P3	46	EPD_VDD
TPS_WAKEUP	5	WAKEUP	VIN3P3	45	3.3V
	6	DGND	VPOS	44	C18 4.7uF, C21 4.7uF, C25 10uF GND
	7	INT_LDO	VPOS_IN	43	
	8	AGND1	VB	42	PWR_FLAG, D4, L2 2.2uH, 5V
−15V	9	VNEG_DIS	PGND1	41	
	10	VIN	VB_SW	40	
	11	NC	NC	39	
TPS_VCOM_CTRL	12	VCOM_CTRL	NC	38	
	13	NC	VDDH_IN	37	
	14	VCOM_DIS	VDDH_DRV	36	D5, D6, R10 1M, C26 2.2uF, PWR_FLAG, +22V
EP_VCOM	15	VCOM	VDDH_DIS	35	+22V, C17 10nF, C22 100nF GND
VNEG_IN	16	VCOM_PWR	VDDH_D	34	
SCL	17	SCL	VDDH_FB	33	
SDA	18	SDA	PGND2	32	
15V	19	VPOS_DIS	VEE_FB	31	GND
	20	NC	VEE_D	30	
TPS_PWRUP	21	PWRUP	VEE_DIS	29	−20V, C15 10nF, D2
VNEG_IN	22	PBKG	VEE_DRV	28	
TPS_PWR_GOOD	23	PWR_GOOD	VEE_IN	27	VNEG_IN
5V	24	VIN_P	VN	26	
			VN_SW	25	L1 4.7uH, D1, R7 1M, D3, R9 52.3k, C16 4.7uF GND, C19 2.2uF, PWR_FLAG

C10 4.7uF, C7 4.7uF, C1 4.7uF, C3 4.7uF, C8 22uF, C5 10uF, C4 4.7uF, C6 4.7uF, C9 22uF, C12 10uF

TP1 −15V, R2 47k, C2 1uF/25V
TP2 +15V, R3 47k, C14 1uF/25V
TP3 VCOM, R4 100k, C13 1uF/25V
Close to EPD connector

TP4 +22V, R5 47k, C11 1uF/50V
TP5 −20V, R8 47k, C20 1uF/50V

EPD_VDD, C27 10uF GND

EPD 6" Connector 34pin, 8bit

U3
ED060XC5

−15V	1	VNEG	
−20V	2	VEE	
	3	VSS	
	4	NC	
	5	NC	
	6	VDD	
EPD_VDD	7	VDD	
XCL	8	VSS	
	9	XCL	
LEH	10	VSS	
EP_OE	11	XLE	
XSTL	12	XOE	
D0	13	XSTL	
D1	14	D0	
D2	15	D1	
D3	16	D2	
D4	17	D3	
D5	18	D4	
D6	19	D5	
D7	20	D6	
EP_VCOM	21	D7	
	22	VCOM	
	23	NC	
	24	NC	
	25	NC	
	26	NC	
EP_MODE	27	VSS	
CKV	28	MODE1	
EP_STV	29	CKV	
	30	SPV	
BORDER	31	NC	
	32	BORDER	
15V	33	VSS	
+22V	34	VPOS	
		VGG	

BORDER: Not important, let's just leave it on a output header pin

This board aims to be a test-board to connect
an EINK panel (6" & 9.7") and test the signals+voltages
FASANI CORP.

Sheet: /		
File: pico-eink.kicad_sch		
Title: ALPHA Pico HAT board to test EINK signals		
Size: A3	Date: 2024-08-18	**Rev: 1.0**
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