Application Report

SLVA380A–November 2009–Revised June 2010

0.9-V to 3.2-V Input, 3.3-V Output, High-Efficiency Boost Converter with Ultra-Low Shutdown Current

PMP - DC/DC Low-Power Converters

ABSTRACT

This reference design is presented to help application designers and others who are trying to use the MSP430 in a system that requires a very low input voltage range while also maintaining high efficiency. Battery life is extended as well as a result of the low quiescent current (5 μA) and ultra-low shutdown current (5 nA) of the TPS61097-33. This particular design allows for an input voltage between 0.9 V and 3.2 V.

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1 Features

- 0.9-V to 3.2-V input voltage range
- Fixed 3.3-V output eliminates need for external voltage-setting resistors
- is capable of driving up to 100 mA (TPS61097-33)
- High efficiency (up to 94%)
- Low quiescent current (less than 5 μA)
- Ultra-low shutdown current (less than 5 nA)
- Small SOT23-5 package

2 Introduction

This reference design is for the MSP430 family of microcontroller devices and accounts for the voltage and current requirements as described herein. The MSP430 devices require only a single 3.3-V input; no sequencing is required. The operating input voltage for this reference design is 0.9 V to 3.2 V. This design is optimized for a very low input voltage range, small design with a low component count.

3 Requirements

The power requirements for each MSP430 family are listed below. The power given is based on the amount of current the core consumes per megahertz (MHz). The *Analog I_{MAX}* column indicates the amount of current added if the additional functional blocks are used.

For more information and other reference designs, please visit www.ti.com/processorpower.

Table 1. CC43 Family Power Requirements

DEVICE FAMILY	PIN NAME	VOLTAGE (V) MIN	VOLTAGE (V) MAX	CPU I_{MAX} (µA/MHz)	ANALOG I_{MAX} (µA)	SEQUENCING ORDER	TIMING DELAY	COMMENTS
F613x, F513x	A_{VCC}, D_{VCC} (1)	1.8	3.6	250 (2)	I_{REF} = 140	n/a	n/a	+Maximum CPU speed of 20 MHz

(1) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated during power-up.

(2) Maximum value for CPU clocked at 20 MHz at 3 V shown. Actual value depends on supply voltage and MCLK/internal regulator settings. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

Table 2. MSP430x1xx Family Power Requirements(1)

DEVICE FAMILY	PIN NAME	VOLTAGE (V) MIN	VOLTAGE (V) MAX	CPU I_{MAX} (µA/MHz) (2)	ANALOG I_{MAX} (µA)	COMMENTS
x11x1A	V_{CC}	1.8	3.6	350	Comp_A = 60	C11x1: 300 µA/MHz max
F12x	V_{CC}	1.8	3.6	350	Comp_A+ = 60	
F11x2, 12x2	V_{CC}	1.8	3.6	350	ADC10 = 1200, I_{REF} = 400	
F13x, 14x[1]	A_{VCC}, D_{VCC} (3)	1.8	3.6	560	Comp_A = 60, ADC12 = 1600, I_{REF} = 800	F13x, 14x: Comp_A, ADC12 F14x1: Comp_A
F15x, 16x, 161x	A_{VCC}, D_{VCC} (3)	1.8	3.6	600	Comp_A = 60, ADC12 = 1600, I_{REF} = 800, DAC12 = 1500	DAC outputs not loaded; DAC12 currents for a single DAC, max of two DAC12s in device)

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.

(2) 8-MHz maximum CPU clock speed (ex. Imax_x11x1 = 8 MHz × 350 µA = 2.8 mA). V_{CC} = D_{VCC} = A_{VCC} = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

(3) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated.

Table 3. MSP430x2xx Family Power Requirements(1)

DEVICE FAMILY	PIN NAME	VOLTAGE (V) MIN	VOLTAGE (V) MAX	CPU I_{MAX} (2) (µA/MHz)	ANALOG I_{MAX} (µA)	COMMENTS
F20xx	V_{CC}	1.8	3.6	370	Comp_A+ = 60 ADC10 = 1200, ADC10_I_{REF} = 400 SD16_A + I_{REF} = 1700 RefBuffer = 600	20x1: Comp_A+ 20x2: ADC10 20x3: SD16_A
F21x1	V_{CC}	1.8	3.6	410	Comp_A+ = 60	
F21x2	A_{VCC}, D_{VCC}	1.8	3.6	350	Comp_A+ = 60 ADC10 = 1200, I_{REF} = 400	
F22xx	A_{VCC}, D_{VCC} (3)	1.8	3.6	550	ADC12 = 1200, I_{REF} = 400 OA = 290	22x2: ADC10 22x4: ADC10, 2 OAs OA currents for a single amplifier
F23x0	A_{VCC}, D_{VCC} (3)	1.8	3.6	550	Comp_A + = 60	

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.

(2) 16 MHz maximum CPU clock speed (ex. Imax_20xx = 16 MHz × 370 µA = 5.90 mA). V_{CC} = D_{VCC} = A_{VCC} = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

(3) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated during power-up.

Table 3. MSP430x2xx Family Power Requirements[(1)] (continued)

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} [(2)] (µA/MHz)	ANALOG I_{MAX} (µA)	COMMENTS
		MIN	MAX			
F23x, 24x[1], 2410	A_{VCC}, D_{VCC} [(3)]	1.8	3.6	445	Comp_A + = 60, ADC12 = 1000, I_{REF} = 700	224x1: Comp_A+ 23x, 24x, 2410: Comp_A+, ADC12
F241x, 261x	A_{VCC}, D_{VCC} [(3)]	1.8	3.6	560	Comp_A + = 60, ADC12 = 1000, I_{REF} = 700 DAC12 = 1500	241x: Comp_A+, ADC12 261x: Comp_A+, ADC12, two DAC12s DAC12 outputs not loaded; DAC12 currents for a single DAC

Table 4. MSP430x4xx Family Power Requirements[(1)]

DEVICE FAMILY	PIN NAME [(2)]	VOLTAGE (V)		CPU I_{MAX} (µA/MHz) [(3)]	ANALOG I_{MAX} (µA)	COMMENTS
		MIN	MAX			
x41x	A_{VCC}, D_{VCC}	1.8	3.6	350	Comp_A = 60	C41x: 300 µA/MHz max
FW42x	A_{VCC}, D_{VCC}	1.8	3.6	350	Comp_A = 60 Scan IF = 650	
F42x	A_{VCC}, D_{VCC}	1.8	3.6	500	SD16 + I_{REF} = 1550 Ref Buffer = 600	SD16 current is for a single A/D (three on device)
FE42x[a], 42x2	A_{VCC}, D_{VCC}	1.8	3.6	500	ESP430CE1 = 4900 Ref Buffer = 600	ESP430 current for 4-MHz operation
F43x[1], F44x	A_{VCC}, D_{VCC}	1.8	3.6	560	Comp_A = 60, ADC12 = 1600, I_{REF} = 800	
F42x0	A_{VCC}, D_{VCC}	1.8	3.6	520	SD16_A + I_{REF}=1800 Ref Buffer = 600 DAC12=1500	DAC12 output not loaded
FG42x0	A_{VCC}, D_{VCC}	1.8	3.6	560	SD16_A + I_{REF}=1800 Ref Buffer = 600 DAC12 = 1500, OA = 290	DAC12 output not loaded; OA current for a single amplifier (two OAs in device)
FG43x	A_{VCC}, D_{VCC}	1.8	3.6	570	Comp_A = 60, ADC12 = 1600, I_{REF} = 800, DAC12 = 1500, OA = 490	DAC12 outputs not loaded; OA and DAC12 currents for a single amplifier/DAC (three OAs, two DACs in device)
FG46xx	A_{VCC}, D_{VCC}	1.8	3.6	740	Comp_A = 60, ADC12 = 1600, V_{REF} = 800, DAC12 = 1500, OA = 490	DAC12 outputs no loaded; OA and DAC12 currents for a single amplifier/DAC (three OAs, two DACs in device)
F47xx	A_{VCC}, D_{VCC}	1.8	3.6	560	Comp_A = 60, SD16_A + I_{REF} = 1700 Ref Buffer = 600	16 MHz max CUP frequency; SD16 current is for a single A/D (four on device)

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.

(2) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated.

(3) 8 MHz maximum CPU clock speed (ex. Imax_x41x = 8 MHz × 350 µA = 2.8 mA). (F47xx max CPU clock = 16 MHz) V_{CC} = D_{VCC} = A_{VCC} = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately. LCD current not included.

Table 5. MSP430x5xx Family Power Requirements[(1)]

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} (µA/MHz) (2)	ANALOG I_{MAX} (µA)	COMMENTS
		MIN	MAX			
F54xx	A_{VCC}, D_{VCC} (3)	2.2	3.6	348	ADC12_A = 220, I_{REF} = 190	18 MHz maximum CPU clock speed

(1) Additional 5-mA maximum required when writing/erasing Flash In-system.
(2) 16 MHz maximum at 3-V CPU clock speed. Actual value depends on supply voltage and MCLK/internal regulator settings. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.
(3) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated during power-up.

4 Schematic

The schematic for this design is shown in Figure 1.

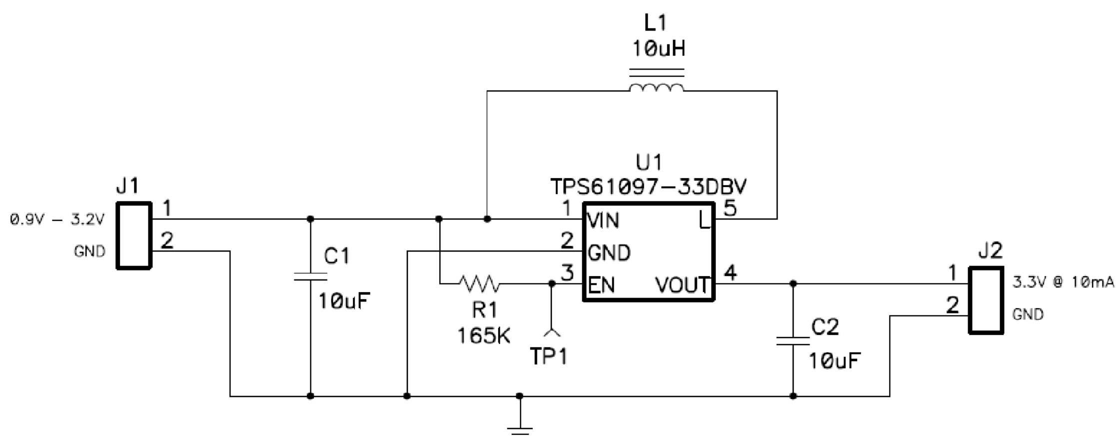

Figure 1. PMP5189 Reference Design Schematic

5 List of Materials

Table 6 shows the bill of materials (BOM) for this design.

Table 6. PMP5189 List of Materials

REF DES	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C1, C2	2	10 µF	Capacitor, ceramic, 6.3 V, X5R, 20%	0603	GRM188R60J106ME47D	muRata
J1, J2	2		Terminal block, 2-pin, 6-A, 3.5mm	0.27 × 0.25 in.	ED555/2DS	OST
L1	1	10 µH	Inductor, SMT, 0.75A, 520 mΩ	0.138 × 0.138 in.^{3}	DO3314-103MLC	Coilcraft
R1	1	165 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
TP1	1		Test Point, red, throughhole color keyed	0.1 × 0.1 in.	5000	Keystone
U1	1		Low-input, voltage synchronous boost converter	SOT23	TPS61097-33DBV	TI

6 Test Results

6.1 Startup

Figure 2 shows the 3.3-V output voltage startup waveform after an input voltage of 0.9 V is applied. I_{OUT} = 0 A. Figure 3 shows the 3.3-V output voltage startup waveform after an input voltage of 3.2 V is applied.

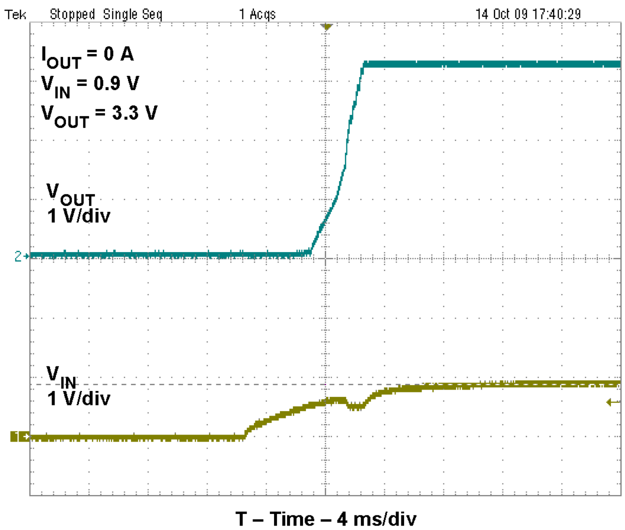

Figure 2. Startup Waveform, V_{IN} = 0.9 V

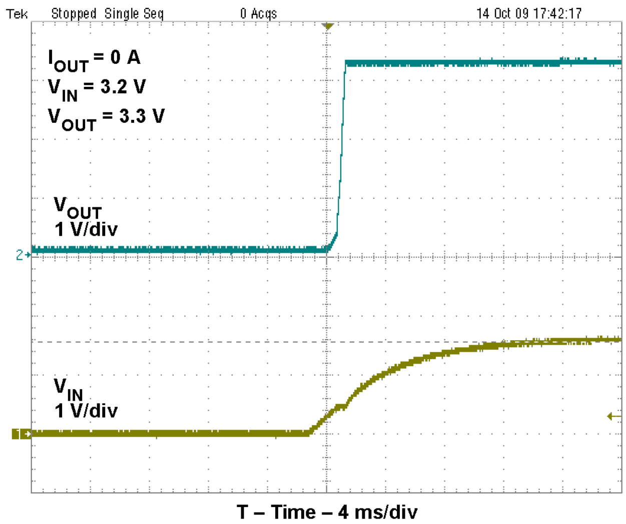

Figure 3. Startup Waveform, V_{IN} = 3.2 V

6.2 Efficiency

The converter efficiency performance is shown in Figure 4. Table 7 and Table 8 present the efficiency data with V_{IN} = 0.9 V and 3.2 V, respectively.

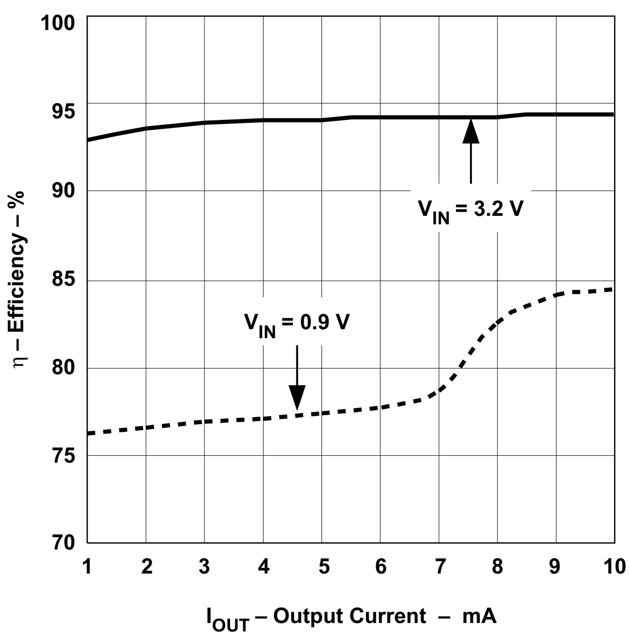

Figure 4. Efficiency

Table 7. Efficiency Data: V_{IN} = 0.9 V

INPUT VOLTAGE V_{IN} (V)	INPUT CURRENT I_{IN} (mA)	OUTPUT VOLTAGE V_{OUT} (V)	OUTPUT CURRENT I_{OUT} (mA)	INPUT POWER (mW)	OUPTUT POWER (mW)	EFFICIENCY (%)
0.900	4.79	3.285	1.00	4.31	3.29	76.2
0.901	9.52	3.284	2.00	8.58	6.57	76.6
0.903	14.20	3.284	3.00	12.82	9.85	76.8
0.900	18.96	3.284	4.00	17.06	13.14	77.0
0.902	23.53	3.284	5.00	21.22	16.42	77.4
0.899	28.28	3.284	6.01	25.42	19.74	77.6
0.902	32.40	3.284	7.00	29.22	22.99	78.7
0.902	35.22	3.283	7.99	31.77	26.23	82.6
0.900	39.06	3.283	9.00	35.15	29.55	84.1
0.903	43.00	3.283	9.99	38.83	32.80	84.5

Table 8. Efficiency Data: V_{IN} = 3.2 V

INPUT VOLTAGE V_{IN} (V)	INPUT CURRENT I_{IN} (mA)	OUTPUT VOLTAGE V_{OUT} (V)	OUTPUT CURRENT I_{OUT} (mA)	INPUT POWER (mW)	OUPTUT POWER (mW)	EFFICIENCY (%)
3.199	1.11	3.300	1.00	3.55	3.30	92.9
3.202	2.20	3.299	2.00	7.04	6.60	93.7
3.200	3.29	3.298	3.00	10.53	9.89	94.0
3.204	4.38	3.298	4.00	14.03	13.19	94.0
3.202	5.47	3.297	5.00	17.51	16.49	94.1
3.200	6.56	3.296	6.00	20.99	19.78	94.2
3.203	7.66	3.296	7.01	24.53	23.10	94.2
3.201	8.74	3.296	8.00	27.98	26.37	94.3
3.199	9.84	3.295	9.01	31.48	29.69	94.3
3.202	10.91	3.295	10.00	34.93	32.95	94.3

6.3 Output Ripple Voltage

Figure 5 and Figure 6 illustrate the design output ripple performance for I_{OUT} = 10 mA and 0 mA, respectively.

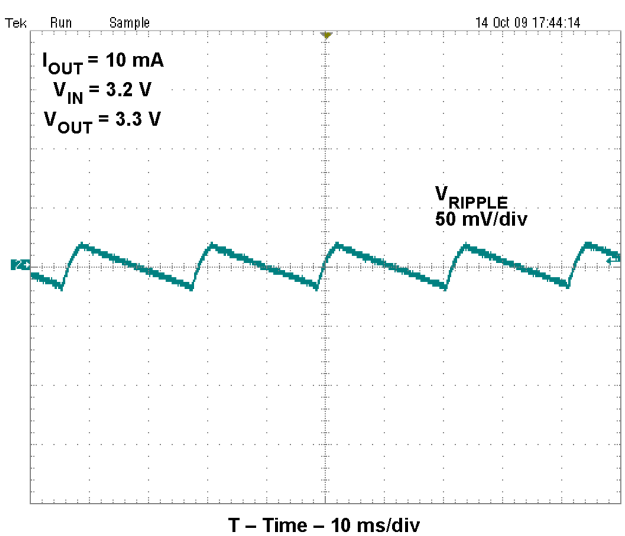

Figure 5. Output Ripple Voltage, I_{OUT} = 10 mA

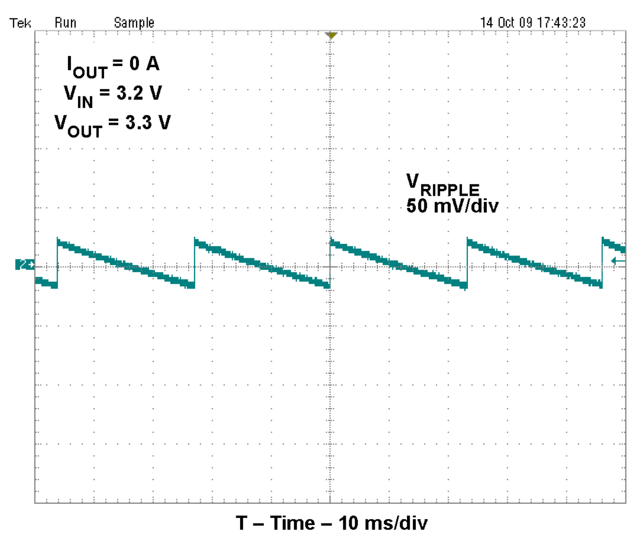

Figure 6. Output Ripple Voltage, I_{OUT} = 0 mA