- **Low Supply Voltage Range: 1.8 V to 3.6 V**
- **Ultralow Power Consumption**
  - **Active Mode: 250 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.7 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Ultrafast Wake-Up From Standby Mode in less than 1 µs**
- **16-Bit RISC Architecture, 62.5 ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Internal Frequencies up to 16MHz With Four Calibrated Frequencies to ±1%**
  - **32-kHz Crystal**
  - **High-Frequency Crystal up to 16MHz**
  - **Resonator**
  - **External Digital Clock Source**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **On-Chip Comparator for Analog Signal Compare Function or Slope A/D Conversion**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **On Chip Emulation Module**
- **Family Members Include:**
  MSP430F2101: 1KB + 256B Flash Memory 128B RAM
  MSP430F2111: 2KB + 256B Flash Memory 128B RAM
  MSP430F2121: 4KB + 256B Flash Memory 256B RAM
  MSP430F2131: 8KB + 256B Flash Memory 256B RAM
- **Available in a 20-Pin Plastic Small-Outline Wide Body (SOWB) Package, 20-Pin Plastic Small-Outline Thin (TSSOP) Package, 20-Pin TVSOP and 24-Pin QFN**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)**

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1µs.

The MSP430x21x1 series is an ultralow-power mixed signal microcontroller with a built-in 16-bit timer, versatile analog comparator, and sixteen I/O pins.

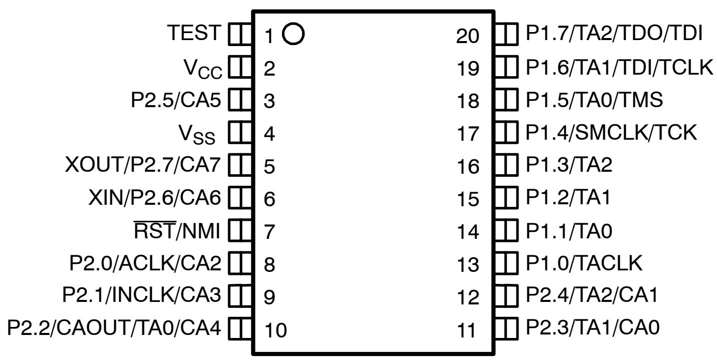
Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand-alone RF sensor front end is another area of application. The analog comparator provides slope A/D conversion capability.

AVAILABLE OPTIONS

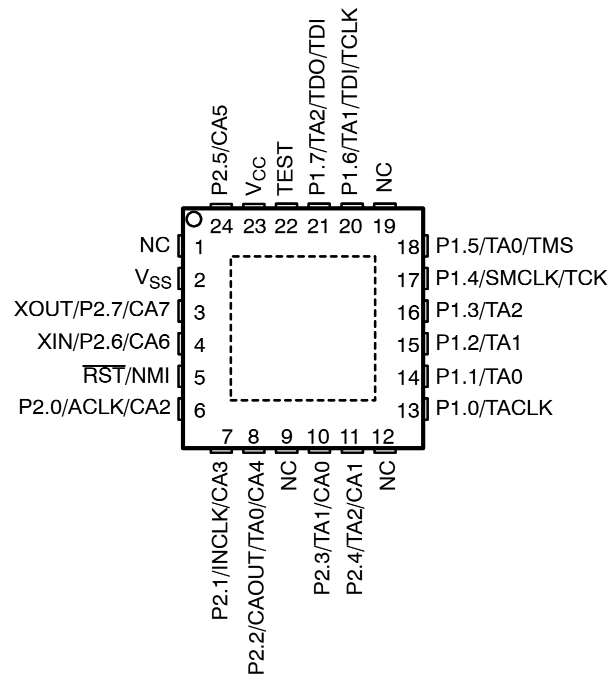
T_A	PACKAGED DEVICES			
	PLASTIC 20-PIN SOWB (DW)	PLASTIC 20-PIN TSSOP (PW)	PLASTIC 20-PIN TVSOP (DGV)	PLASTIC 24-PIN QFN (RGE)
−40°C to 85°C	MSP430F2101IDW MSP430F2111IDW MSP430F2121IDW MSP430F2131IDW	MSP430F2101IPW MSP430F2111IPW MSP430F2121IPW MSP430F2131IPW	MSP430F2101IDGV MSP430F2111IDGV MSP430F2121IDGV MSP430F2131IDGV	MSP430F2101IRGE MSP430F2111IRGE MSP430F2121IRGE MSP430F2131IRGE
−40°C to 105°C	MSP430F2101TDW MSP430F2111TDW MSP430F2121TDW MSP430F2131TDW	MSP430F2101TPW MSP430F2111TPW MSP430F2121TPW MSP430F2131TPW	MSP430F2101TDGV MSP430F2111TDGV MSP430F2121TDGV MSP430F2131TDGV	MSP430F2101TRGE MSP430F2111TRGE MSP430F2121TRGE MSP430F2131TRGE

device pinout

DW, PW, or DGV PACKAGE
(TOP VIEW)

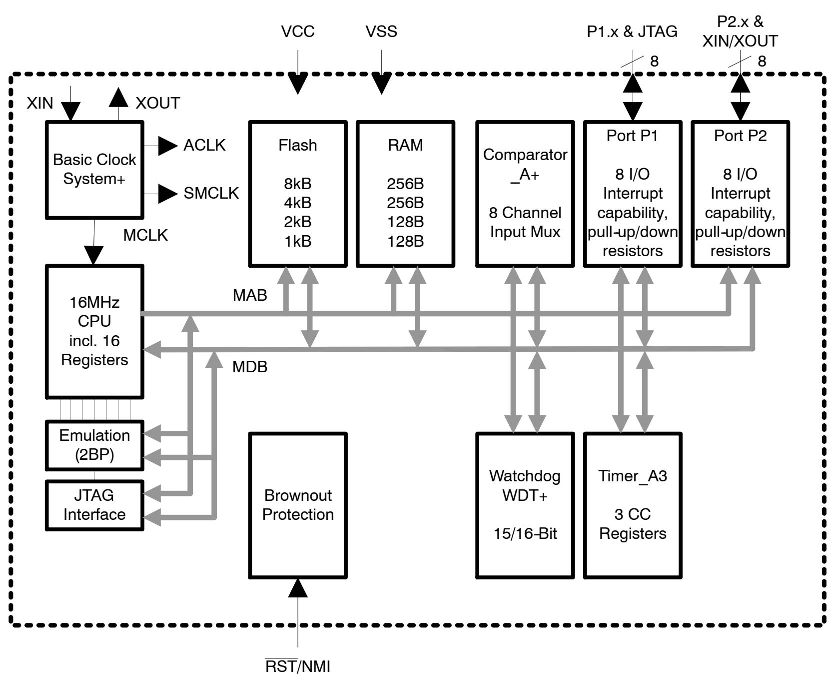


RGE PACKAGE
(TOP VIEW)



Note: NC pins not internally connected
Power Pad connection to V_{SS} recommended

functional block diagram



NOTE: See port schematics section for detailed I/O information.

Terminal Functions

TERMINAL				DESCRIPTION
NAME	DW, PW, or DGV NO.	RGE NO.	I/O	
P1.0/TACLK	13	13	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input
P1.1/TA0	14	14	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	15	15	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	16	16	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK/TCK	17	17	I/O	General-purpose digital I/O pin / SMCLK signal output Test Clock input for device programming and test
P1.5/TA0/TMS	18	18	I/O	General-purpose digital I/O pin / Timer_A, compare: Out0 output Test Mode Select input for device programming and test
P1.6/TA1/TDI/TCLK	19	20	I/O	General-purpose digital I/O pin / Timer_A, compare: Out1 output Test Data Input or Test Clock Input for programming and test
P1.7/TA2/TDO/TDI†	20	21	I/O	General-purpose digital I/O pin / Timer_A, compare: Out2 output Test Data Output or Test Data Input for programming and test
P2.0/ACLK/CA2	8	6	I/O	General-purpose digital I/O pin / ACLK output Comparator_A+, CA2 input
P2.1/INCLK/CA3	9	7	I/O	General-purpose digital I/O pin / Timer_A, clock signal at INCLK Comparator_A+, CA3 input
P2.2/CAOUT/ TA0/CA4	10	8	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input/BSL receive Comparator_A+, output / CA4 input
P2.3/CA0/TA1	11	10	I/O	General-purpose digital I/O pin / Timer_A, compare: Out1 output Comparator_A+, CA0 input
P2.4/CA1/TA2	12	11	I/O	General-purpose digital I/O pin / Timer_A, compare: Out2 output Comparator_A+, CA1 input
P2.5/CA5	3	24	I/O	General-purpose digital I/O pin Comparator_A+, CA5 input
XIN/P2.6/CA6	6	4	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Comparator_A+, CA6 input
XOUT/P2.7/CA7	5	3	I/O	Output terminal of crystal oscillator general-purpose digital I/O pin Comparator_A+, CA7 input
$\overline{\text{RST}}$/NMI	7	5	I	Reset or nonmaskable interrupt input
TEST	1	22	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST.
V_{CC}	2	23		Supply voltage
V_{SS}	4	2		Ground reference
QFN Pad	NA	Package Pad	NA	QFN package pad connection to V_{SS} recommended.

† TDO or TDI is selected via JTAG instruction.

NOTE: If XOUT/P2.7/CA7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

short-form description

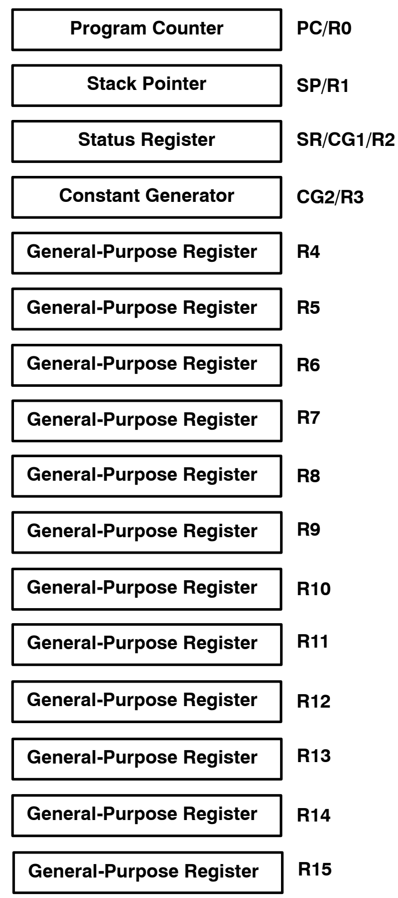
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; Table 2 shows the address modes.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 −−−> R5
Single operands, destination only	e.g. CALL R8	PC −−>(TOS), R8−−> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 −−> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)−−> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) −−> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) −−> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) −−> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) −−> R11 R10 + 2−−> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 −−> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed) the CPU goes into LPM4 immediately after power−up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash key violation PC out-of-range (see Note 1)	PORIFG RSTIFG WDTIFG KEYV (see Note 2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 2 and 4)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	30
			0FFFAh	29
			0FFF8h	28
Comparator_A+	CAIFG	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer_A3	TACCR0 CCIFG (see Note 3)	maskable	0FFF2h	25
Timer_A3	TACCR2, TACCR1 CCIFG, TAIFG (see Notes 2 and 3)	maskable	0FFF0h	24
			0FFEEh	23
			0FFECh	22
			0FFEAh	21
			0FFE8h	20
I/O Port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 2 and 3)	maskable	0FFE6h	19
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 2 and 3)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
(see Note 5)			0FFDEh	15
(see Note 6)			0FFDCh to 0FFC0h	14 to 0, lowest

NOTES:
1. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh).
2. Multiple source flags
3. Interrupt flags are located in the module
4. (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
5. This location is used as bootstrap loader security key (BSLSKEY).
   A value of 0AA55h at this location disables the BSL completely.
   A value of 0h disables the erasure of the flash if an invalid password is supplied.
6. The interrupt vectors at addresses 0FFDCh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE: Oscillator fault enable
NMIIE: (Non)maskable interrupt enable
ACCVIE: Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h								

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG: Flag set on oscillator fault
RSTIFG: External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up
PORIFG: Power-On Reset interrupt flag. Set on V_{CC} power-up.
NMIIFG: Set via $\overline{RST}$/NMI-pin

Address	7	6	5	4	3	2	1	0
03h								

Legend

rw:	Bit can be read and written.
rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
rw-(0,1):	Bit can be read and written. It is Reset or Set by POR.
(shaded box)	SFR bit is not present in device

memory organization

		MSP430F2101	MSP430F2111	MSP430F2121	MSP430F2131
Memory Main: interrupt vector Main: code memory	Size Flash Flash	1KB Flash 0FFFFh−0FFE0h 0FFFFh−0FC00h	2KB Flash 0FFFFh−0FFE0h 0FFFFh−0F800h	4KB Flash 0FFFFh−0FFE0h 0FFFFh−0F000h	8KB Flash 0FFFFh−0FFE0h 0FFFFh−0E000h
Information memory	Size Flash	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h
Boot memory	Size ROM	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h
RAM	Size	128 Byte 027Fh − 0200h	128 Byte 027Fh − 0200h	256 Byte 02FFh − 0200h	256 Byte 02FFh − 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. A bootstrap loader security key is provided at address 0FFDEh to disable the BSL completely or to disable the erasure of the flash if an invalid password is supplied. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

BSLKEY	DESCRIPTION
00000h	Erasure of flash disabled if an invalid password is supplied
0AA55h	BSL disabled
any other value	BSL enabled

BSL FUNCTION	DW, PW, DGV PACKAGE PINS	RGE PACKAGE PINS
Data Transmit	14 - P1.1	14 - P1.1
Data Receive	10 - P2.2	8 - P2.2

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory.*
- Segment A contains calibration data. After reset segment A is protected against programming or erasing. It can be unlocked but care should be taken not to erase this segment if the calibration data is required.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x2xx Family User's Guide.*

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

DCO CALIBRATION DATA (PROVIDED FROM FACTORY IN FLASH INFO MEMORY SEGMENT A)			
DCO FREQUENCY	CALIBRATION REGISTER	SIZE	ADDRESS
1 MHz	CALBC1_1MHZ	byte	010FFh
	CALDCO_1MHZ	byte	010FEh
8 MHz	CALBC1_8MHZ	byte	010FDh
	CALDCO_8MHZ	byte	010FCh
12 MHz	CALBC1_12MHZ	byte	010FBh
	CALDCO_12MHZ	byte	010FAh
16 MHz	CALBC1_16MHZ	byte	010F9h
	CALDCO_16MHZ	byte	010F8h

brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

digital I/O

There are two 8-bit I/O ports implemented—ports P1 and P2:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pull-up/pull-down resistor.

WDT+ watchdog timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

Comparator_A+

The primary function of the Comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A3 SIGNAL CONNECTIONS

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
DW, PW, DGV	RGE					DW, PW, DGV	RGE
13 - P1.0	13 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 - P2.1	7 - P2.1	INCLK	INCLK				
14 - P1.1	14 - P1.1	TA0	CCI0A	CCR0	TA0	14 - P1.1	14 - P1.1
10 - P2.2	8 - P2.2	TA0	CCI0B			18 - P1.5	18 - P1.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				
15 - P1.2	15 - P1.2	TA1	CCI1A	CCR1	TA1	11 - P2.3	10 - P2.3
		CAOUT (internal)	CCI1B			15 - P1.2	15 - P1.2
		V_{SS}	GND			19 - P1.6	20 - P1.6
		V_{CC}	V_{CC}				
16 - P1.3	16 - P1.3	TA2	CCI2A	CCR2	TA2	12 - P2.4	11 - P2.4
		ACLK (internal)	CCI2B			16 - P1.3	16 - P1.3
		V_{SS}	GND			20 - P1.7	21 - P1.7
		V_{CC}	V_{CC}				

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Timer_A	Capture/compare register Capture/compare register Capture/compare register Timer_A register Capture/compare control Capture/compare control Capture/compare control Timer_A control Timer_A interrupt vector	TACCR2 TACCR1 TACCR0 TAR TACCTL2 TACCTL1 TACCTL0 TACTL TAIV	0176h 0174h 0172h 0170h 0166h 0164h 0162h 0160h 012Eh
Flash Memory	Flash control 3 Flash control 2 Flash control 1	FCTL3 FCTL2 FCTL1	012Ch 012Ah 0128h
Watchdog TImer+	Watchdog/timer control	WDTCTL	0120h
PERIPHERALS WITH BYTE ACCESS			
Comparator_A+	Comparator_A+ port disable Comparator_A+ control 2 Comparator_A+ control 1	CAPD CACTL2 CACTL1	05Bh 05Ah 059h
Basic Clock	Basic clock system control 3 Basic clock system control 2 Basic clock system control 1 DCO clock frequency control	BCSCTL3 BCSCTL2 BCSCTL1 DCOCTL	053h 058h 057h 056h
Port P2	Port P2 resistor enable Port P2 selection Port P2 interrupt enable Port P2 interrupt edge select Port P2 interrupt flag Port P2 direction Port P2 output Port P2 input	P2REN P2SEL P2IE P2IES P2IFG P2DIR P2OUT P2IN	02Fh 02Eh 02Dh 02Ch 02Bh 02Ah 029h 028h
Port P1	Port P1 resistor enable Port P1 selection Port P1 interrupt enable Port P1 interrupt edge select Port P1 interrupt flag Port P1 direction Port P1 output Port P1 input	P1REN P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN	027h 026h 025h 024h 023h 022h 021h 020h
Special Function	SFR interrupt flag 2 SFR interrupt flag 1 SFR interrupt enable 2 SFR interrupt enable 1	IFG2 IFG1 IE2 IE1	003h 002h 001h 000h

absolute maximum ratings (see Note 1)

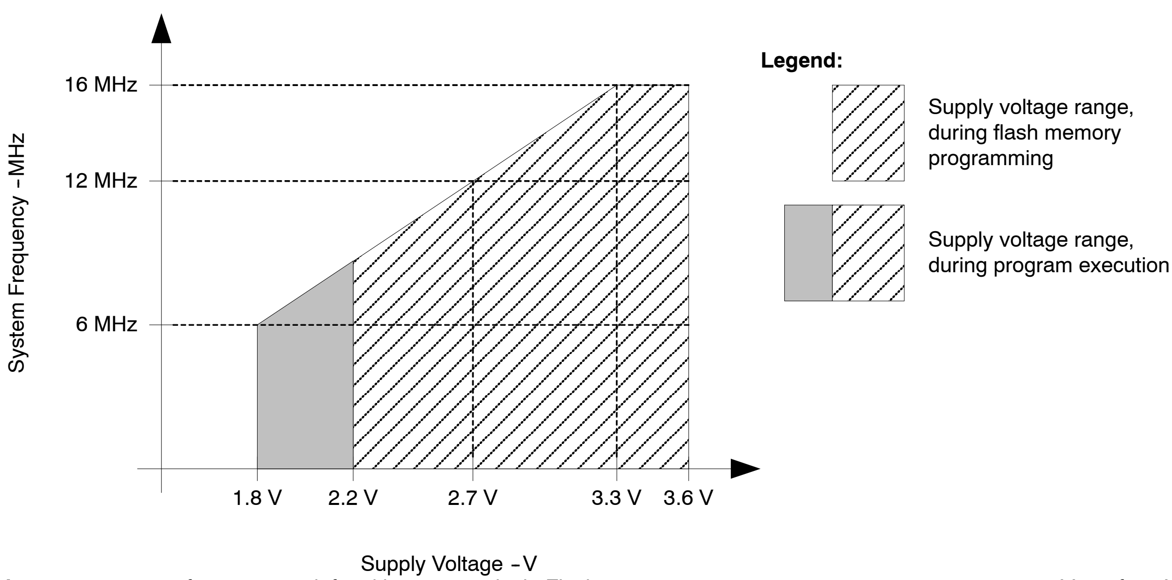
Voltage applied at V_{CC} to V_{SS} . . . . . −0.3 V to 4.1 V
Voltage applied to any pin (see Note 2) . . . . . −0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg} (unprogrammed device, see Note 3) . . . . . −55°C to 150°C
Storage temperature, T_{stg} (programmed device, see Note 3) . . . . . −40°C to 85°C

NOTES: 1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J−STD−020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage during program execution, V_{CC}		1.8		3.6	V
Supply voltage during program/erase flash memory, V_{CC}		2.2		3.6	V
Supply voltage, V_{SS}			0		V
Operating free-air temperature range, T_A	I Version	−40		85	°C
	T Version	−40		105	°C
Processor frequency f_{SYSTEM} (Maximum MCLK frequency) (see Notes 1, 2 and Figure 1)	V_{CC} = 1.8 V, Duty Cycle = 50% ±10%	0		6	MHz
	V_{CC} = 2.7 V, Duty Cycle = 50% ±10% (see Note 3)	0		12	
	V_{CC} = 3.3 V, Duty Cycle = 50% ±10% (see Note 4)	0		16	

NOTES: 1. The MSP430 CPU is clocked directly with MCLK.
Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
2. Modules might have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.
3. This includes using the provided DCO calibration value for 12 MHz for V_{CC} = 2.7 V to 3.6 V over the operating temperature range.
4. This includes using the provided DCO calibration value for 16 MHz for V_{CC} = 3.3 V to 3.6 V over the operating temperature range.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

active mode supply current (into V_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1MHz, f_{ACLK} = 32,768Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		250	300	μA
				3 V		350	410	
$I_{AM,1MHz}$	Active mode (AM) current (1MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1MHz, f_{ACLK} = 32,768Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		200		μA
				3 V		300		
$I_{AM,4kHz}$	Active mode (AM) current (4kHz)	$f_{MCLK} = f_{SMCLK} =$ f_{ACLK} = 32,768Hz/8 = 4,096Hz, f_{DCO} = 0Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40–85°C	2.2 V		2	5	μA
			105°C	2.2 V			6	
			-40–85°C	3 V		3	9	
			105°C	3 V			9	
$I_{AM,100kHz}$	Active mode (AM) current (100kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)} \approx$ 100kHz, f_{ACLK} = 0Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1		2.2 V		60	85	μA
				3 V		72	95	

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a Micro Crystal CC4V–T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9pF.

typical characteristics − active mode supply current (into V_{CC})

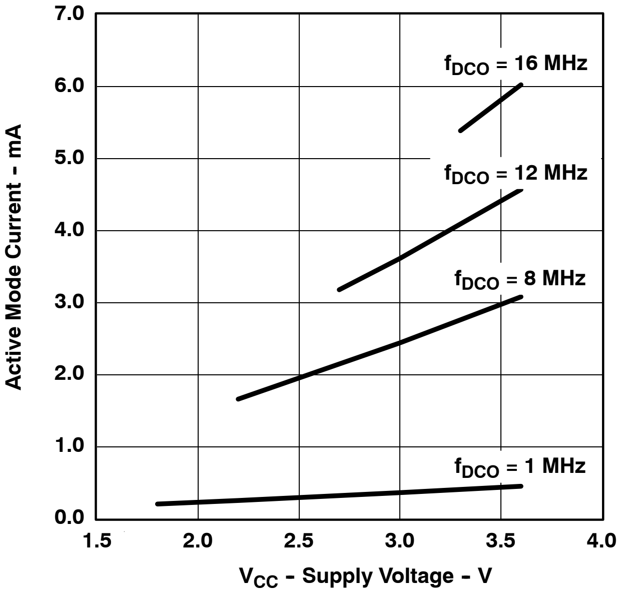


Figure 2. Active mode current vs V_{CC}, T_A = 25°C

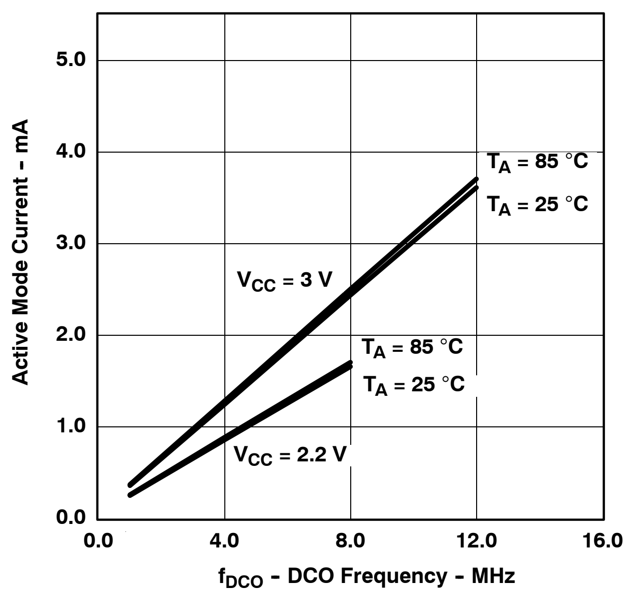


Figure 3. Active mode current vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

low power mode supply currents (into V_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current, see Note 3	f_{MCLK} = 0MHz, f_{SMCLK} = f_{DCO} = 1MHz, f_{ACLK} = 32,768Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		65	80	μA
				3 V		85	100	
$I_{LPM0,100kHz}$	Low-power mode 0 (LPM0) current, see Note 3	f_{MCLK} = 0MHz, f_{SMCLK} = $f_{DCO(0, 0)}$ ≈ 100kHz, f_{ACLK} = 0Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1		2.2 V		37	48	μA
				3 V		41	52	
I_{LPM2}	Low-power mode 2 (LPM2) current, see Note 4	f_{MCLK} = f_{SMCLK} = 0MHz, f_{DCO} = 1MHz, f_{ACLK} = 32,768Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40−85°C	2.2 V		22	29	μA
			105°C				31	
			-40−85°C	3 V		25	32	
			105°C				34	
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current, see Note 4	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0MHz, f_{ACLK} = 32,768Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.7	1.2	μA
			25°C			0.7	1.0	
			85°C			1.6	2.3	
			105°C			3	6	
			-40°C	3 V		0.9	1.2	μA
			25°C			0.9	1.2	
			85°C			1.6	2.8	
			105°C			3	7	
I_{LPM4}	Low-power mode 4 (LPM4) current, see Note 5	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0MHz, f_{ACLK} = 0Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C	2.2 V/3 V		0.1	0.5	μA
			25°C			0.1	0.5	
			85°C			0.8	1.9	
			105°C			2	4	

NOTES:
1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a Micro Crystal CC4V−T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
3. Current for brownout and WDT clocked by SMCLK included.
4. Current for brownout and WDT clocked by ACLK included.
5. Current for brownout included.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1 and P2

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45		0.75	V_{CC}
			2.2 V	1.00		1.65	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25		0.55	V_{CC}
			2.2 V	0.55		1.20	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		2.2 V	0.2		1.0	V
			3 V	0.3		1.0	
R_{Pull}	Pullup/pulldown resistor	For pull–up: V_{IN} = V_{SS}; For pull–down: V_{IN} = V_{CC}		20	35	50	kΩ
C_I	Input capacitance	V_{IN} = V_{SS} or V_{CC}			5		pF

inputs – Ports P1 and P2

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger puls width to set interrupt flag, (see Note 1)	2.2 V/3 V	20			ns

NOTES: 1. An external signal sets the interrupt flag every time the minimum interrupt puls width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current – Ports P1 and P2

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	see Notes 1 and 2	2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs − Ports P1 and P2

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = −1.5 mA (see Note 1)	2.2 V	V_{CC}−0.25		V_{CC}	V
		$I_{(OHmax)}$ = −6 mA (see Note 2)	2.2 V	V_{CC}−0.6		V_{CC}	
		$I_{(OHmax)}$ = −1.5 mA (see Note 1)	3 V	V_{CC}−0.25		V_{CC}	
		$I_{(OHmax)}$ = −6 mA (see Note 2)	3 V	V_{CC}−0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA (see Note 1)	2.2 V	V_{SS}		V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA (see Note 2)	2.2 V	V_{SS}		V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA (see Note 1)	3 V	V_{SS}		V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA (see Note 2)	3 V	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

output frequency − Ports P1 and P2

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kOhm (see Note 1 and 2)	2.2 V			10	MHz
			3 V			12	MHz
f_{Port_CLK}	Clock output frequency	P2.0/ACLK, P1.4/SMCLK, C_L = 20 pF (see Note 2)	2.2 V			12	MHz
			3 V			16	MHz

NOTES: 1. A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
2. The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – outputs

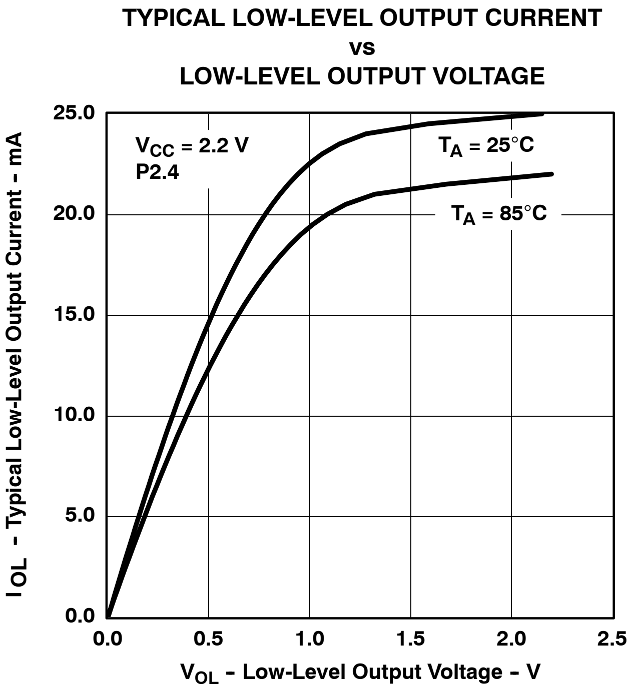


Figure 4

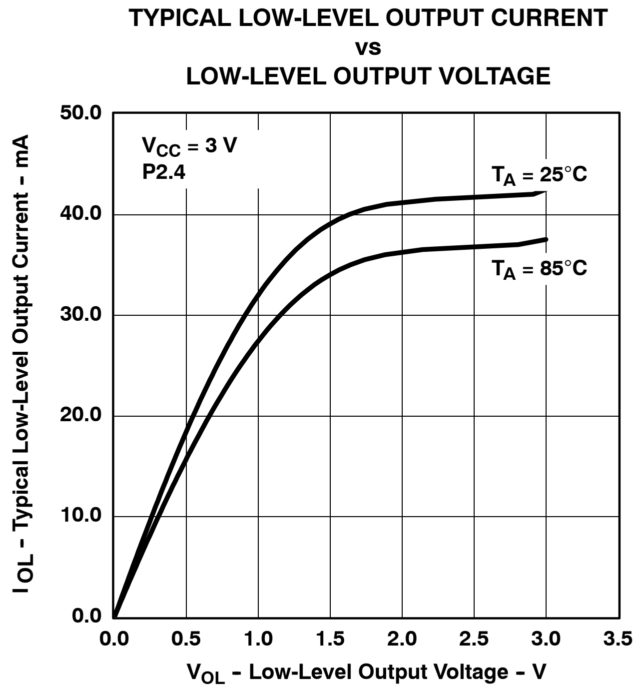


Figure 5

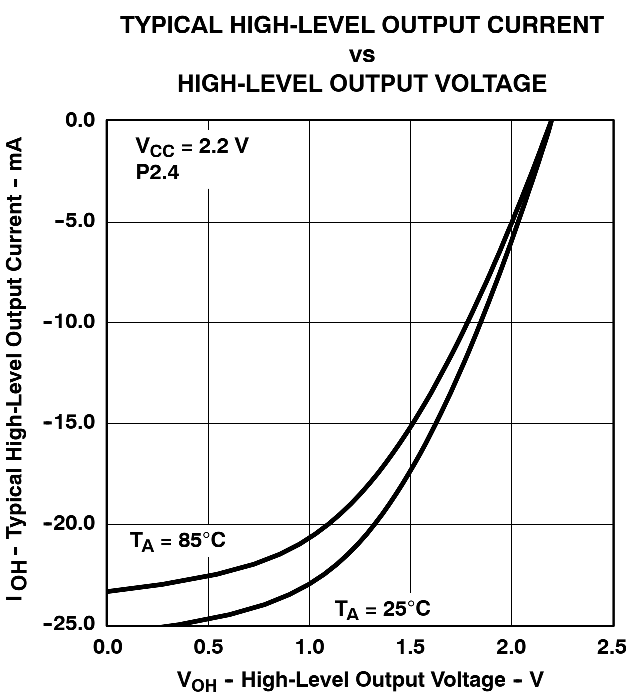


Figure 6

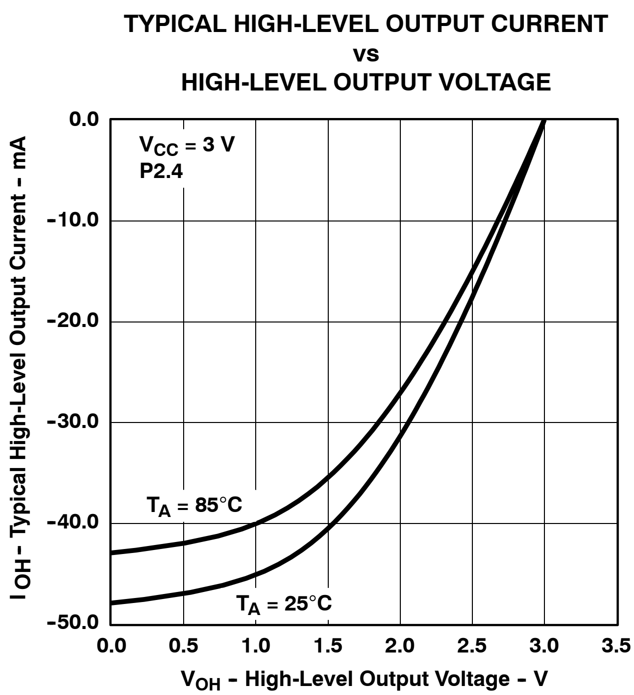


Figure 7

NOTE: One output loaded at a time.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	(see Figure 8)	$dV_{CC}/dt \le 3$ V/s				$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	(see Figure 8 through Figure 10)	$dV_{CC}/dt \le 3$ V/s					1.71	V
$V_{hys(B\_IT-)}$	(see Figure 8)	$dV_{CC}/dt \le 3$ V/s	-40°C–85°C		70	130	180	mV
			105°C		70	130	210	mV
$t_{d(BOR)}$	(see Figure 8)						2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally			2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

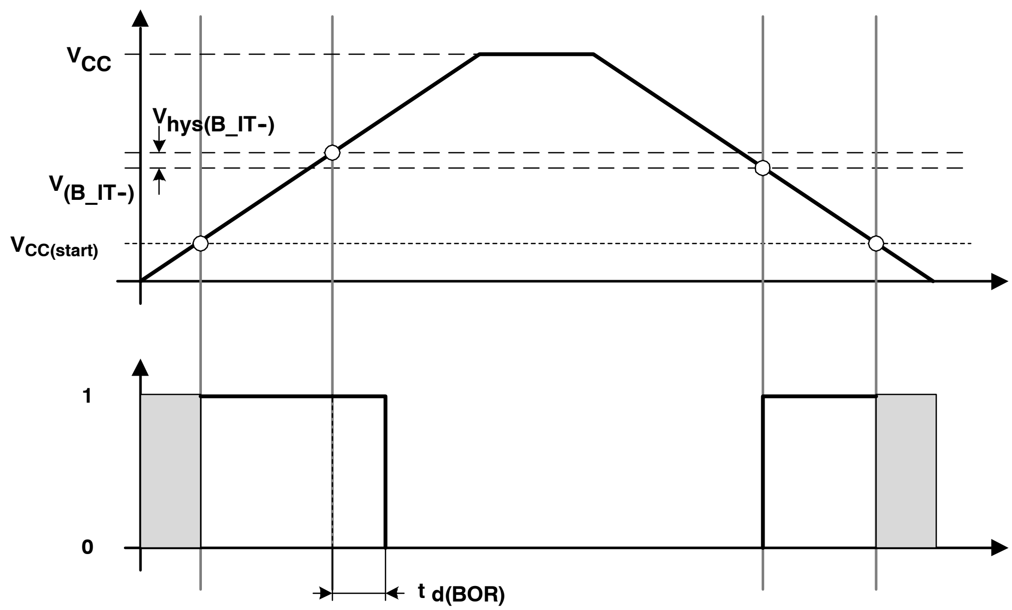


Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – POR/brownout reset (BOR)

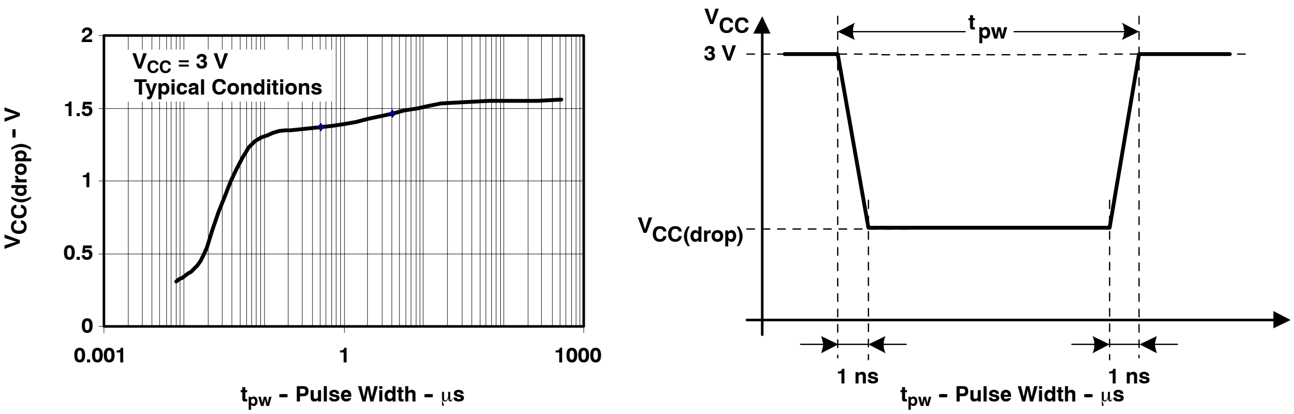


Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

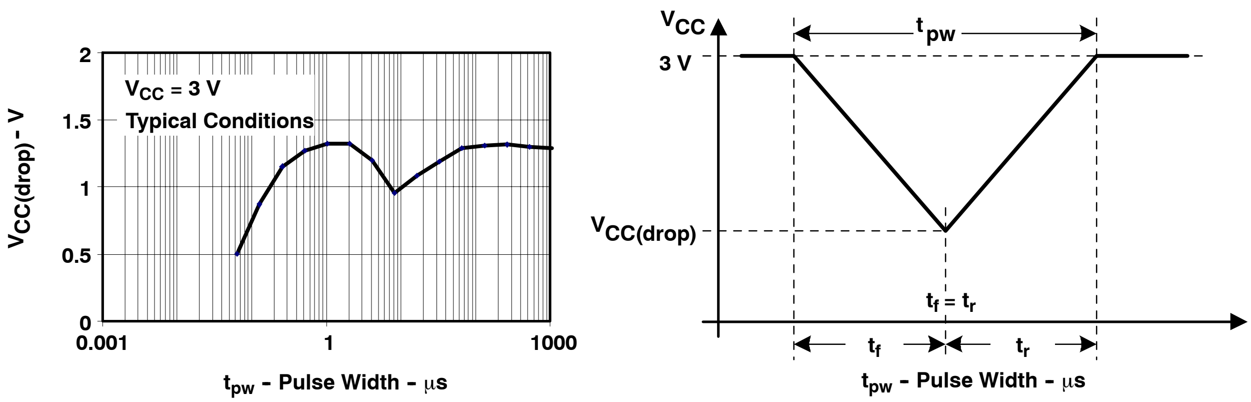


Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO frequency

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Vcc	Supply voltage range	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	V
		RSELx = 15		3.0		3.6	V
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V			1.55	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.05	1.08	1.12	ratio
Duty Cycle		Measured at P1.4/SMCLK	2.2 V/3 V	40	50	60	%

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies − tolerance at calibration

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
Frequency tolerance at calibration			25°C	3 V	−1	±0.2	+1	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ DCOCTL = CALDCO_1MHZ Gating time: 5ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ DCOCTL = CALDCO_8MHZ Gating time: 5ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ DCOCTL = CALDCO_12MHZ Gating time: 5ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ DCOCTL = CALDCO_16MHZ Gating time: 2ms	25°C	3 V	15.84	16	16.16	MHz

calibrated DCO frequencies − tolerance over temperature 0°C − +85°C

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature			0−85°C	3.0 V	−2.5	±0.5	+2.5	%
8-MHz tolerance over temperature			0−85°C	3.0 V	−2.5	±1.0	+2.5	%
12-MHz tolerance over temperature			0−85°C	3.0 V	−2.5	±1.0	+2.5	%
16-MHz tolerance over temperature			0−85°C	3.0 V	−3.0	±2.0	+3.0	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ DCOCTL = CALDCO_1MHZ Gating time: 5ms	0−85°C	2.2 V	0.970	1	1.030	MHz
				3.0 V	0.975	1	1.025	MHz
				3.6 V	0.970	1	1.030	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ DCOCTL = CALDCO_8MHZ Gating time: 5ms	0−85°C	2.2 V	7.760	8	8.400	MHz
				3.0 V	7.800	8	8.200	MHz
				3.6 V	7.600	8	8.240	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ DCOCTL = CALDCO_12MHZ Gating time: 5ms	0−85°C	2.2 V	11.70	12	12.30	MHz
				3.0 V	11.70	12	12.30	MHz
				3.6 V	11.70	12	12.30	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ DCOCTL = CALDCO_16MHZ Gating time: 2ms	0−85°C	3.0 V	15.52	16	16.48	MHz
				3.6 V	15.00	16	16.48	MHz

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies – tolerance over supply voltage V_{CC}

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over V_{CC}			25°C	1.8 V – 3.6 V	−3	±2	+3	%
8-MHz tolerance over V_{CC}			25°C	1.8 V – 3.6 V	−3	±2	+3	%
12-MHz tolerance over V_{CC}			25°C	2.2 V – 3.6 V	−3	±2	+3	%
16-MHz tolerance over V_{CC}			25°C	3.0 V – 3.6 V	−3	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ DCOCTL = CALDCO_1MHZ Gating time: 5ms	25°C	1.8 V – 3.6 V	0.970	1	1.030	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ DCOCTL = CALDCO_8MHZ Gating time: 5ms	25°C	1.8 V – 3.6 V	7.760	8	8.240	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ DCOCTL = CALDCO_12MHZ Gating time: 5ms	25°C	2.2 V – 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ DCOCTL = CALDCO_16MHZ Gating time: 2ms	25°C	3.0 V – 3.6 V	15.00	16	16.48	MHz

calibrated DCO frequencies – overall tolerance

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance overall			I: -40–85°C T: -40–105°C	1.8 V – 3.6 V	−5	±2	+5	%
8-MHz tolerance overall			I: -40–85°C T: -40–105°C	1.8 V – 3.6 V	−5	±2	+5	%
12-MHz tolerance overall			I: -40–85°C T: -40–105°C	2.2 V – 3.6 V	−5	±2	+5	%
16-MHz tolerance overall			I: -40–85°C T: -40–105°C	3.0 V – 3.6 V	−6	±3	+6	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ DCOCTL = CALDCO_1MHZ Gating time: 5ms	I: -40–85°C T: -40–105°C	1.8 V – 3.6 V	0.950	1	1.050	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ DCOCTL = CALDCO_8MHZ Gating time: 5ms	I: -40–85°C T: -40–105°C	1.8 V – 3.6 V	7.600	8	8.400	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ DCOCTL = CALDCO_12MHZ Gating time: 5ms	I: -40–85°C T: -40–105°C	2.2 V – 3.6 V	11.40	12	12.60	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ DCOCTL = CALDCO_16MHZ Gating time: 2ms	I: -40–85°C T: -40–105°C	3.0 V – 3.6 V	15.00	16	17.00	MHz

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – calibrated 1MHz DCO frequency

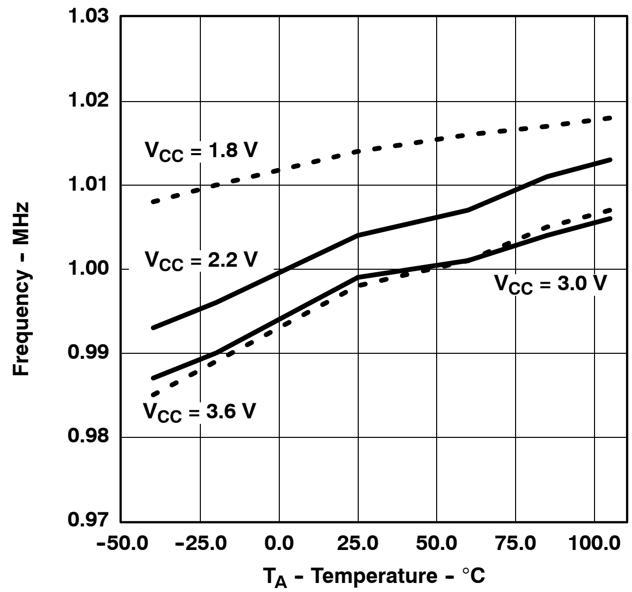


Figure 11. Calibrated 1-MHz Frequency vs Temperature

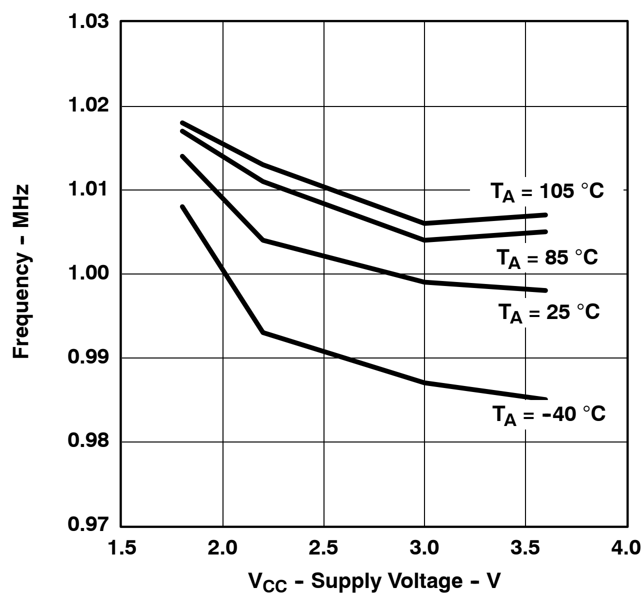


Figure 12. Calibrated 1-MHz Frequency vs V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

wake-up from lower power modes (LPM3/4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (see Note 1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V/3 V			2	μs
		BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ	2.2 V/3 V			1.5	
		BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ	2.2 V/3 V			1	
		BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (see Note 2)					$1/f_{MCLK} + t_{Clock,LPM3/4}$	

NOTES: 1. The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
2. Parameter applicable only if DCOCLK is used for MCLK.

typical characteristics – DCO clock wake-up time from LPM3/4

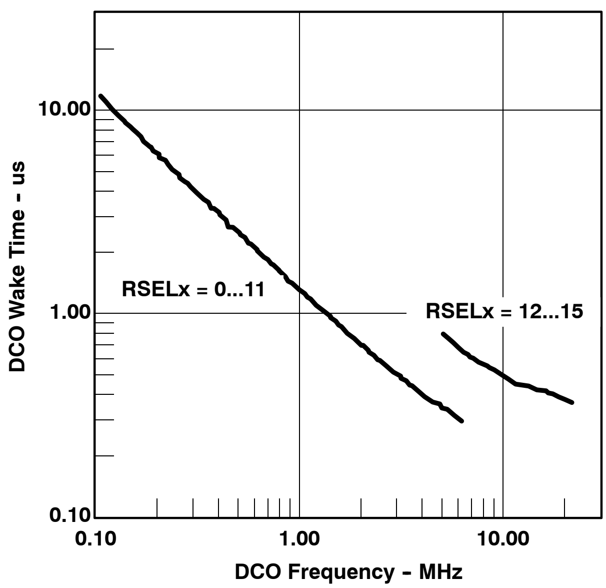


Figure 13. DCO wake-up time from LPM3 vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, low-frequency modes (see Note 4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V – 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3	1.8 V – 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation Allowance for LF crystals	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 12 pF			200		kΩ
$C_{L,eff}$	Integrated effective Load Capacitance, LF mode (see Note 1)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
Duty Cycle	LF mode	XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode (see Note 3)	XTS = 0, LFXT1Sx = 3 (see Notes 2)	2.2 V/3 V	10		10,000	Hz

NOTES:
1. Includes parasitic bond and package capacitance (approximately 2pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep as short of a trace as possible between the device and the crystal.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, high-frequency modes (see Note 5)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0	1.8 V – 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1	1.8 V – 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2	1.8 V – 3.6 V	2		10	MHz
			2.2 V – 3.6 V	2		12	MHz
			3.0 V – 3.6 V	2		16	MHz
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic level square wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3	1.8 V – 3.6 V	0.4		10	MHz
			2.2 V – 3.6 V	0.4		12	MHz
			3.0 V – 3.6 V	0.4		16	MHz
OA_{HF}	Oscillation Allowance for HF crystals (refer to Figure 14 and Figure 15)	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 0, LFXT1Sx = 1 $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		Ω
		XTS = 0, LFXT1Sx = 2 $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		Ω
$C_{L,eff}$	Integrated effective Load Capacitance, HF mode (see Note 1)	XTS = 1 (see Note 2)			1		pF
Duty Cycle	HF mode	XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V/3 V	40	50	60	%
		XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 16 MHz	2.2 V/3 V	40	50	60	%
$f_{Fault,HF}$	Oscillator fault frequency, HF mode (see Note 4)	XTS = 1, LFXT1Sx = 3 (see Notes 3)	2.2 V/3 V	30		300	kHz

NOTES:
1. Includes parasitic bond and package capacitance (approximately 2pF per pin).
   Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
3. Measured with logic level input frequency but also applies to operation with crystals.
4. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
5. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep as short of a trace as possible between the device and the crystal.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics − LFXT1 oscillator in HF mode (XTS = 1)

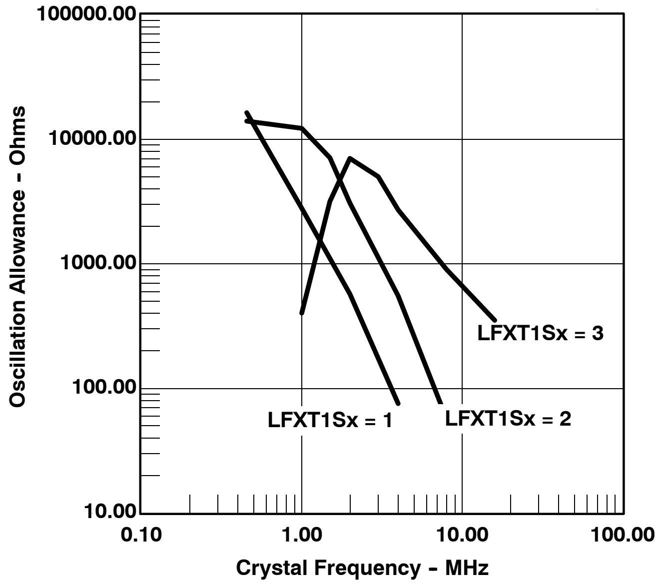


Figure 14. Oscillation Allowance vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

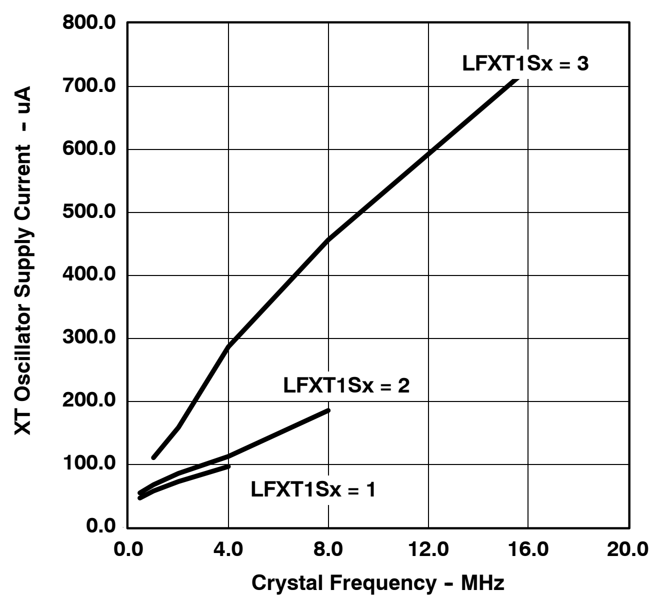


Figure 15. XT Oscillator Supply Current vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Timer_A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK; External: TACLK, INCLK; Duty Cycle = 50% ±10%	2.2 V			10	MHz
			3 V			16	
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1, TA2	2.2 V/3 V	20			ns

Comparator_A+ (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	2.2 V		25	40	μA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		30	50	μA
			3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON=1	2.2 V/3 V	0		V_{CC}−1	V
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5} V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	(see Figure 19 and Figure 20)	PCA0=1, CARSEL=1, CAREF=3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 2	2.2 V/3 V	−30		30	mV
V_{hys}	Input hysteresis	CAON=1	2.2 V/3 V	0	0.7	1.4	mV
$t_{(response)}$	Response time (low-high and high-low)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0 (see Note 3, Figure 16 and Figure 17)	2.2 V	80	165	300	ns
			3 V	70	120	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1 (see Note 3, Figure 16 and Figure 17)	2.2 V	1.4	1.9	2.8	μs
			3 V	0.9	1.5	2.2	

NOTES:
1. The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
3. Response time measured at P2.2/CAOUT.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

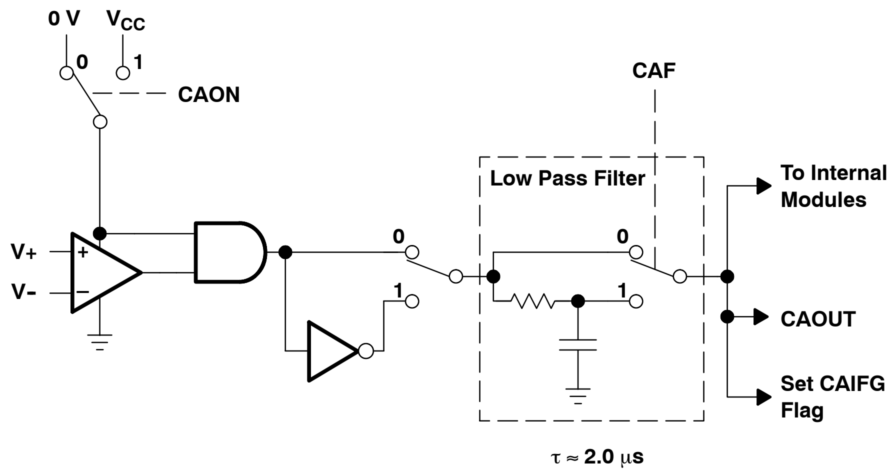


Figure 16. Block Diagram of Comparator_A+ Module

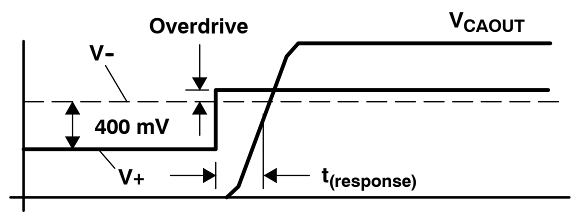


Figure 17. Overdrive Definition

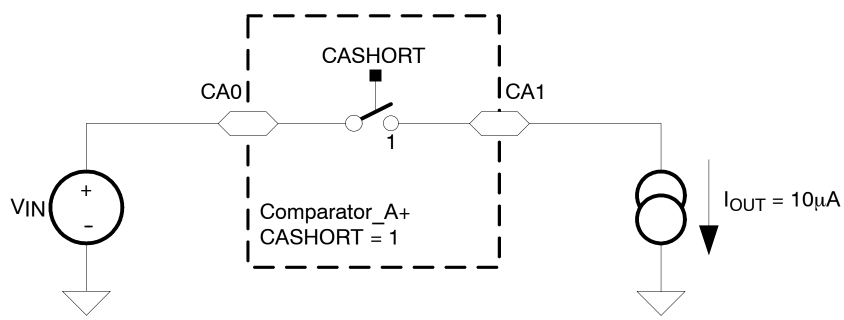


Figure 18. Comparator_A+ Short Resistance Test Condition

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – Comparator_A+

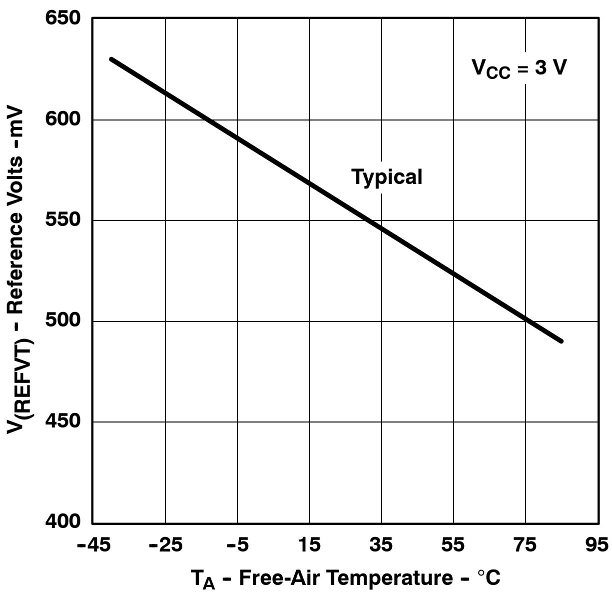


Figure 19. $V_{(RefVT)}$ **vs Temperature,** V_{CC} **= 3 V**

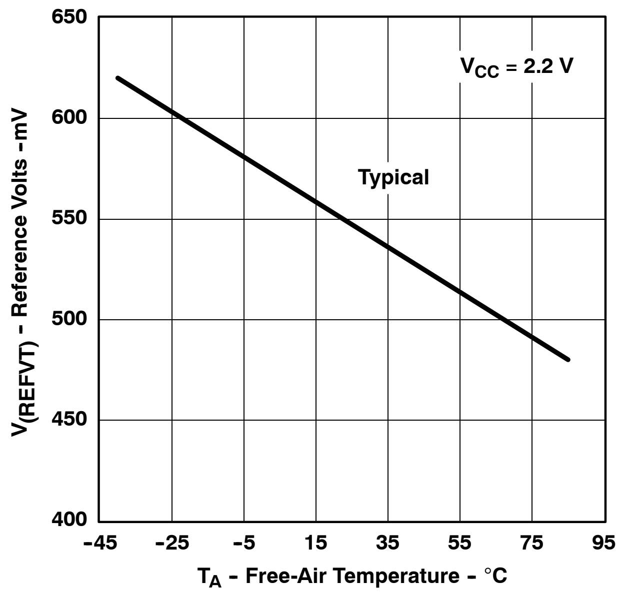


Figure 20. $V_{(RefVT)}$ **vs Temperature,** V_{CC} **= 2.2 V**

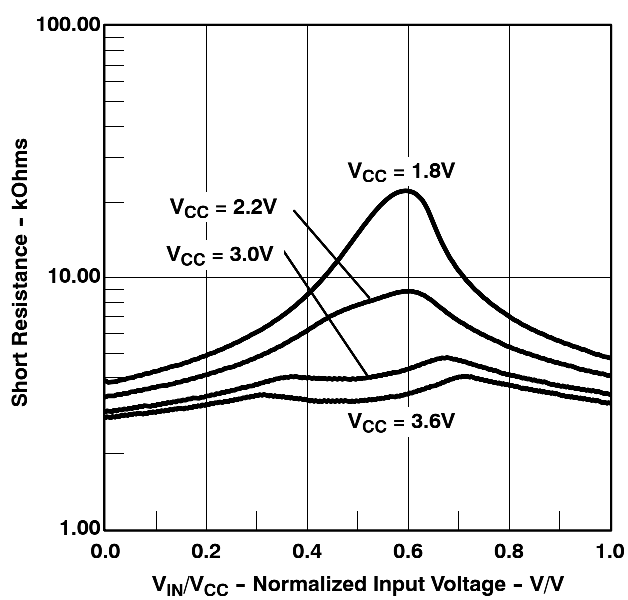


Figure 21. Short Resistance vs V_{IN}/V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.2		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		3	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		3	7	mA
t_{CPT}	Cumulative program time (see Note 1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 2			30		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				25		
$t_{Block, 1-63}$	Block program time for each additional byte or word				18		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				10593		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (see Note 1)	CPU halted	1.6			V

NOTE 1: This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-down resistance on TEST		2.2 V/3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.

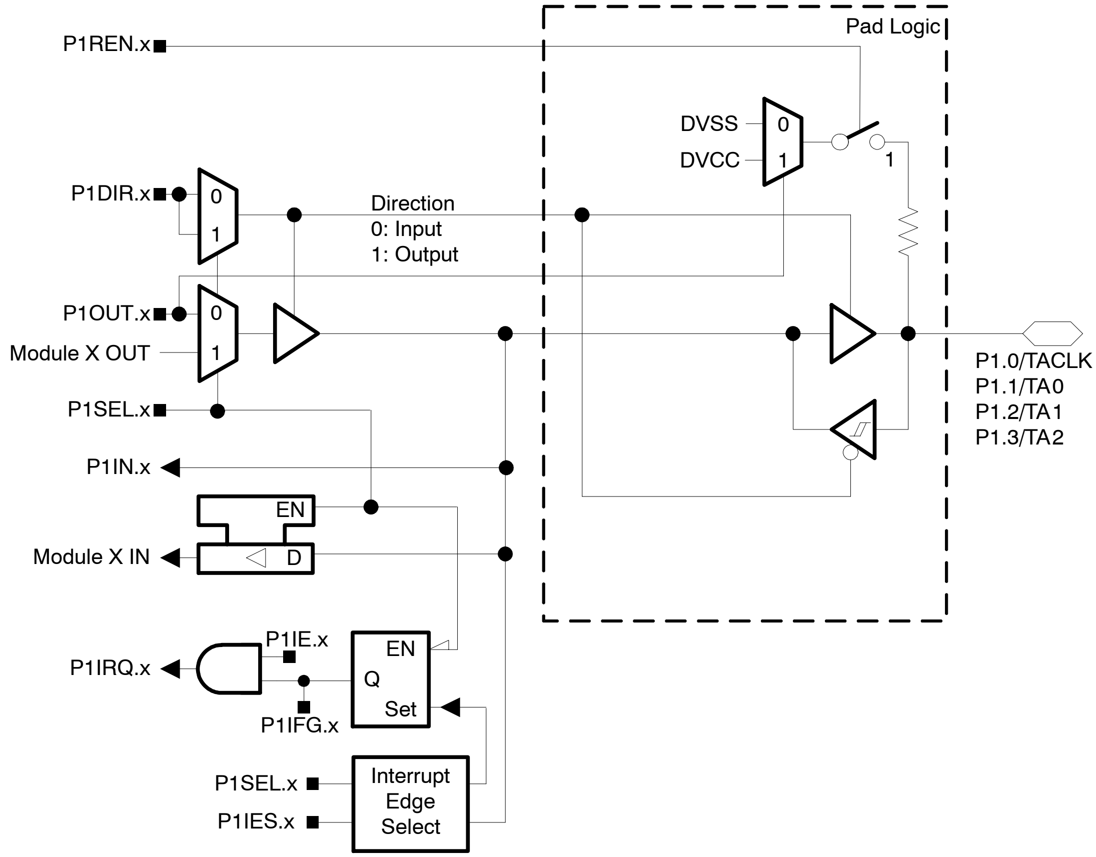
JTAG fuse (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TEST for fuse-blow	T_A = 25°C		6		7	V
I_{FB}	Supply current into TEST during fuse blow	T_A = 25°C				100	mA
t_{FB}	Time to blow fuse	T_A = 25°C				1	ms

NOTES: 1. Once the fuse is blown, no further access to the JTAG/Test and emulation feature is possible and is switched to bypass mode.

APPLICATION INFORMATION

Port P1 pin schematic: P1.0 to P1.3, input/output with Schmitt-trigger



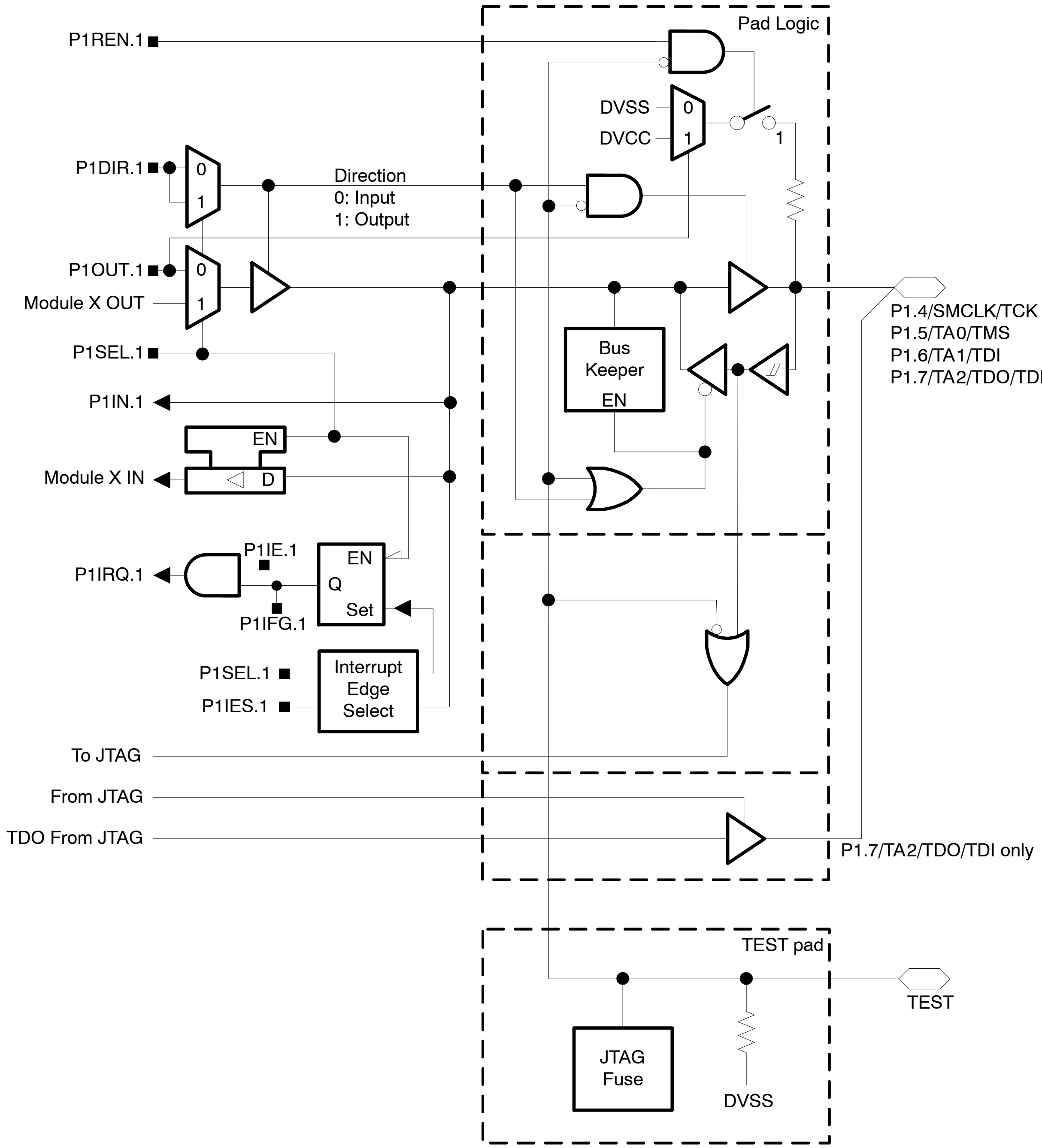
Port P1 (P1.0 to P1.3) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK	0	P1.0† (I/O)	I: 0; O: 1	0
		TACLK	0	1
		DV_{SS}	1	1
P1.1/TA0	1	P1.1† (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2† (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.3/TA2	3	P1.3† (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.

Port P1 pin schematic: P1.4 to P1.7, input/output with Schmitt-trigger and in-system access features



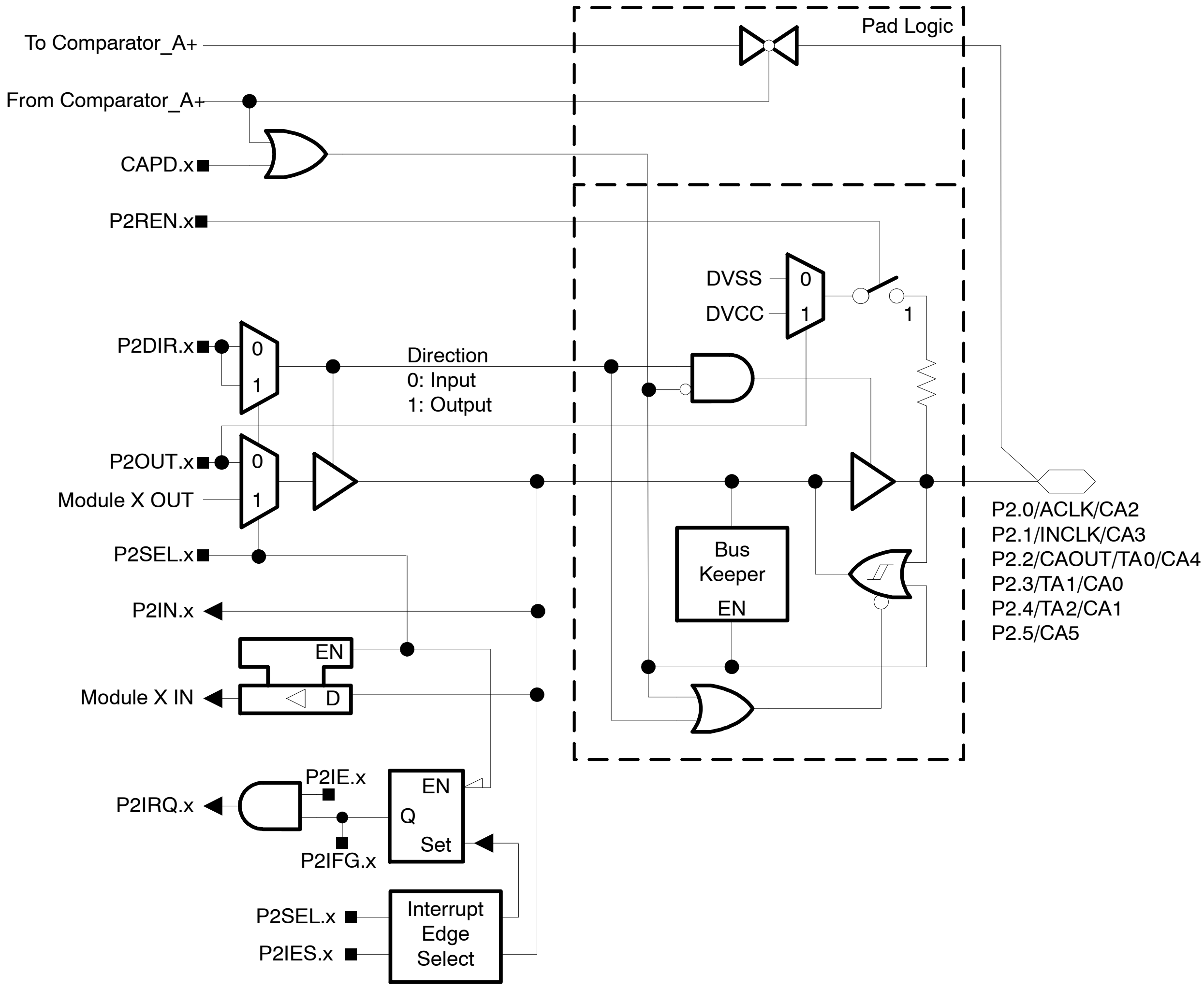
Port P1 (P1.4 to P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	TEST
P1.4/SMCLK/TCK	4	P1.4† (I/O)	I: 0; O: 1	0	0
		SMCLK	1	1	0
		TCK	X	X	1
P1.5/TA0/TMS	5	P1.5† (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA0	1	1	0
		TMS	X	X	1
P1.6/TA1/TDI/TCLK	6	P1.6† (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA1	1	1	0
		TDI/TCLK (see Note 3)	X	X	1
P1.7/TA2/TDO/TDI	7	P1.7† (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA2	1	1	0
		TDO/TDI (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.
3. Function controlled by JTAG.

Port P2 pin schematic: P2.0 to P2.5, input/output with Schmitt-trigger



Control Signal "From Comparator_A+"

PIN NAME	FUNCTION	SIGNAL "FROM COMPARATOR_A+" = 1					
		P2CA4	P2CA0		P2CA3	P2CA2	P2CA1
P2.0/ACLK/CA2	CA2	1	1	OR	0	1	0
P2.1/INCLK/CA3	CA3	N/A	N/A		0	1	1
P2.2/CAOUT/TA0/CA4	CA4	N/A	N/A		1	0	0
P2.3/TA1/CA0	CA0	0	1		N/A	N/A	N/A
P2.4/TA2/CA1	CA1	1	0		0	0	1
P2.5/CA5	CA5	N/A	N/A		1	0	1

NOTES: 1. N/A: Not available or not applicable.

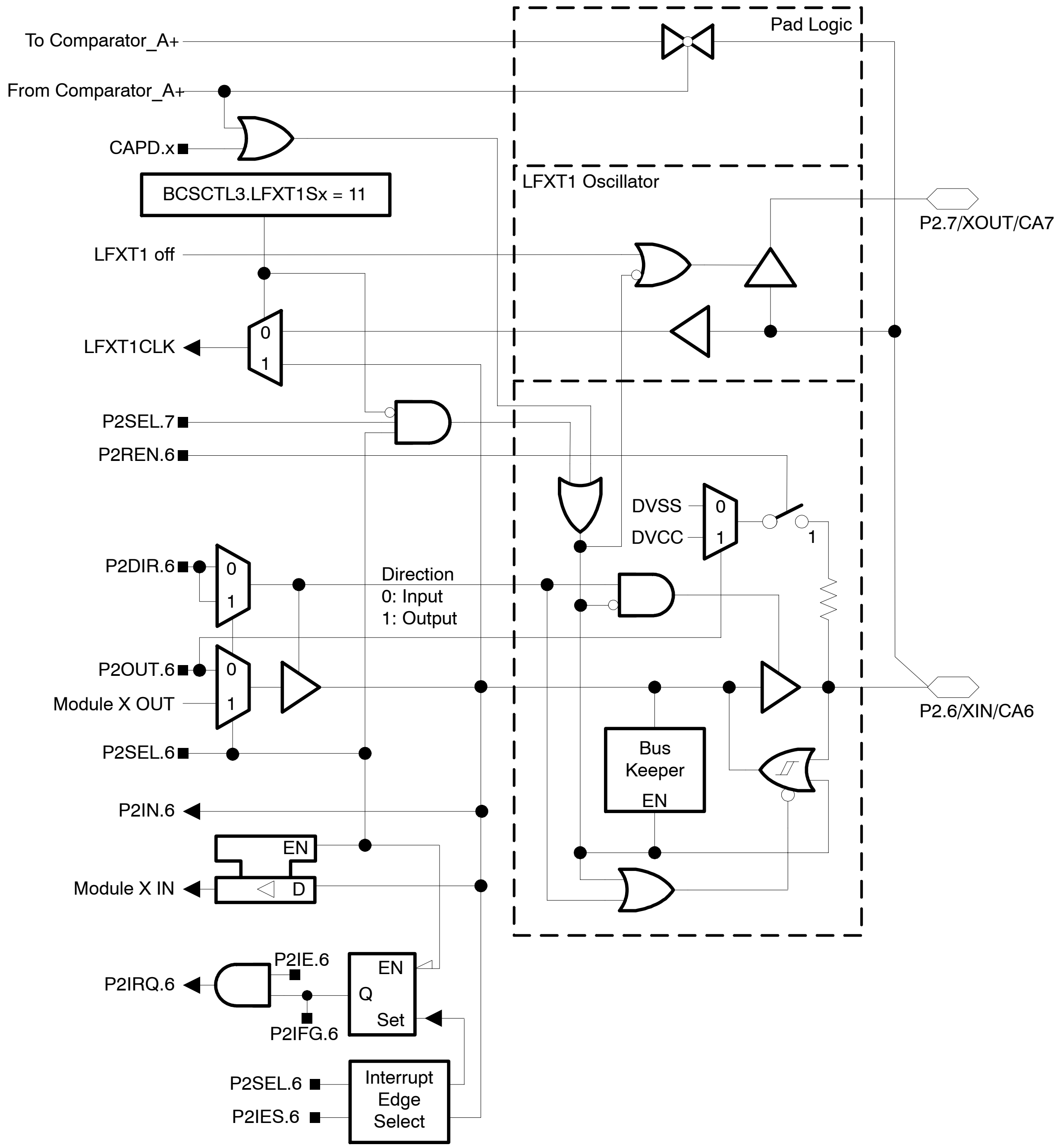
Port P2 (P2.0 to P2.5) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	CAPD.x
P2.0/ACLK/CA2	0	P2.0† (I/O)	I: 0; O: 1	0	0
		ACLK	1	1	0
		CA2 (see Note 3)	X	X	1
P2.1/INCLK/CA3	1	P2.1† (I/O)	I: 0; O: 1	0	0
		Timer_A3.INCLK	0	1	0
		DV_{SS}	1	1	0
		CA3 (see Note 3)	X	X	1
P2.2/CAOUT/TA0/CA4	2	P2.2† (I/O)	I: 0; O: 1	0	0
		Timer_A3.CCI0B	0	1	0
		CAOUT	1	1	0
		CA4 (see Note 3)	X	X	1
P2.3/TA1/CA0	3	P2.3† (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA1	1	1	0
		CA0 (see Note 3)	X	X	1
P2.4/TA2/CA1	4	P2.4† (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA2	1	1	0
		CA1 (see Note 3)	X	X	1
P2.5/CA5	5	P2.5† (I/O)	I: 0; O: 1	0	0
		CA5 (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the CAPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CAx input pin to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

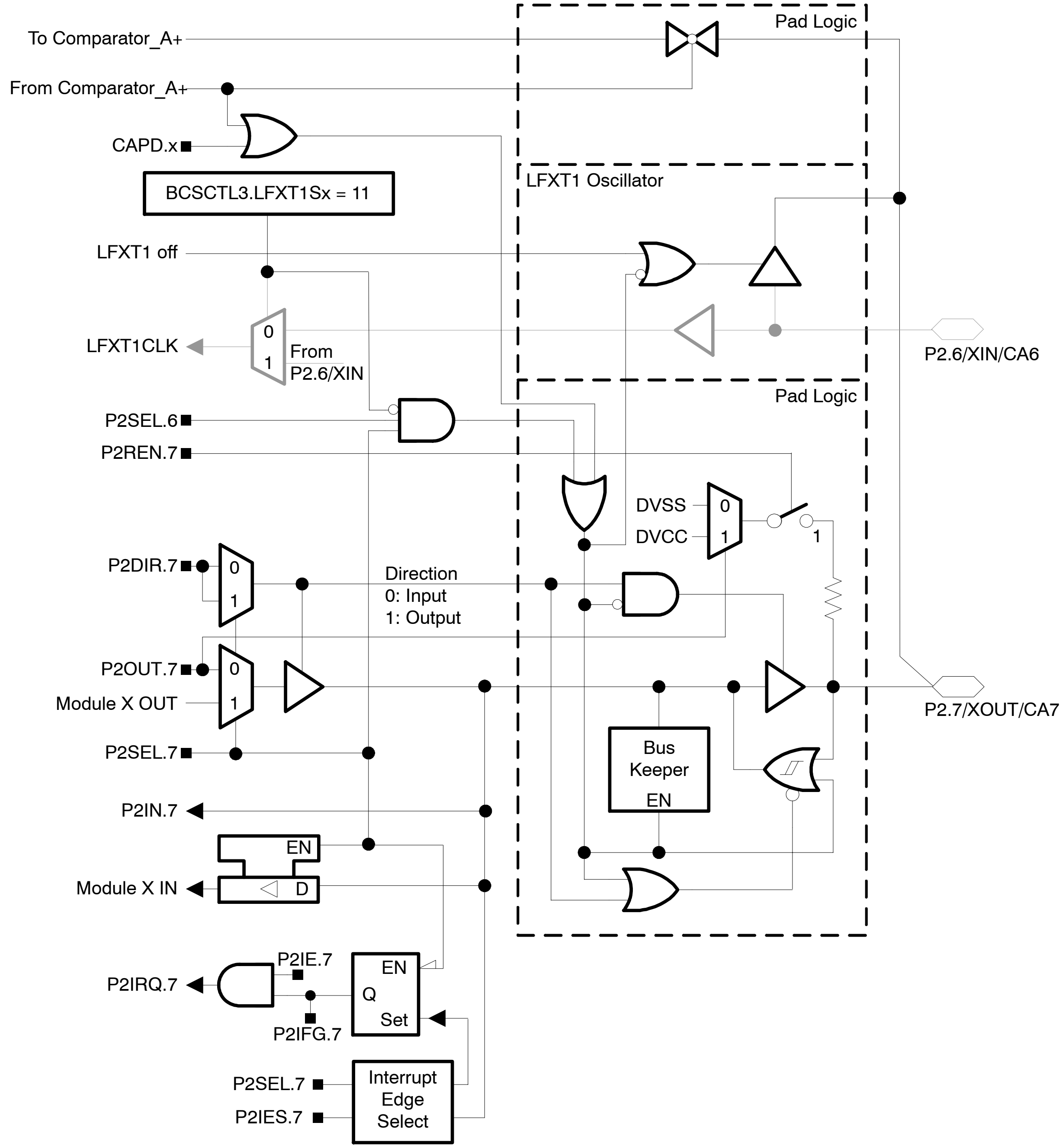
Port P2 pin schematic: P2.6, input/output with Schmitt-trigger and crystal oscillator input



Control signal “From Comparator_A+”

PIN NAME	FUNCTION	SIGNAL “FROM COMPARATOR_A+” = 1		
		P2CA3	P2CA2	P2CA1
P2.6/XIN/CA6	CA6	1	1	0

Port P2 pin schematic: P2.7, input/output with Schmitt-trigger and crystal oscillator output



Control signal "From Comparator_A+"

PIN NAME	FUNCTION	SIGNAL "FROM COMPARATOR_A+" = 1		
		P2CA3	P2CA2	P2CA1
P2.7/XOUT/CA7	CA7	1	1	1

Port P2 (P2.6) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	CAPD.x
P2.6/XIN/CA6	6	P2.6 (I/O)	I: 0; O: 1	0	0
		XIN†	X	1	0
		CA6 (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.
3. Setting the CAPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CAx input pin to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPDx bit.

Port P2 (P2.7) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	CAPD.x
P2.7/XOUT/CA7	6	P2.7 (I/O)	I: 0; O: 1	0	0
		XOUT† (see Note 4)	X	1	0
		CA7 (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.
3. Setting the CAPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CAx input pin to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.
4. If the pin XOUT/P2.7/CA7 is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

JTAG fuse check mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 22). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

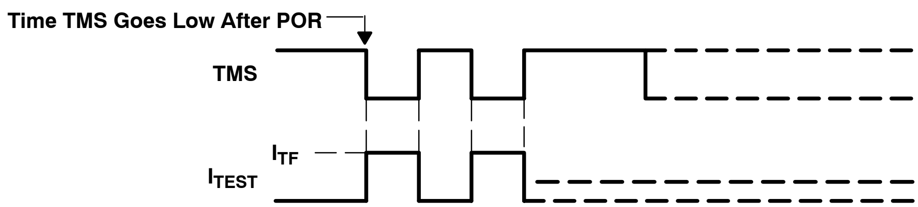


Figure 22. Fuse Check Mode Current, MSP430F21x1

NOTE:

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the *bootstrap loader* section for more information.

Data Sheet Revision History

LITERATURE NUMBER	SUMMARY
SLAS439	Preliminary PRODUCT PREVIEW data sheet release.
SLAS439A	MSP430x21x1 production data sheet release.
SLAS439B	Corrected instruction cycle time to 62.5ns, pg 1 Updated Figure 1. Operating Area, pg 12 Updated Figures 2 and 3, pg 13 R_{Pull} unit corrected from ”Ω” to ”kΩ”, pg 15 Max load current specification and Note 3 removed from ”outputs” table, pg 16 MIN and MAX percentages for ”calibrated DCO frequencies − tolerance over supply voltage VCC” corrected from 2.5% to 3% to match the specified frequency ranges., pg 22
SLAS439C	MSP430x21x1T production data sheet release. 105°C characterization results added.
SLAS439D	Corrected Timer_A2 to Timer_A3 and added TACCR2 to Interrupt Flag column in “interrupt vector addresses”, pg 6

NOTE: Page and figure numbers apply to the specified document revision and may differ in other revisions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP430F2101IDGV	ACTIVE	TVSOP	DGV	20	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2101IDGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2101IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2101IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2101IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2101IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2101IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2101IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2101TDGV	ACTIVE	TVSOP	DGV	20	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2101TDGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2101TDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2101TDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2101TPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2101TPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2101TRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2101TRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2111IDGV	ACTIVE	TVSOP	DGV	20	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2111IDGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2111IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2111IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2111IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2111IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2111IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2111IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2111TDGV	ACTIVE	TVSOP	DGV	20	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP430F2111TDGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2111TDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2111TDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2111TPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2111TPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2111TRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2111TRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2121IDGV	ACTIVE	TVSOP	DGV	20	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2121IDGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2121IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2121IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2121IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
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MSP430F2121TDGV	ACTIVE	TVSOP	DGV	20	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2121TDGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2121TDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2121TDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2121TPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2121TPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2121TRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2121TRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2131IDGV	ACTIVE	TVSOP	DGV	20	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2131IDGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2131IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP430F2131IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2131IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2131IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2131IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2131IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2131TDGV	ACTIVE	TVSOP	DGV	20	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2131TDGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2131TDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2131TDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2131TPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2131TPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MSP430F2131TRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2131TRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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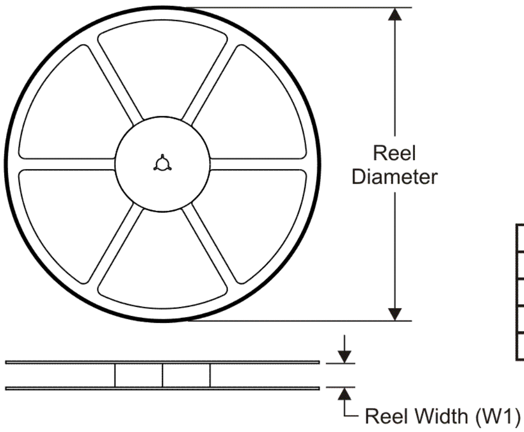
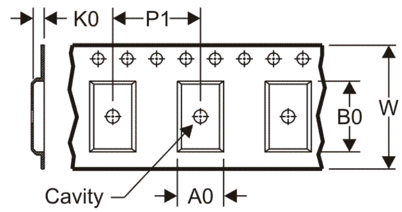
TAPE AND REEL INFORMATION

REEL DIMENSIONS

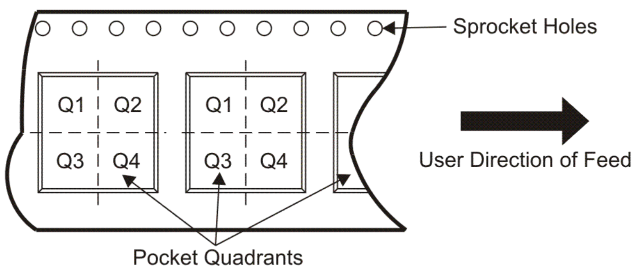


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

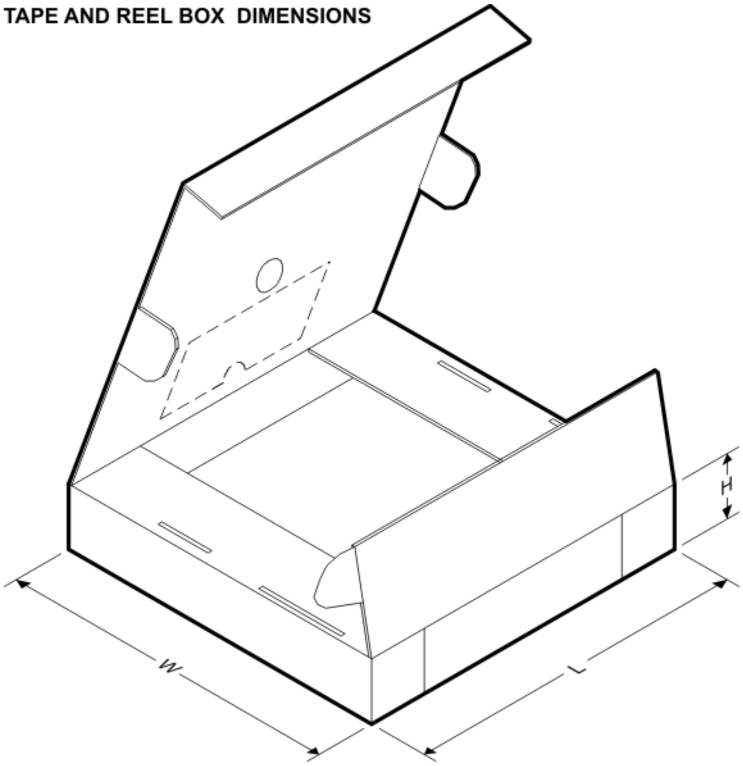


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2101IDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2101IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
MSP430F2101IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2101IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2101IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2101TDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2101TDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
MSP430F2101TPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2101TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2101TRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2111IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
MSP430F2111IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2111IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2111IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2111TDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2111TDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
MSP430F2111TPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2111TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2111TRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2121IDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2121IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
MSP430F2121IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2121IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2121IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2121TDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2121TDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
MSP430F2121TPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2121TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2121TRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2131IDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2131IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
MSP430F2131IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2131IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2131IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2131TDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F2131TDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
MSP430F2131TPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F2131TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F2131TRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

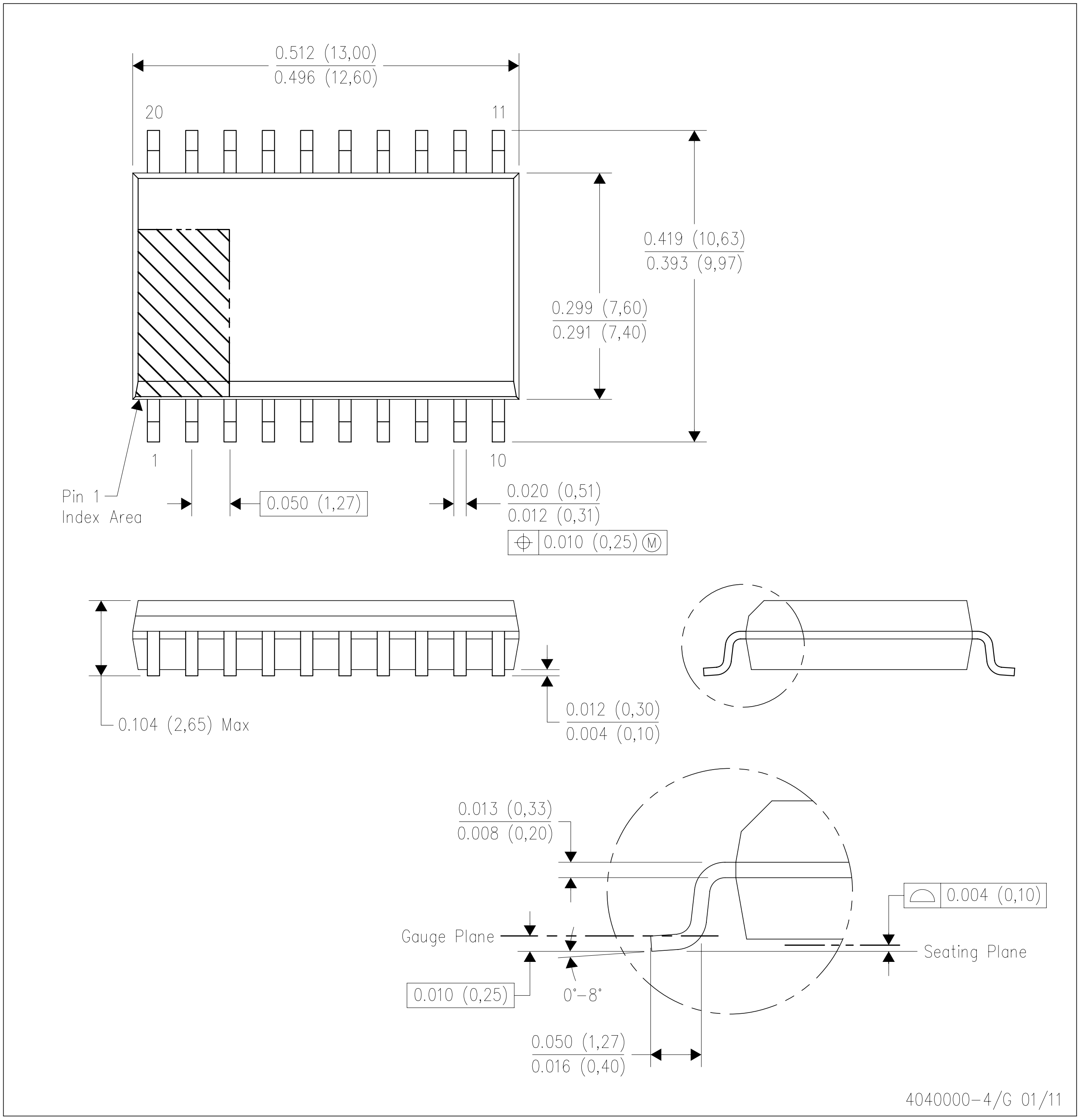


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2101IDGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
MSP430F2101IDWR	SOIC	DW	20	2000	346.0	346.0	41.0
MSP430F2101IPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
MSP430F2101IRGER	VQFN	RGE	24	3000	346.0	346.0	29.0
MSP430F2101IRGET	VQFN	RGE	24	250	190.5	212.7	31.8
MSP430F2101TDGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
MSP430F2101TDWR	SOIC	DW	20	2000	346.0	346.0	41.0
MSP430F2101TPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
MSP430F2101TRGER	VQFN	RGE	24	3000	346.0	346.0	29.0
MSP430F2101TRGET	VQFN	RGE	24	250	190.5	212.7	31.8
MSP430F2111IDWR	SOIC	DW	20	2000	346.0	346.0	41.0
MSP430F2111IPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
MSP430F2111IRGER	VQFN	RGE	24	3000	346.0	346.0	29.0
MSP430F2111IRGET	VQFN	RGE	24	250	190.5	212.7	31.8
MSP430F2111TDGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
MSP430F2111TDWR	SOIC	DW	20	2000	346.0	346.0	41.0
MSP430F2111TPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
MSP430F2111TRGER	VQFN	RGE	24	3000	346.0	346.0	29.0
MSP430F2111TRGET	VQFN	RGE	24	250	190.5	212.7	31.8
MSP430F2121IDGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0

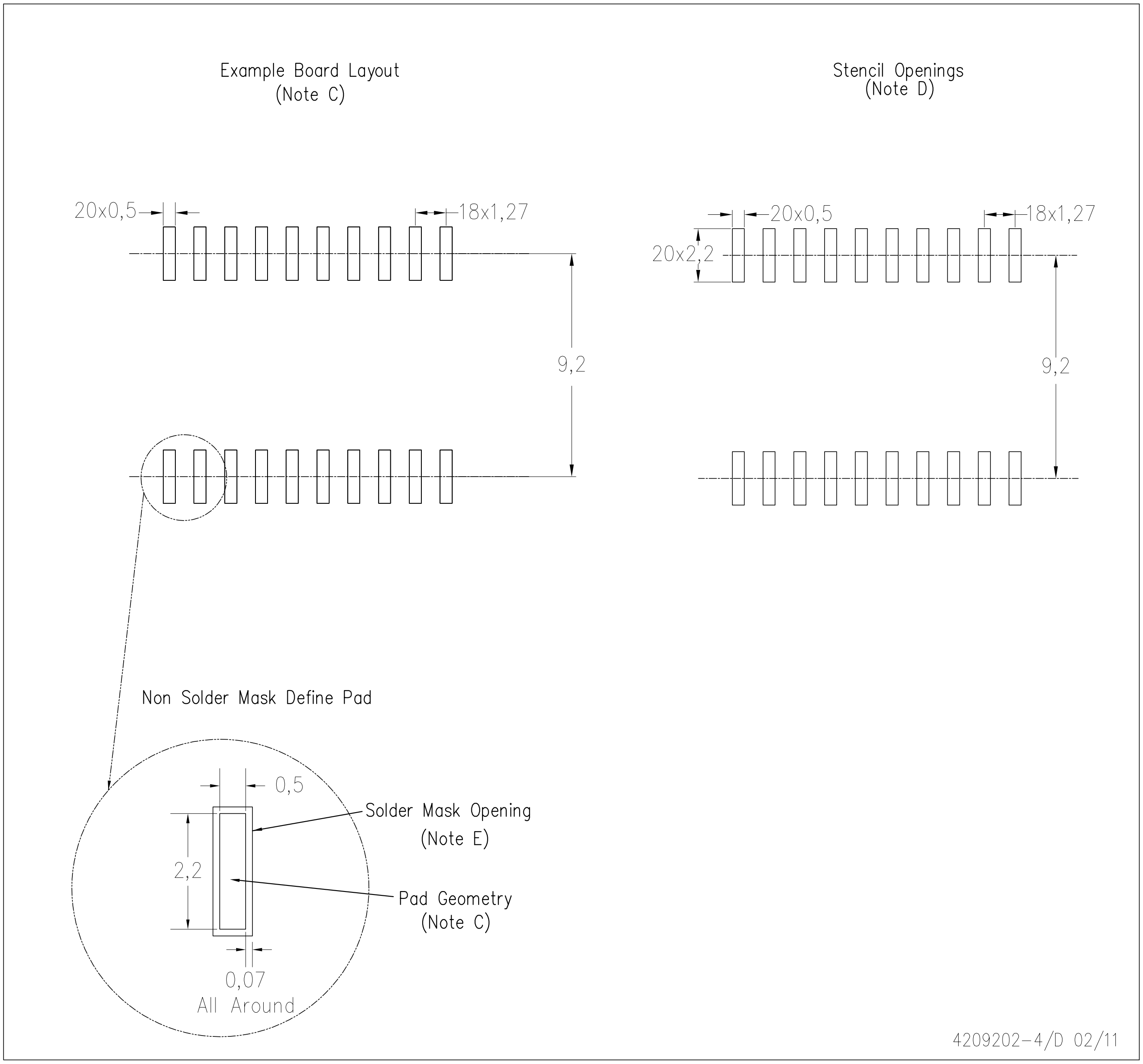
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2121IDWR	SOIC	DW	20	2000	346.0	346.0	41.0
MSP430F2121IPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
MSP430F2121IRGER	VQFN	RGE	24	3000	346.0	346.0	29.0
MSP430F2121IRGET	VQFN	RGE	24	250	190.5	212.7	31.8
MSP430F2121TDGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
MSP430F2121TDWR	SOIC	DW	20	2000	346.0	346.0	41.0
MSP430F2121TPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
MSP430F2121TRGER	VQFN	RGE	24	3000	346.0	346.0	29.0
MSP430F2121TRGET	VQFN	RGE	24	250	190.5	212.7	31.8
MSP430F2131IDGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
MSP430F2131IDWR	SOIC	DW	20	2000	346.0	346.0	41.0
MSP430F2131IPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
MSP430F2131IRGER	VQFN	RGE	24	3000	346.0	346.0	29.0
MSP430F2131IRGET	VQFN	RGE	24	250	190.5	212.7	31.8
MSP430F2131TDGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
MSP430F2131TDWR	SOIC	DW	20	2000	346.0	346.0	41.0
MSP430F2131TPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
MSP430F2131TRGER	VQFN	RGE	24	3000	346.0	346.0	29.0
MSP430F2131TRGET	VQFN	RGE	24	250	190.5	212.7	31.8

DW (R-PDSO-G20) PLASTIC SMALL OUTLINE



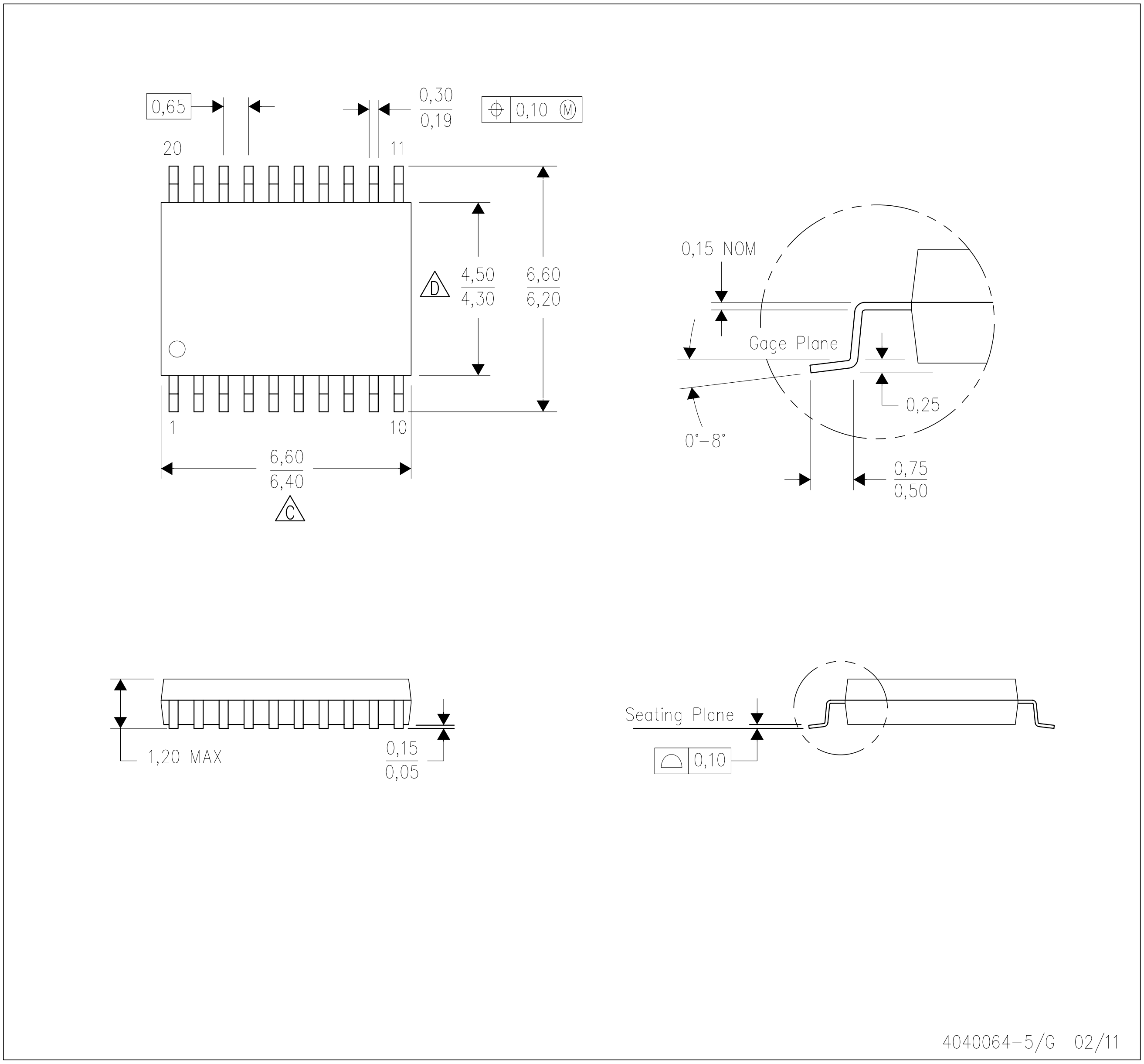
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20) PLASTIC SMALL OUTLINE



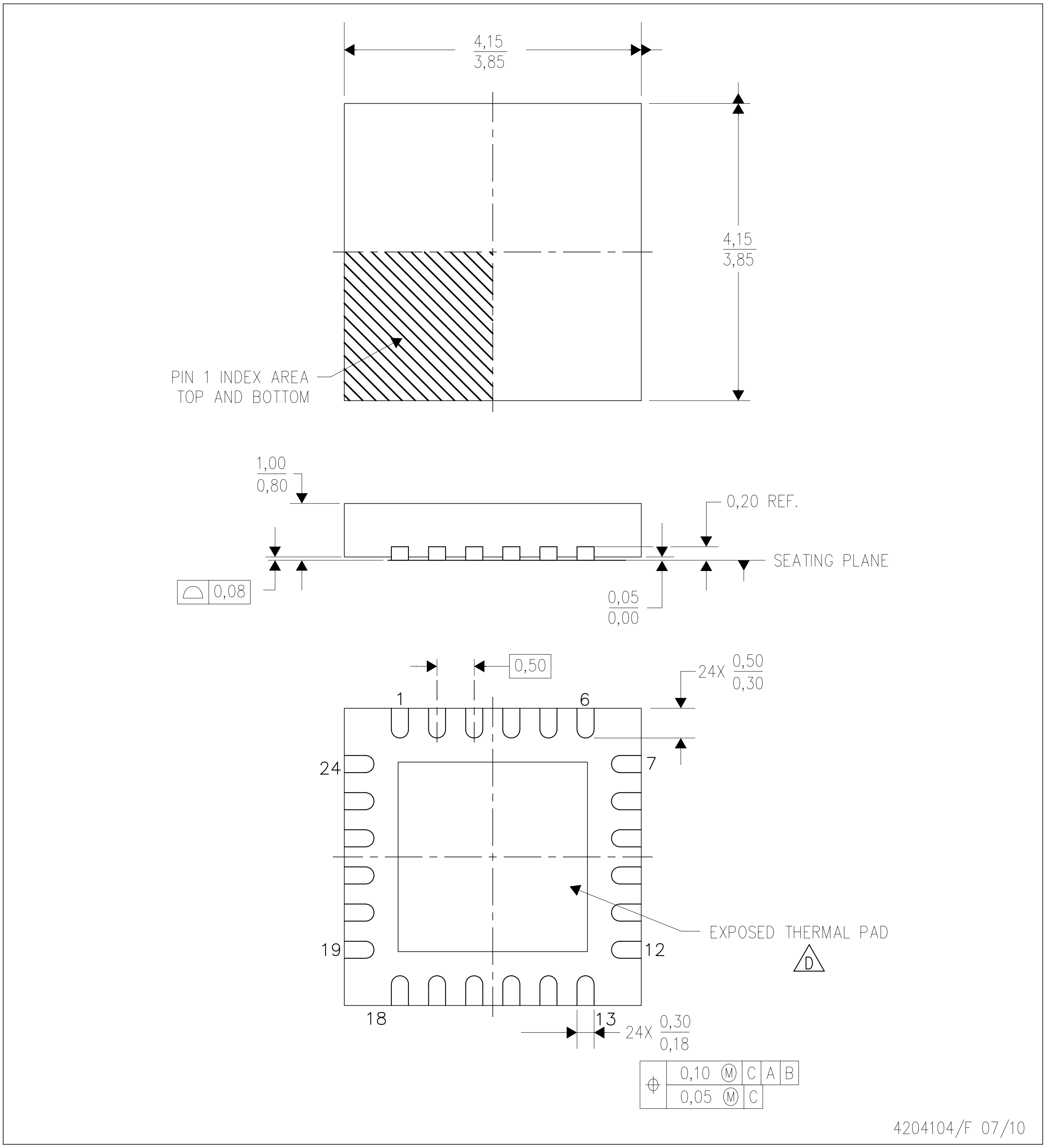
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–220.

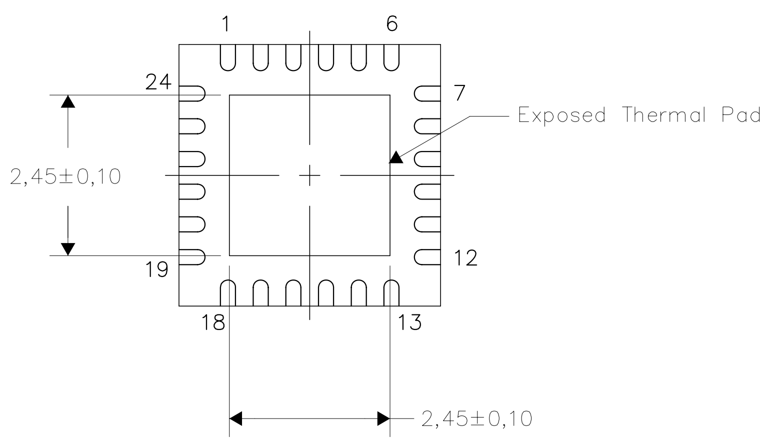
RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



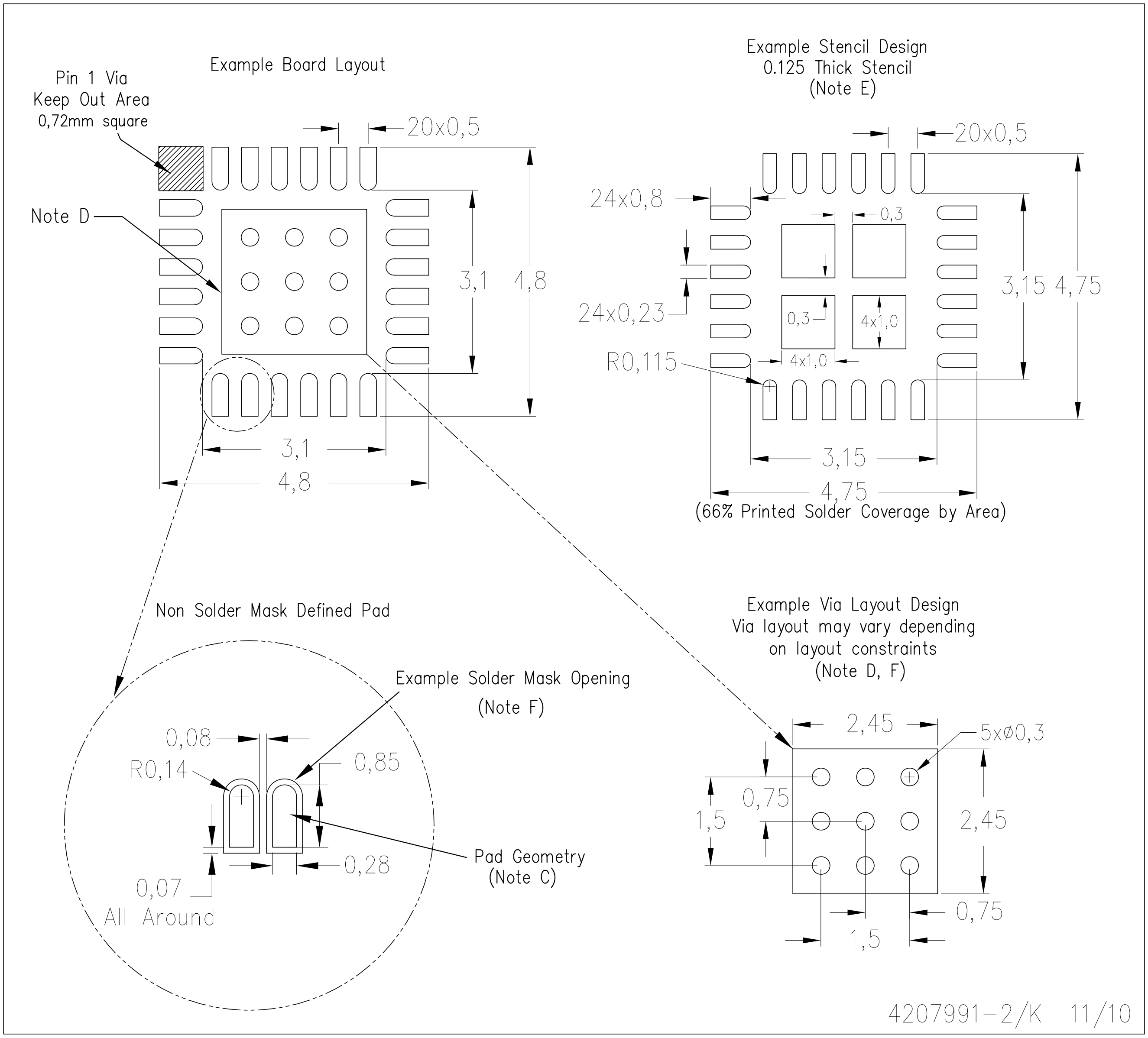
Bottom View

Exposed Thermal Pad Dimensions

4206344-3/W 01/11

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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