```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all;
3
4   ENTITY register_file_tb IS
5   END register_file_tb;
6
7   ARCHITECTURE register_file_tb_arch OF register_file_tb IS
8
9     TYPE EN_ARRAY  IS ARRAY (1 TO 10) OF STD_LOGIC;
10    TYPE REG_ARRAY IS ARRAY (1 TO 10) OF STD_LOGIC_VECTOR(2  DOWNTO 0);
11    TYPE DATAARRAY IS ARRAY (1 TO 10) OF STD_LOGIC_VECTOR(31 DOWNTO 0);
12
13    CONSTANT DELAY    :  time := 10 ns;
14
15    CONSTANT RR_IN    :  EN_ARRAY  := ('0',     '1',   '0',   '1',   '0',   '1',   '0',
      '0',   '0',   '0');
16    CONSTANT RW_IN    :  EN_ARRAY  := ('0',     '0',   '0',   '0',   '1',   '0',   '0',
      '0',   '0',   '0');
17    CONSTANT RS_IN    :  REG_ARRAY := ("001", "001", "010", "010", "000", "110", "000",
      "000", "000", "000");
18    CONSTANT RT_IN    :  REG_ARRAY := ("000", "111", "000", "101", "000", "110", "000",
      "000", "000", "000");
19    CONSTANT RD_IN    :  REG_ARRAY := ("000", "000", "000", "110", "110", "000", "000",
      "000", "000", "000");
20
21    CONSTANT WR_IN    :  DATAARRAY := ("00000000000000000000000000000000",
      "00000000000000000000000000000000",
22                                       "00000000000000000000000000000000",
                                         "00000000000000000000000000000000",
23                                       "11111111111111111111111111111111",
                                         "00000000000000000000000000000000",
24                                       "00000000000000000000000000000000",
                                         "00000000000000000000000000000000",
25                                       "00000000000000000000000000000000",
                                         "00000000000000000000000000000000");
26
27    CONSTANT D1_OUT   :  DATAARRAY := ("00000000000000000000000000000000",
      "00000000000000000000000000000000",
28                                        "00000000000000000000000000000000",
                                          "00000000000000000000000000000000",
29                                        "00000000000000000000000000000000",
                                          "00000000000000000000000000000000",
30                                        "00000000000000000000000000000000",
                                          "00000000000000000000000000000000",
31                                        "00000000000000000000000000000000",
                                          "00000000000000000000000000000000");
32
33    CONSTANT D2_OUT   :  DATAARRAY := ("00000000000000000000000000000000",
      "00000000000000000000000000000000",
34                                        "00000000000000000000000000000000",
                                          "00000000000000000000000000000000",
35                                        "00000000000000000000000000000000",
                                          "00000000000000000000000000000000",
36                                        "00000000000000000000000000000000",
                                          "00000000000000000000000000000000",
37                                        "00000000000000000000000000000000",
                                          "00000000000000000000000000000000");
38
39
40
41
42    SIGNAL RegRead    :  STD_LOGIC := '0';
43    SIGNAL RegWrite   :  STD_LOGIC := '0';
44    SIGNAL RegS       :  std_logic_vector (2  downto 0) := "000";
45    SIGNAL RegT       :  std_logic_vector (2  downto 0) := "000";
46    SIGNAL RegD       :  std_logic_vector (2  downto 0) := "000";
47    SIGNAL WriteData  :  std_logic_vector (31 downto 0) :=
      "00000000000000000000000000000000";
48    SIGNAL ReadData1  :  std_logic_vector (31 downto 0) :=
```

```
    "00000000000000000000000000000000";
49  SIGNAL ReadData2  :  std_logic_vector (31 downto 0) :=
    "00000000000000000000000000000000";
50
51    COMPONENT Register_File
52      PORT (
53        RegRead   :  in STD_LOGIC ;
54        RegWrite  :  in STD_LOGIC ;
55        RegS      :  in std_logic_vector (2  downto 0);
56        RegT      :  in std_logic_vector (2  downto 0);
57        RegD      :  in std_logic_vector (2  downto 0);
58        WriteData :  in std_logic_vector (31 downto 0);
59        ReadData1 : out std_logic_vector (31 downto 0);
60        ReadData2 : out std_logic_vector (31 downto 0));
61    END COMPONENT;
62
63  BEGIN
64
65    TEST : PROCESS
66      variable i : integer := 1;
67      BEGIN
68        FOR i IN 1 TO 10 LOOP
69          RegRead   <= RR_IN(i);
70          RegWrite  <= Rw_IN(i);
71          RegS      <= RS_IN(i);
72          RegT      <= RT_IN(i);
73          RegD      <= RD_IN(i);
74          WriteData <= WR_IN(i);
75          wait for DELAY;
76        end loop;
77        wait;
78      end process TEST;
79
80  --  CHECK : PROCESS
81  --    variable i : integer := 1;
82  --    BEGIN
83  --      FOR i IN 1 TO 10 LOOP
84  --        RegRead   <= RR_IN(i);
85  --        RegWrite  <= Rw_IN(i);
86  --        RegS      <= RS_IN(i);
87  --        RegT      <= RT_IN(i);
88  --        RegD      <= RD_IN(i);
89  --        WriteData <= WR_IN(i);
90  --        wait for DELAY/2;
91  --      end loop;
92  --      wait;
93  --    end process CHECK;
94
95    DUT  : Register_File
96      PORT MAP (
97        RegRead   => RegRead,
98        RegWrite  => RegWrite,
99        RegS      => RegS,
100       RegT      => RegT,
101       RegD      => RegD,
102       WriteData => WriteData,
103       ReadData1 => ReadData1,
104       ReadData2 => ReadData2) ;
105
106 END register_file_tb_arch;
107
108
```