CMOS Static RAM 64K (8K x 8-Bit)

IDT7164S
IDT7164L

Features

- **High-speed address/chip select access time**
  - *Military: 20/25/35/45/55/70/85/100ns (max.)*
  - *Industrial: 20/25ns (max.)*
  - *Commercial: 20/25ns (max.)*
- **Low power consumption**
- **Battery backup operation – 2V data retention voltage (L Version only)**
- **Produced with advanced CMOS high-performance technology**
- **Inputs and outputs directly TTL-compatible**
- **Three-state outputs**
- **Available in 28-pin DIP, CERDIP and SOJ**
- **Military product compliant to MIL-STD-883, Class B**

Description

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

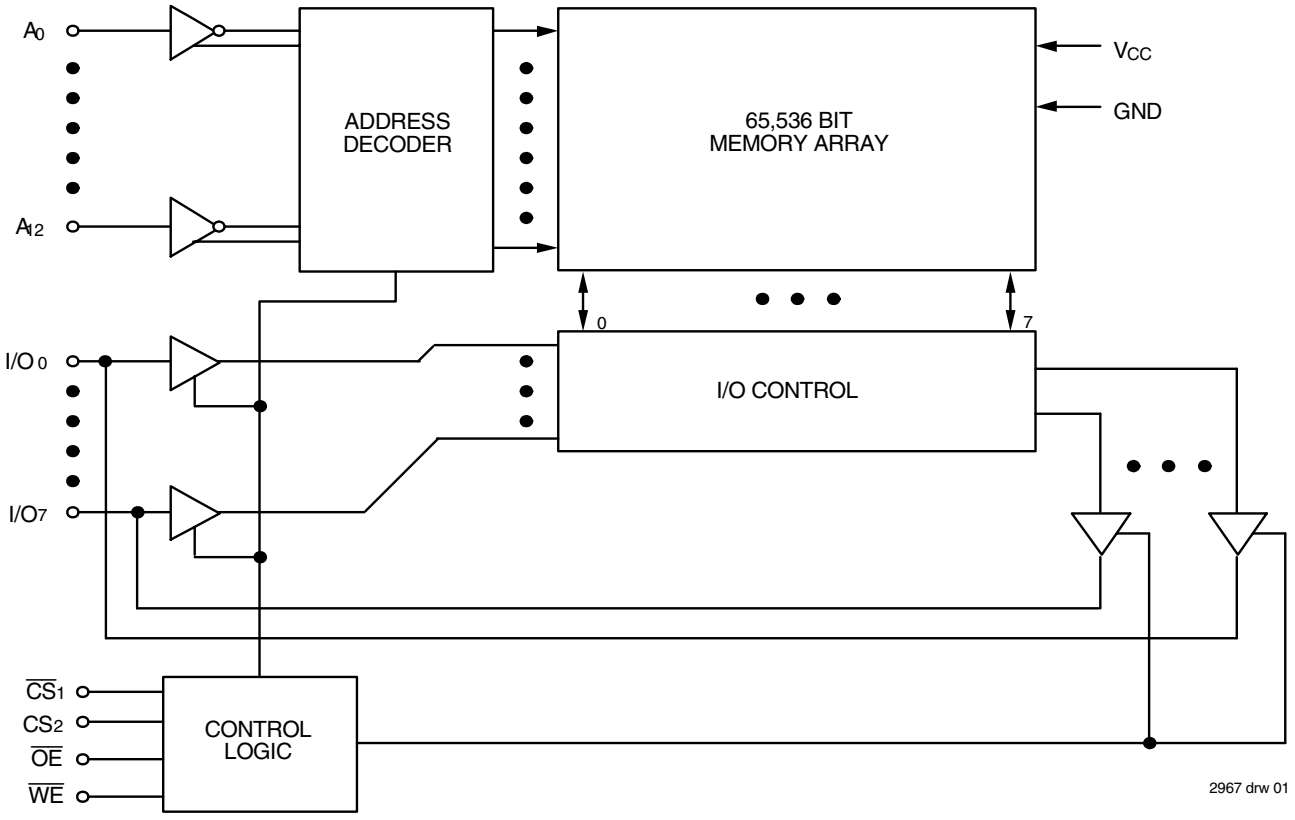
Address access times as fast as 20ns are available and the circuit offers a reduced power standby mode. When $\overline{CS}_1$ goes HIGH or CS_2 goes LOW, the circuit will automatically go to, and remain in, a low-power stand by mode. The low-power (L) version also offers a battery backup data retention capability at power supply levels as low as 2V.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin 300 mil DIP and SOJ and a 28-pin 600 mil CERDIP.

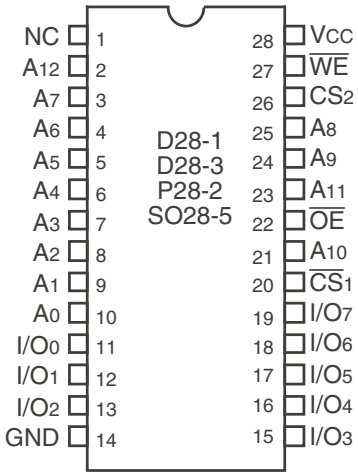
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Functional Block Diagram



APRIL 2011

Pin Configurations



2967 drw 02

DIP/SOJ
Top View

Absolute Maximum Ratings(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

2967 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

Pin Descriptions

Name	Description
A_0 - A_{12}	Address
I/O_0 - I/O_7	Data Input/Output
$\overline{CS_1}$	Chip Select
CS_2	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

2967 tbl 01

Truth Table(1,2,3)

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O	Function
X	H	X	X	High-Z	Deselected - Standby (I_{SB})
X	X	L	X	High-Z	Deselected - Standby (I_{SB})
X	V_{HC}	V_{HC} or V_{LC}	X	High-Z	Deselected - Standby (I_{SB1})
X	X	V_{LC}	X	High-Z	Deselected - Standby (I_{SB1})
H	L	H	H	High-Z	Output Disabled
H	L	H	L	$DATA_{OUT}$	Read Data
L	L	H	X	$DATA_{IN}$	Write Data

2967 tbl 03

NOTES:
1. CS_2 will power-down $\overline{CS_1}$, but $\overline{CS_1}$ will not power-down CS_2.
2. H = V_{IH}, L = V_{IL}, X = don't care.
3. V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input HIGH Voltage	2.2	—	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage	-0.5(1)	—	0.8	V

2967 tbl 05

NOTE:
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Industrial	-40°C to +85°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2967 tbl 04

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

2967 tbl 06

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

DC Electrical Characteristics[1] (V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7164S20 7164L20			7164S25 7164L25			Unit
			Com'l.	Ind.	Mil.	Com'l.	Ind.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open V_{CC} = Max., f = 0[2]	S	100	110	110	90	110	110	mA
		L	90	100	100	90	100	100	
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	170	170	180	170	170	180	mA
		L	150	150	160	150	150	160	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1} \geq V_{IH}$, $CS_2 \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	S	20	20	20	20	20	20	mA
		L	3	3	5	3	3	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[2], V_{CC} = Max. 1. $\overline{CS_1} \geq V_{HC}$ and $CS_2 \geq V_{HC}$, or 2. $CS_2 \leq V_{LC}$	S	15	15	20	15	15	20	mA
		L	0.2	0.2	1	0.2	0.2	1	

2967 tbl 07

Symbol	Parameter	Power	7164S35 7164L35	7164S45 7164L45	7164S55 7164L55	7164S70 7164L70	7164S85/100 7164L85/100	Unit
			Mil.	Mil.	Mil.	Mil.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open V_{CC} = Max., f = 0[2]	S	100	100	100	100	100	mA
		L	90	90	90	90	90	
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	160	160	160	160	160	mA
		L	140	130	125	120	120	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1} \geq V_{IH}$, $CS_2 \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	S	20	20	20	20	20	mA
		L	5	5	5	5	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[2], V_{CC} = Max. 1. $\overline{CS_1} \geq V_{HC}$ and $CS_2 \geq V_{HC}$, or 2. $CS_2 \leq V_{LC}$	S	20	20	20	20	20	mA
		L	1	1	1	1	1	

2967 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		IDT7164S Min.	IDT7164S Max.	IDT7164L Min.	IDT7164L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L. & IND	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS_1}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L. & IND	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2967 tbl 09

Data Retention Characteristics Over All Temperature Ranges
(L Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0V	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	1. $\overline{CS_1} \geq V_{HC}$ $CS_2 \geq V_{HC}$, or 2. $CS_2 \leq V_{LC}$	MIL. COM'L. & IND	— —	10 10	15 15	200 60	300 90	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LL}\|$[3]	Input Leakage Current			—	—	—	2	2	µA

2967 tbl 10

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2967 tbl 11

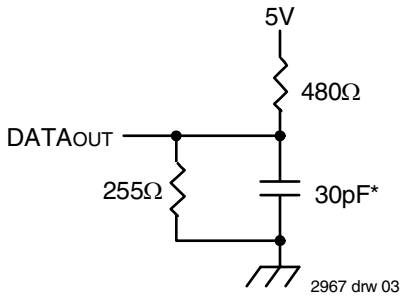


Figure 1. AC Test Load

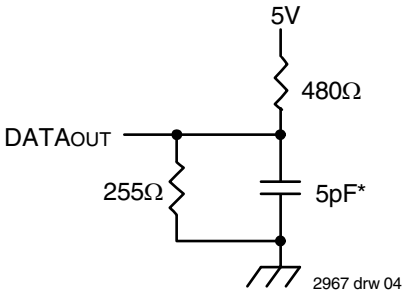


Figure 2. AC Test Load
(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Includes scope and jig capacitances

AC Electrical Characteristics (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S20 7164L20		7164S25 7164L25		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	20	—	25	—	ns
t_{AA}	Address Access Time	—	19	—	25	ns
t_{ACS1}(1)	Chip Select-1 Access Time	—	20	—	25	ns
t_{ACS2}(1)	Chip Select-2 Access Time	—	25	—	30	ns
$t_{CLZ1,2}$(2)	Chip Select-1, 2 to Output in Low-Z	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	8	—	12	ns
t_{OLZ}(2)	Output Enable to Output in Low-Z	0	—	0	—	ns
$t_{CHZ1,2}$(2)	Chip Select-1,2 to Output in High-Z	—	9	—	13	ns
t_{OHZ}(2)	Output Disable to Output in High-Z	—	8	—	10	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	ns
t_{PU}(2)	Chip Select to Power Up Time	0	—	0	—	ns
t_{PD}(2)	Chip Deselect to Power Down Time	—	20	—	25	ns
Write Cycle						
t_{WC}	Write Cycle Time	20	—	25	—	ns
$t_{CW1,2}$	Chip Select to End-of-Write	15	—	18	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	18	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	21	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	ns
t_{WHZ}(2)	Write Enable to Output in High-Z	—	8	—	10	ns
t_{DW}	Data to Write Time Overlap	10	—	13	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	—	5	—	ns
t_{OW}(2)	Output Active from End-of-Write	4	—	4	—	ns

2967 tbl 12

NOTES:
1. Both chip selects must be active for the device to be selected.
2. This parameter is guaranteed by device characterization, but is not production tested.

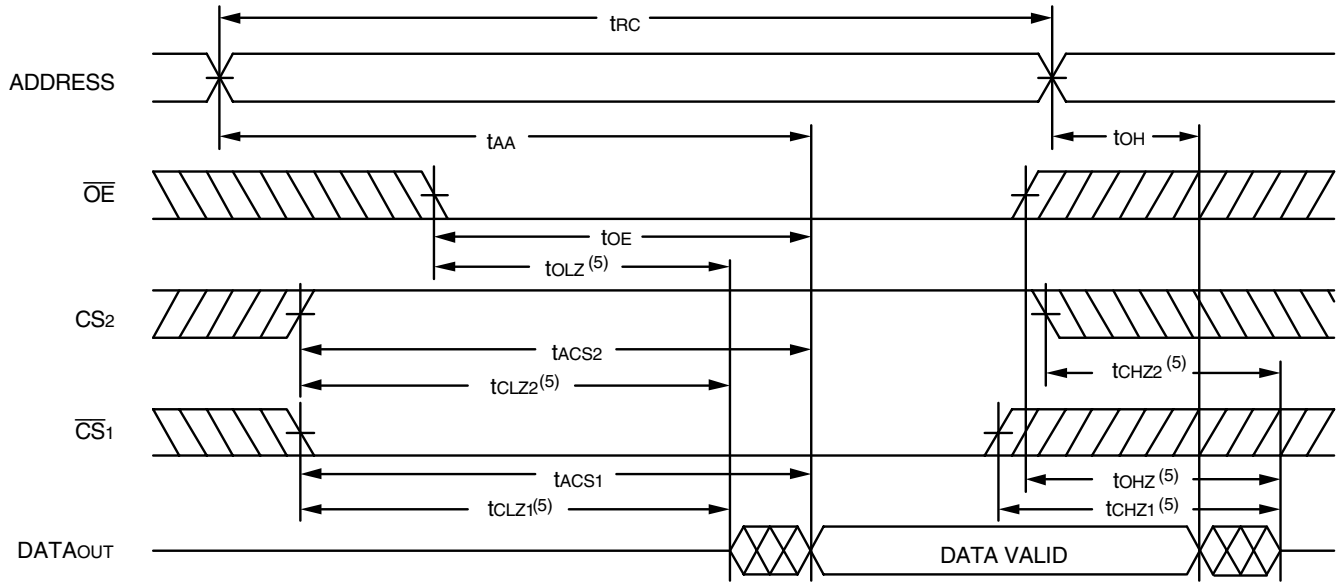
AC Electrical Characteristics (con't.) (Vcc = 5.0V ± 10%, Military Temperature Ranges)

Symbol	Parameter	7164S35 7164L35		7164S45 7164L45		7164S55 7164L55		7164S70 7164L70		7164S85/100 7164L85/100		Unit
		Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	35	—	45	—	55	—	70	—	85/100	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	70	—	85/100	ns
t_{ACS1}(1)	Chip Select-1 Access Time	—	35	—	45	—	55	—	70	—	85/100	ns
t_{ACS2}(1)	Chip Select-2 Access Time	—	40	—	45	—	55	—	70	—	85/100	ns
$t_{CLZ1,2}$(2)	Chip Select-1, 2 to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	18	—	25	—	30	—	35	—	40	ns
t_{OLZ}(2)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns
$t_{CHZ1,2}$(2)	Chip Select-1,2 to Output in High-Z	—	15	—	20	—	25	—	30	—	35	ns
t_{OHZ}(2)	Output Disable to Output in High-Z	—	15	—	20	—	25	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}(2)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(2)	Chip Deselect to Power Down Time	—	35	—	45	—	55	—	70	—	85/100	ns
Write Cycle												
t_{WC}	Write Cycle Time	35	—	45	—	55	—	70	—	85/100	—	ns
$t_{CW1,2}$	Chip Select to End-of-Write	25	—	33	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End-of-Write	25	—	33	—	50	—	60	—	75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	25	—	50	—	60	—	75	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	5	—	ns
t_{WHZ}(2)	Write Enable to Output in High-Z	—	14	—	18	—	25	—	30	—	35	ns
t_{DW}	Data to Write Time Overlap	15	—	20	—	25	—	30	—	35	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}(2)	Output Active from End-of-Write	4	—	4	—	4	—	4	—	4	—	ns

2967 tbl 13

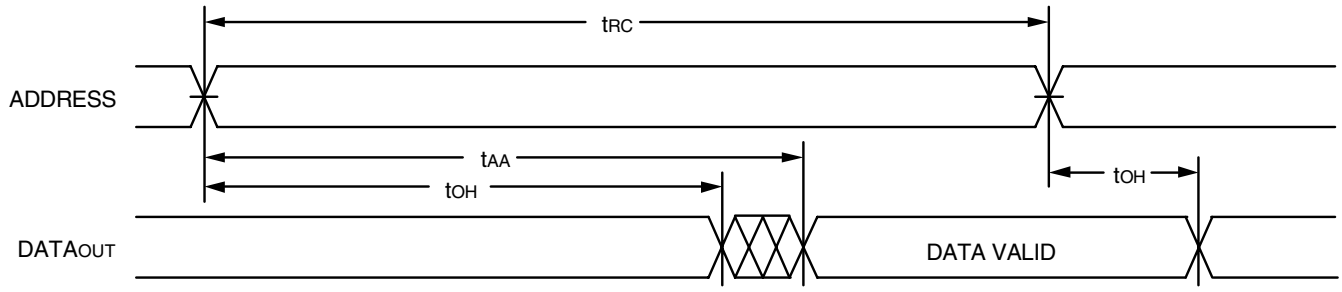
NOTES:
1. Both chip selects must be active for the device to be selected.
2. This parameter is guaranteed by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1(1)



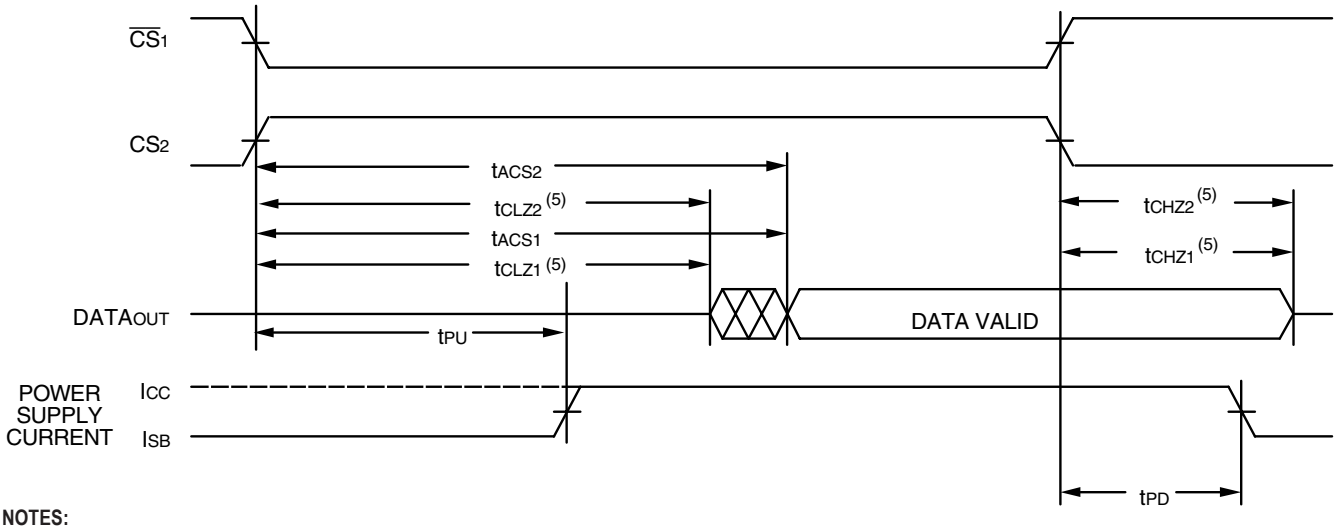
2967 drw 05

Timing Waveform of Read Cycle No. 2(1,2,4)



2967 drw 06

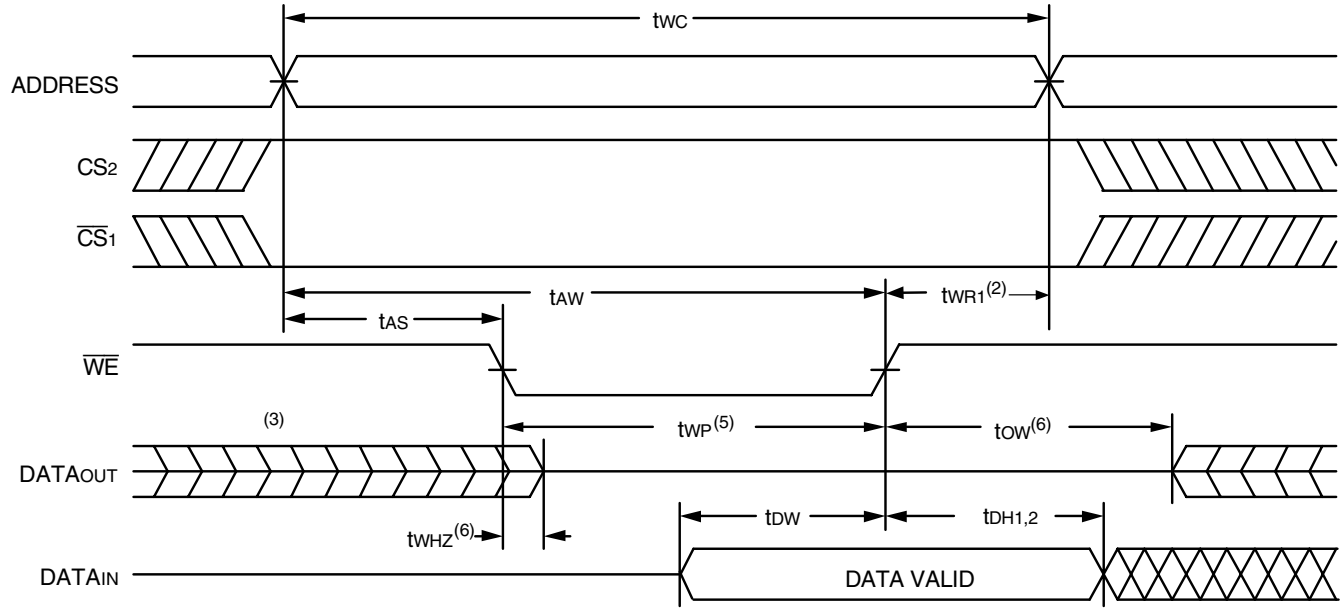
Timing Waveform of Read Cycle No. 3(1,3,4)



2967 drw 07

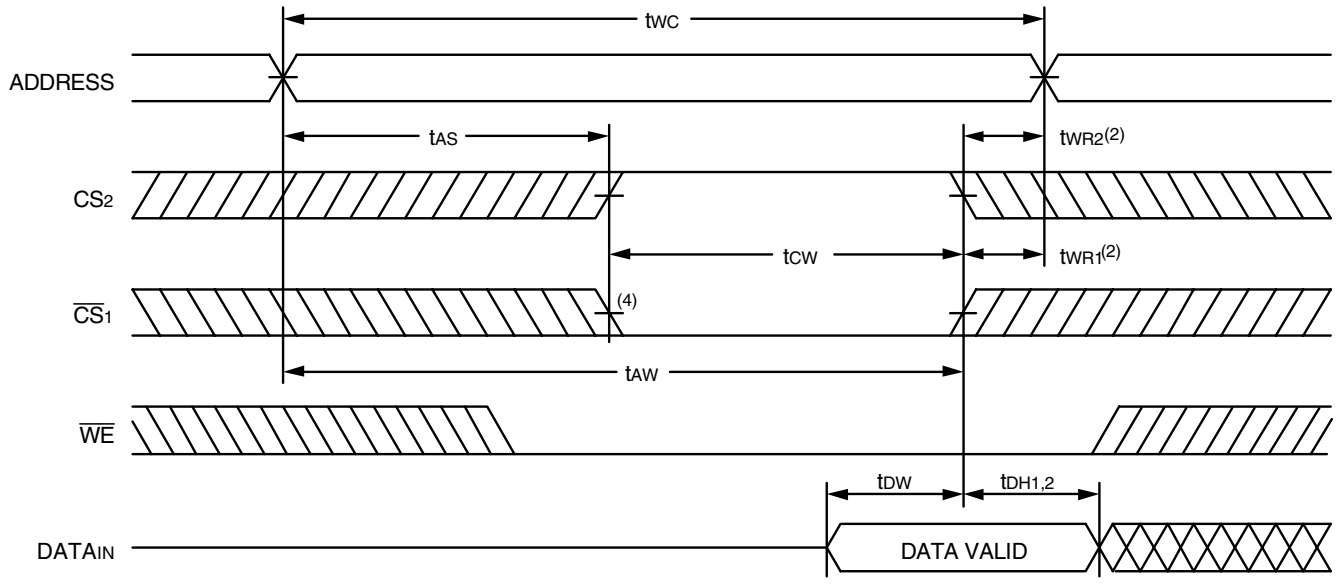
NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS_1}$ is LOW, CS_2 is HIGH.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition LOW and CS_2 transition HIGH.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,5)



2967 drw 08

Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1)

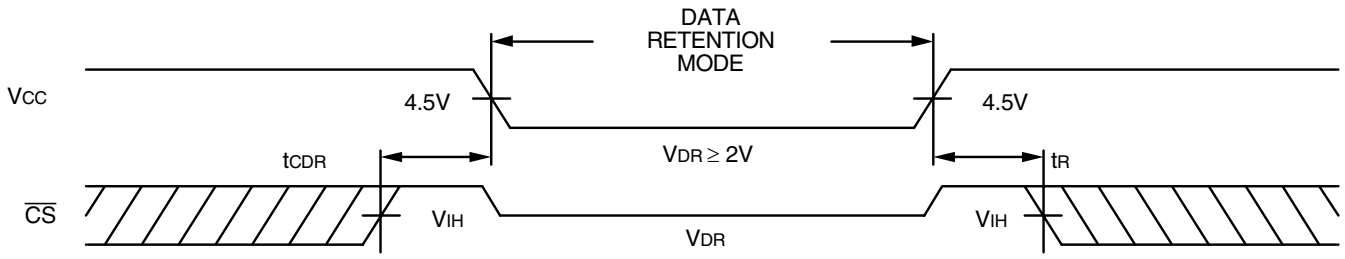


2967 drw 09

NOTES:

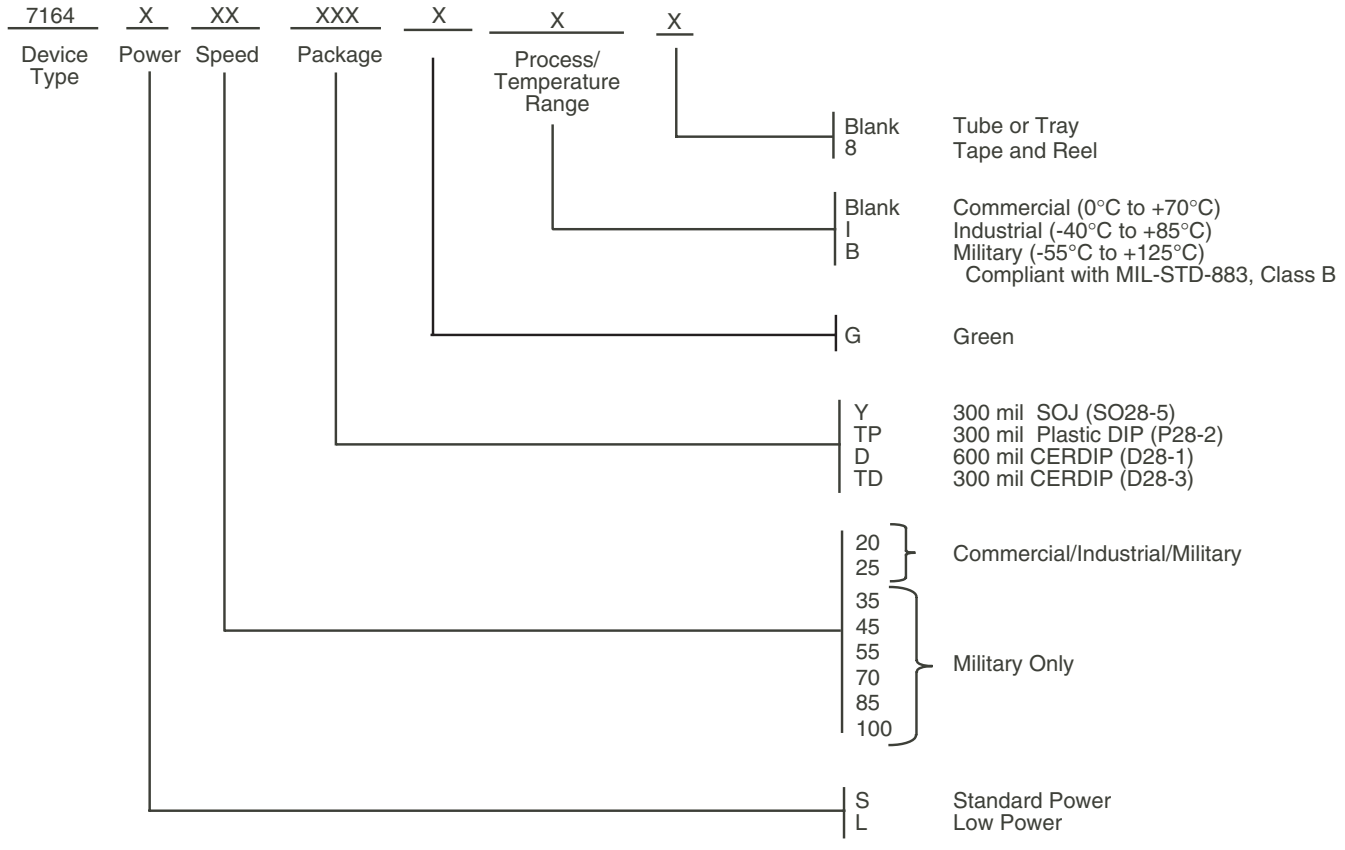
1. A write occurs during the overlap of a LOW $\overline{WE}$, a LOW $\overline{CS}_1$ and a HIGH CS_2.
2. $t_{WR1,\ 2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going HIGH or CS_2 going LOW to the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals must not be applied.
4. If the $\overline{CS}_1$ LOW transition or CS_2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} +t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified t_{WP}.
6. Transition is measured ±200mV from steady state.

Low Vcc Data Retention Waveform



2967 drw 10

Ordering Information



2967 drw 11

Datasheet Document History

01/13/00		Updated to new format
	Pp. 1, 2, 3, 5, 10	Added Industrial Temperature range offerings
	Pp. 1, 3, 9	Removed commercial 70ns speed grade offering
	Pp. 1, 3, 6, 10	Added 100ns speed grade specification details
	Pg. 3	Revised notes and footnotes in DC Electrical tables
	Pp. 5, 6	Revised notes and footnotes in AC Electrical tables
	Pg. 8	Removed Note 1 from Write Cycle No. 1 and No. 2 diagrams; renumbered notes and footnotes
	Pp. 9, 10	Separated Ordering Information into commercial, industrial, and military offerings
	Pg. 11	Added Datasheet Document History
08/09/00		Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"
12/07/01	Pg. 10	Add PJ28 to Industrial temperature.
09/30/04	Pg. 9,10	Added "restricted hazardous substance device" to ordering information.
11/16/06	Pg.3	Added inustrial temp power limits for 20ns part. Changed power limits for 25ns part for commercial and industrial. Changed power limits for commercial and industrial for 35ns part.
	Pg.10	Added 20ns part to ordering information. Refer to PCN SR-0602-01
02/20/07	Pg. 9, 10	Added L generation die step to data sheet ordering informatiom.
04/27/11	Pg. 1-3,5,6,9	Obsoleted 24-pin 600 mil, 15ns for Commercial and 35ns for Industrial & Commercial. Added Tape and Reel to Ordering information and updated description of Restricted hazardous substance device to Green.

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