

Improving Performance Estimation for **FPGA-based Accelerators for Convolutional Neural Networks**

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Outline

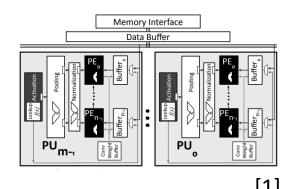


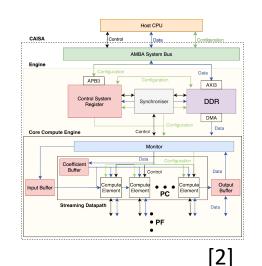
- Background Slides: X to Y
- Method Slides: X to Y
- Experiments Slides: X to Y
- Conclusion and Summary Slides: X to Y

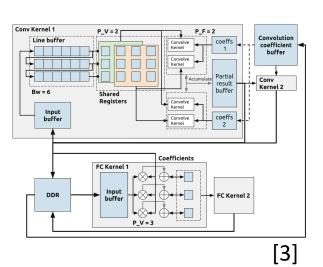
Background: Problem



FPGA-based multi CNN Accelerators







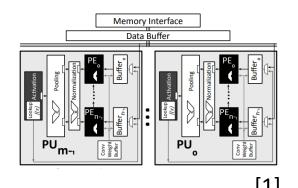
Design space exploration (DSE)

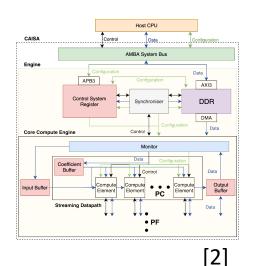
min/max Objective $SW, HW \ Variables$ $Hardware \ consumption(SW, HW \ variables) \leq Resources$ $Accelerator \ specific \ constraints$ $Network \ constraints$

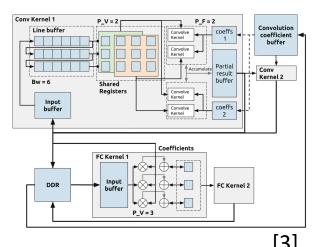
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FPGA-based multi CNN Accelerators







Design space exploration (DSE)

min/max Objective $SW, HW \ Variables$ $Hardware \ consumption(SW, HW \ variables) \leq Resources$ $Accelerator \ specific \ constraints$ $Network \ constraints$

Estimate the influence of attributes to save computational resources

Background: Challenges



Design space exploration (DSE)

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Estimate the influence of attributes to save computational resources

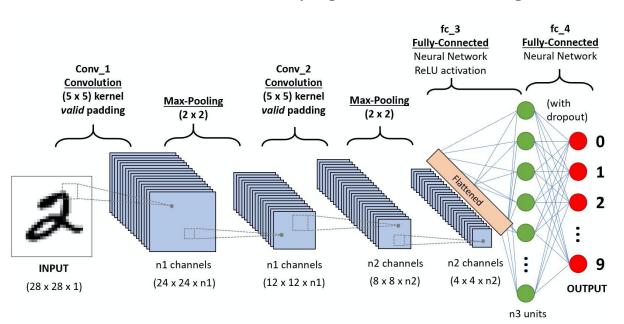
Challenges

- Scheduling which might be complicated if it supports
 Complicated operations
- I/O and Interruptions which might or might not be regular or irregular

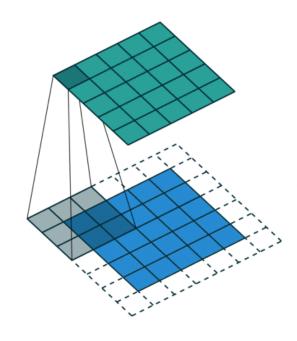
Background: Convolutional neural nets



LeNet-5 For classifying hand-written images



Building block: 2D Convolution



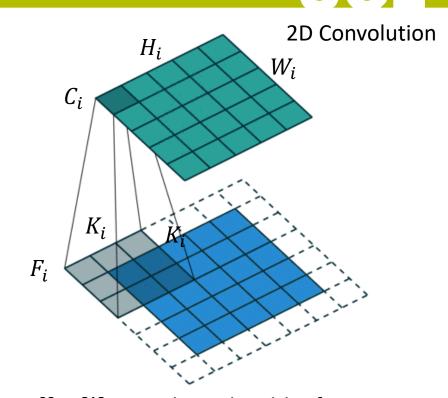
Background: Standard way - Convolution AUCL

$$T_{compute_i} = \frac{F_i \times C_i \times H_i \times W_i \times K_i \times K_i}{Clock \ cycle \ time}$$

$$T_{store_i} = \frac{H_{O_i} \times W_{O_i} \times F_i}{Memory\ bandwidth}$$

$$T_{load_i} = \frac{C_i \times H_i \times W_i}{Memory\ bandwidth}$$

$$T_{i} = \frac{\max(T_{compute_{i}}, T_{load_{i}}, T_{store_{i}})}{Parallelism}$$



 H_{O_i} , W_{O_i} Height and width of output github.com/martinferianc

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Background: Standard way



$$Latency = \sum_{i}^{N} T_{i}$$
 For each layer

$$T_{compute_i} = \frac{Number\ of\ operations}{Clock\ cycle\ time}$$

$$T_{load_i} = \frac{Input\ Size}{Memory\ bandwidth}$$

$$T_{store_i} = \frac{Output \, Size}{Memory \, bandwidth}$$

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Background: Standard way



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But it can act as a prior
 knowledge and a regulariser

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- Given that we have some **measurements** $X = \{x_1, x_2, x_3 ...\}$ For which we know the **features** such as the **software** Or **hardware parameters** such as: *Convolution parameters*, *Clock cycle time...*
- We have also recorded the objective such as **latency** as $Y = \{y_1, y_2, y_3 ...\}$
- We can then use the measurements and the standard way for estimation



- Gaussian process enables us to combine both
 - Measurements which give us a way to learn the estimation
 - Standard heuristic gives us a heuristic and a prior knowledge that can be followed to avoid overfitting

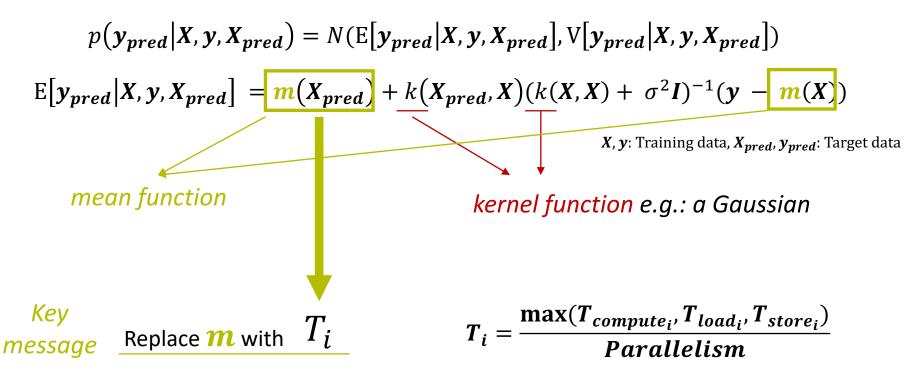


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$$p(y_{pred}|X, y, X_{pred}) = N(E[y_{pred}|X, y, X_{pred}], V[y_{pred}|X, y, X_{pred}])$$

$$E[y_{pred}|X, y, X_{pred}] = m(X_{pred}) + k(X_{pred}, X)(k(X, X) + \sigma^2 I)^{-1}(y - m(X))$$





Experiments: Our accelerator



$$T_{weights_{i}} = \frac{K_{i} \times K_{i} \times F_{i} \times C_{i}}{PF \times M_{CLK} \times S \times M_{EFF}} \qquad T_{compute_{i}} = \frac{F_{i} \times C_{i} \times H_{i} \times W_{i} \times K_{i} \times K_{i}}{PF \times PC \times L_{CLK}}$$

$$T_{data_{i}} = \frac{H_{i} \times W_{i} \times C_{i} \times DW}{PF \times M_{CLK} \times S \times M_{EFF}} \qquad T_{store_{i}} = \frac{H_{O_{i}} \times W_{O_{i}} \times F_{i} \times DW}{PF \times M_{CLK} \times S \times M_{EFF}}$$

$$T_{i} = \begin{cases} T_{i=1} = T_{load_{i}} + T_{compute_{i}} \\ T_{i \neq 1, i < N} = \max(T_{weights_{i}}, T_{compute_{i}}) \\ T_{i=N} = \max(T_{weights_{i}}, T_{compute_{i}}) + T_{store_{i}} \end{cases}$$

In total we had 15 features corresponding to software and hardware parameters

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Experiments: Results for latency



3 CNNs (ResNet, SSD, Yolo), quantised to 8-bits with PC, PF=64

	Heuristic	GP	GP and Standard	GP and ANN	LR	GTB	ANN	Intel Arria GX 1150
Leave-one- out cross- validation (LOO) [ms]	0.450	0.521	0.312	0.692	0.450	0.607	1.257	$\frac{0.312}{0.450}$
Training Time	None	$O(N^3)$	$O(N^3)$	-	$O(N^2)$	$O(N_{trees} * N * \log(N))$	-	31% lower error
Inference Time	1	$O(N^3)$	$O(N^3)$	$O(N^3 * L)$	<i>O(P)</i>	$O(P * \log(P))$	O(P * L)	

N stands for the number of training points, P for the number of input features, in this case 15, L stands for a complexity of hidden layers in a neural network. - stands for a variable complexity which depends on the architecture of artificial neural network as well as the optimiser method.

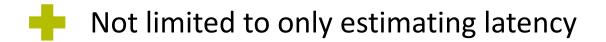
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Conclusion



	GP and Standard				
LOO [ms]	0.312				
Training Time	$O(N^3)$				
Inference Time	$O(N^3)$				



Reuses previously developed knowledge

Works if the data is scarce (152 samples)

Scalability if large dataset, should not have a lot evaluations

Future work



Multiple objectives: Energy, throughput

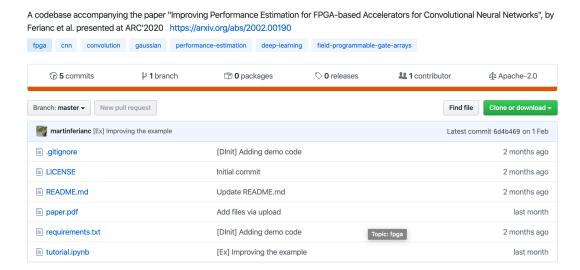
Multiple functions: 3D Convolution or other arch.

Co-design of accelerator and neural network
 Architecture through neural architecture search

Summary







QR Code for an online tutorial

https://github.com/martinferianc/Improving
Per Esti for FPGA-based Acc for CNNsARC2020

References



[1] Njikam, A. N. S. and Zhao, H. (2016). A novel activation function for multilayer feed-forward neural networks. In *Applied Intelligence*, volume 45, pages 75–82, New York, NY, USA. Springer.

[2] Corerain Technologies Ltd. (2019). Rainman accelerator. https://bit.ly/2H5jFO0.

[3] Zhao, R., Niu, X., Wu, Y., Luk, W., and Liu, Q. (2017a). Optimizing CNN-based object detection algorithms on embedded FPGA platforms. In *Proceedings of 2017 International Symposium on Applied Reconfigurable Computing*, pages 255–267, Belfast, UK. Springer.