

## ASSIGNMENT 4:

*The assignment is aimed at verifying understanding of cache-coherence protocols and interconnect networks. Please consult the lecture notes:*

*L6-Memory-Hierarchy-Coherence and L7-Interconnect.*

Request Type	Time to carry out protocol action	Traffic
Read hit	1 cycle	N/A
Write hit	1 cycle	N/A
Read request serviced by next level	40 cycles	6 bytes + B
Read-exclusive request serviced by next level	40 cycles	6 bytes + B
Bus Upgrade/update request	10 cycles	10 bytes

**Task 1)** Assume that a shared-memory multiprocessor with a number of processor/private cache units connected by a shared single(atomic)-transaction bus. Our baseline cache-coherence protocol is an MSI protocol, but we want to investigate what performance gains can be achieved by using an exclusive state to make it an MESI protocol. The time to carry out various protocol actions is listed in the above table: for example, while a read and write hit takes only 1 cycle, a read request takes 40 cycles as it has to bring the block from the next level of the cache hierarchy. A bus upgrade request takes less time as it does not involve a block transfer but rather invalidates other shared copies.

We write  $R_i/B$  and  $W_i/B$  to denote a read and write operation, respectively, by processor/cache unit  $i$  to block  $B$ . Assuming block  $X$  is not in any of the private caches of processors 1 to 4, we want to determine the time it takes to execute the following sequence of accesses:

$R1/X, W1/X, W1/X, R2/X, W2/X, W2/X, R3/X, W3/X, W3/X, R4/X, W4/X, W4/X$

**Task 1.a)** Assume that a transaction from state E to state M brings no access cost. How many cycles does it take to execute the access sequence under MSI vs. MESI?

**Task 1.b)** Compare the traffic generated by the MSI and MESI protocols counted in bytes transferred using the table above, and assuming that the size of a memory block  $B$  is 32 bytes.

**Task 2)** Assume that a shared-memory multiprocessor with a number of processor/private cache units connected by a shared single(atomic)-transaction bus. Our baseline cache-coherence protocol is an MESI protocol, but we want to investigate what performance gains can be achieved by adding migratory sharing detection/optimization to it. We want to determine the time and traffic under the execution of a sequence of accesses with a MESI with and without migratory sharing detection/optimization by using the parameters in the above table.

Assume that the migratory sharing is disabled in the beginning, and is automatically enabled immediately after, but excluding, the first (read serviced by a remote node in modified state, write) pair of consecutive accesses to the same memory block by the same processor/cache. Consider the following sequence of accesses by the processors, and assume that migratory sharing (initially processor 1 does not have a copy of X in its cache):

R1/X, W1/X, R2/X, W2/X, R3/X, W3/X, R4/X, W4/X

**Task 2.a)** How many cycles does it take to execute the access sequence under the MSI protocol with and without migratory detection/optimization, assuming the access costs for the protocol transactions in the table above?

**Task 2.b)** Compare the traffic generated by the MESI protocol with and without migratory detection/optimization assuming B = 32 bytes and the information in the table above.

Time	Processor 1	Processor 2	Processor 3
1	Read A		
2		Read B	
3			Read C
4	Write A		
5			Read D
6		Read B	
7	Write B		
8			Read C
9		Read B	

**Task 3)** Consider a shared-memory multiprocessor that consists of three processor/cache units and where cache coherence is maintained by an MSI protocol. The private caches are direct-mapped. The table above shows the access sequence taken by the three processors to four variables (A,B,C, and D), where A, B, and C belong to the same block and D belongs to a different block. The two blocks map to the same entry in the caches, and the cache is full initially and A, B, C, and D have not been accessed yet in the program.

**Task 3.a)** Classify the misses with respect to cold, replacement, true sharing, and false sharing misses.

**Task 3.b)** Which of the misses could be ignored and still guarantee that the execution is correct?

Request Type	Time to carry out protocol action	Traffic
Read hit	1 cycle	N/A
Write hit	1 cycle	N/A
BusRd	20 cycles	6 bytes
RemRd	20 cycles	6 bytes
RdAck	40 cycles	6 bytes
Flush	100 cycles	6 bytes + B
InvRq	20 cycles	6 bytes
InvAck	20 cycles	6 bytes
UpgrAck	20 cycles	6 bytes

**Task 4)** We consider a scalable implementation of a shared-memory multiprocessor using a set of nodes that each contain a processor, a private cache, and a portion of the memory. Cache coherence is maintained using a directory cache protocol, where the directory uses a presence-flag vector associated with each memory block to keep track of which nodes have copies of that block. The time it takes to process a *directory request* at the home and a remote node is in both cases 50 cycles. (Also the time to lookup or install into the cache at remote/host/local node is also 50 cycles). The latency and traffic of all consistency-induced requests and responses are detailed in the table above, where the block size B is 32 bytes. **Answer the following questions for each of the two MSI coherence protocols, i.e., the classical one that works in four hops and the optimized one (Standard DASH) that works in only three hops:**

**Task 4.a)** Determine the number of cycles needed to handle a read-cache miss when the home node is the same as the requesting node and the memory copy is clean. Also determine the amount of traffic (in bytes) caused by the coherence transaction.

**Task 4.b)** Determine the number of cycles needed to handle a read-cache miss when the home node is the same as the requesting node and the memory copy is dirty. Also determine the amount of traffic (in bytes) caused by the coherence transaction.

**Task 4.c)** Determine the number of cycles needed to handle a read-cache miss when the home node is different from the requesting node and the memory copy is clean. Also determine the amount of traffic (in bytes) caused by the coherence transaction.

**Task 4.d)** Determine the number of cycles needed to handle a read-cache miss when the home node is the same as the requesting node, the memory copy is dirty, and the remote node is the same as the home node. Also determine the amount of traffic (in bytes) caused by the coherence transaction.

**Task 4.e)** Determine the number of cycles needed to handle a read-cache miss when the home node is different from the requesting node, the memory copy is dirty, and the remote node is different from the home node (and of course different from the requesting node). Also determine the amount of traffic (in bytes) caused by the coherence transaction.

**Task 5)** We Consider a 16-by-16 torus (tori) interconnection network and determine the following interconnection network properties:

**Task 5.a)** network diameter,

**Task 5.b)** bisection bandwidth, assuming that each link has a bandwidth of 100 Mbits/s,

**Task 5.c)** the bandwidth per node.

**Task 6)** A design team is contemplating whether to use a  $n$ -by- $n$  torus (tori) or an  $n$ -dimensional hypercube to build an interconnect network that connects 4, 16, 64, and 256 nodes. In this exercise you will compare the network diameter and the bisection width for the two topologies to understand the trade-offs between them:

**Task 6.a)** At what scale does the hypercube provide (strictly) higher bisection width than the torus?

**Task 6.b)** Determine the network diameter and the switch degree for the scale at which the hypercube provides a higher bisection width than the torus.

**Task 6.c)** What can you say about the relative merits of the two topologies?