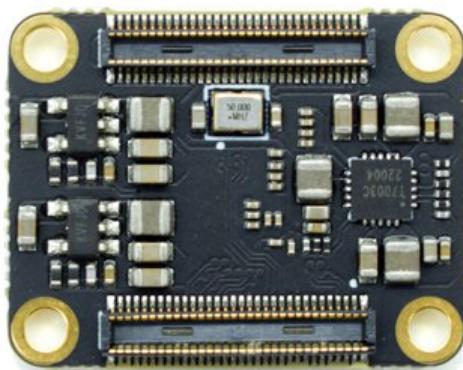




Tang Primer 25K

Specification v1.0



Release Note

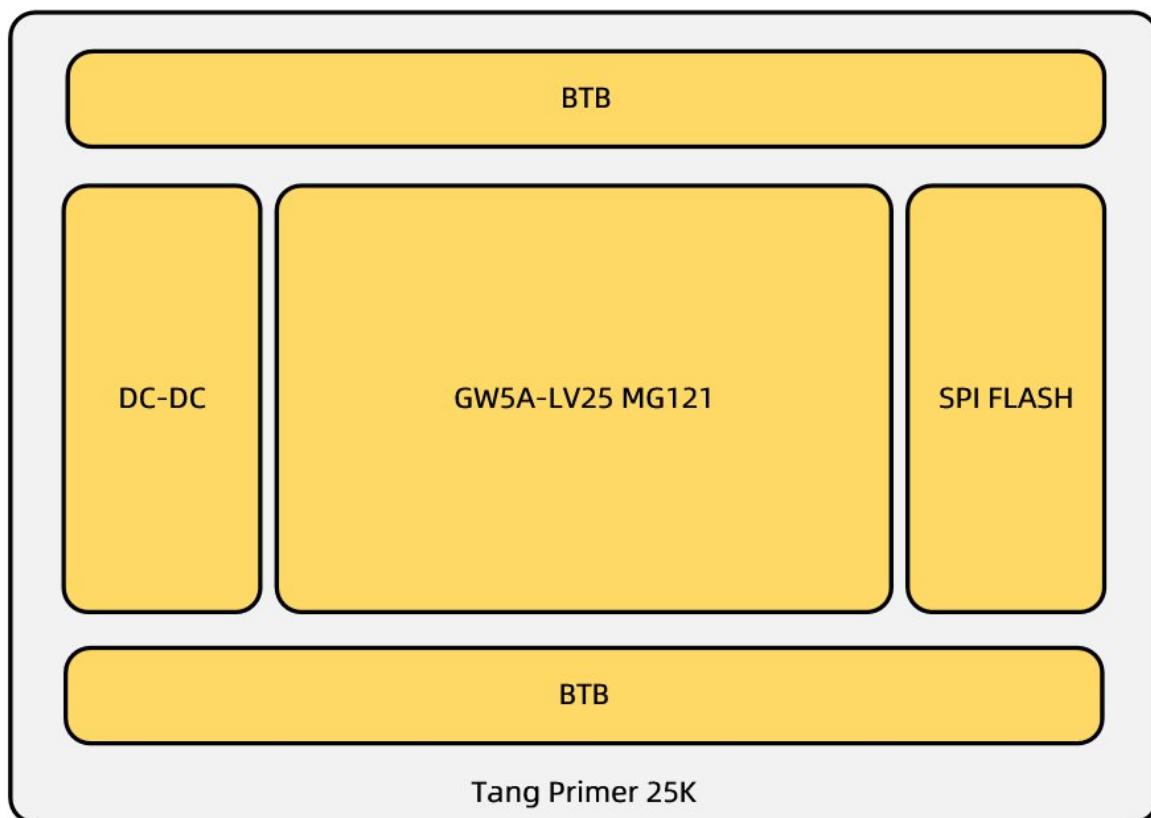
Version	Update content
V1.0	Edited on September 15 , 2023 ; Original Version ; PCB version : 52300

1. Overview

Tang Primer 25K is a compact and highly integrated FPGA core board. It integrates the Gowin GW5A-LV25MG121 as the main chip, 64Mbit SPI FLASH, DC-DC power supply, and BTB connectors. The core board provides 76 GPIOs, 1 hardcore 4-lane MIPI TX/RX, and 3 power outputs. By simply providing the core board with 5V power and configuring resistors, users can easily run the Tang Primer 25K core board.

Tang Primer 25K core board and Gowin FPGA development platform jointly help customers quickly achieve commercial landing in fields such as data communication, image processing, and industrial control.

1.1 Block Diagram



1.2 Hardware Overview

Component	Characteristic
Tang Primer 25K Core Board Note: Only some key features of the chip are mentioned on the right side. Please refer to the chip datasheet for detailed features	Logic Units (LUT4) : 23,040
	Register (REG) : 23,040
	Distributed Static Random Access Memory SSRAM: 180 kbits
	Block Static Random Access Memory BSRAM: 1,008 kbits
	Number of BSRAMs: 56个
	DSP: 28
	Phase locked loop (PLLs) : 6
	Global Clocks: 16
	High-speed Clocks: 16
	LVDS: 1.25Gbps
	MIPI D-PHY Hardcore : 2.5Gbps (RX/TX) , 4 data lanes, 1 clock lanes
	ADC: 1
	Available IO quantity : 75
	Dimension: 22.9mm x 17.8mm
	BTB male connector in Core Board: DF40C-60DP-0.4V(51) BTB female connector in Base Board: DF40C-60DS-0.4V(51)
	Note: BTB female connector has several heights for users to choose

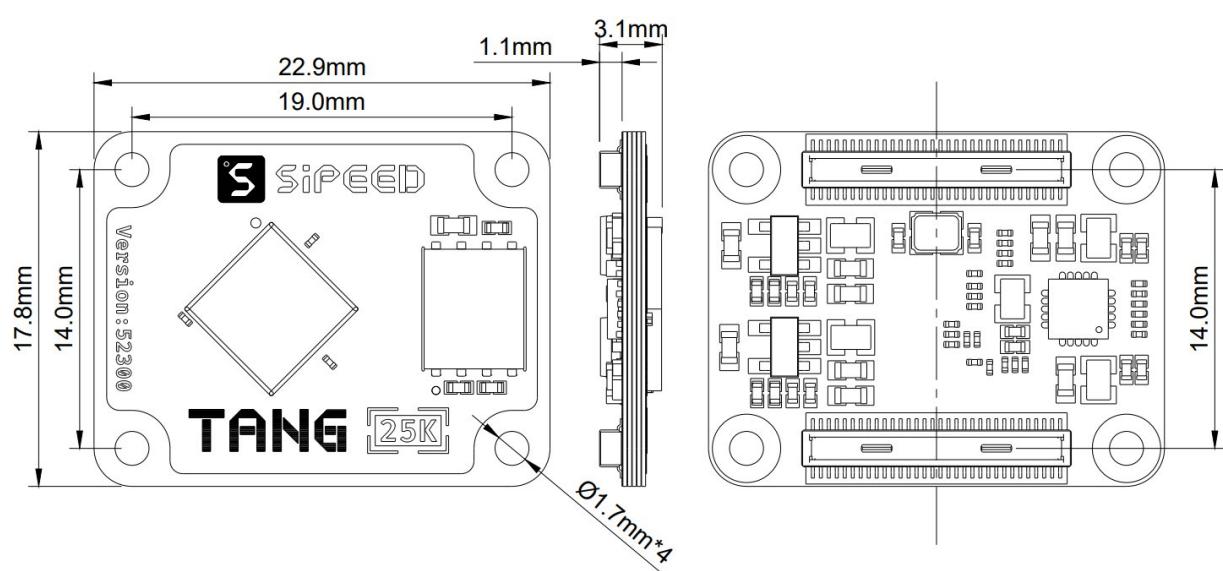
1.4 Working Conditions

Items	Description
Core board power supply demand	Working Voltage : Mainboard provide 3.6~5.5V to CoreBoard through VCC_5V net Working Current : Depends on actual operating conditions
Temperature rise	< 40K
Recommended operating temperature range	0°C ~ 85°C This series of chips has models with a wider operating temperature range to choose from. If you need it, please contact us via email
Minimum System Requirements	1.Mainboard provides VCC_5V for Coreboard. (Main power supply) 2.Mainboard provides VCCIO0/1, VCCIO2/3, VCCIO6/7 for Coreboard. (Bank power supply) 3.Reasonably configure READY, DONE, and JTAG_TCK through resistors on the Mainboard

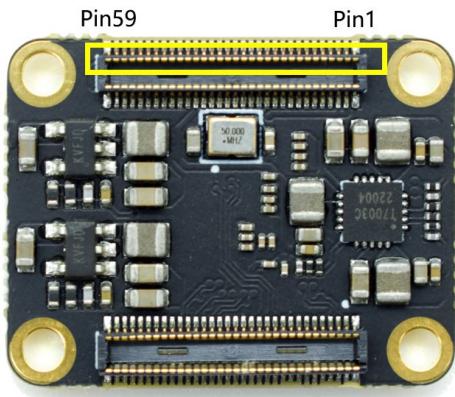
2. Apperance Parameters

2.1 Dimension

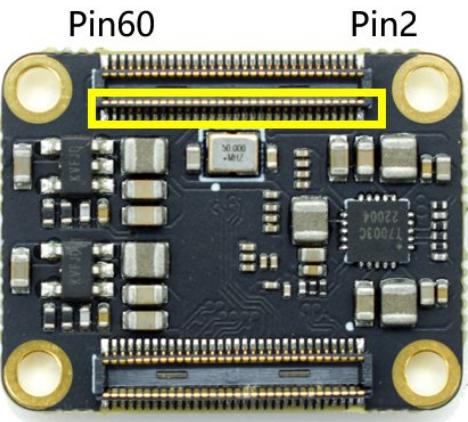
Items	Description
Length	22.9 mm
width	17.8 mm
Thickness	Please review the 3D drawings



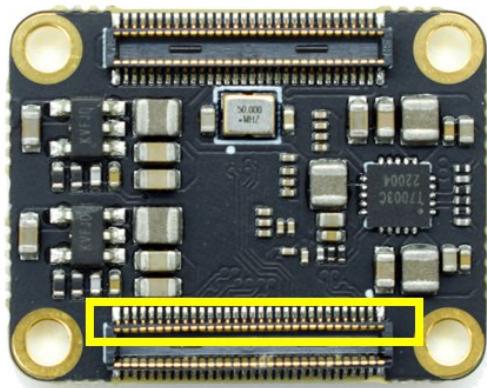
3. Description of pinout



CoreBoard Schematic	BTB Pin number	SOC pin	Bank	Bank Voltage	Pin Name	Configuration Pin	GCLK/PLL
J2 BTB Connector	1	GND					
	3	B2	5	3.3V	IOB4A		LPLL1_T_FBO
	5	C2	5	3.3V	IOB4B		
	7	F2	5	3.3V	IOB26A		GCLKT_12
	9	F1	5	3.3V	IOB26B		GCLKC_12
	11	A1	5	3.3V	IOB24A		
	13	D8	5	3.3V	IOB1A	RECONFIG	
	15	E1	5	3.3V	IOB12B		GCLKC_10B/ LPLL1_C_IN1
	17	D1	5	3.3V	IOB14B		CLKHOLD_N
	19	GND					
	21	C1	10	3.3V	IOR1A	JTAG_TCK	
	23	B1	10	3.3V	IOR3A	JTAG_TMS	
	25	A2	10	3.3V	IOR3B	JTAG_TDO	
	27	A3	10	3.3V	IOR1B	JTAG_TDI	
	29	GND					
	31	MIPI_D3_P					
	33	MIPI_D3_N					
	35	GND					
	37	MIPI_D2_P					
	39	MIPI_D2_N					
	41	GND					
	43	MIPI_CK_P					
	45	MIPI_CK_N					
	47	GND					
	49	MIPI_D1_P					
	51	MIPI_D1_N					
	53	GND					
	55	MIPI_D0_P					
	57	MIPI_D0_N					
	59	GND					



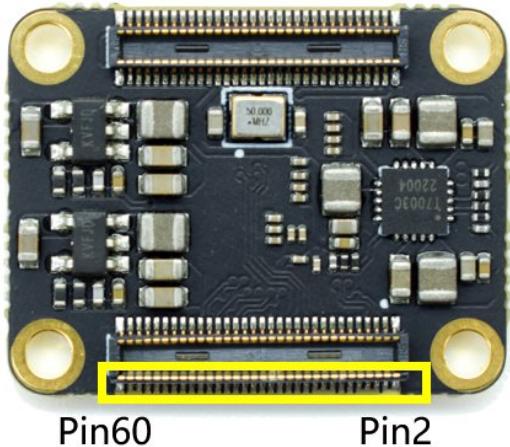
CoreBoard Schematic	BTB Pin number	SOC pin	Bank	Bank Voltage	Pin Name	Configuration Pin	GCLK/PLL
J2 BTB Connector	2	VCCIO2/3 Input					
	4	VCCIO2/3 Input					
	6	L2	2	Depend on VCCIO2/3	IOR18A		
	8	L1	2	Depend on VCCIO2/3	IOR18B		
	10	K1	2	Depend on VCCIO2/3	IOR20A		
	12	K2	2	Depend on VCCIO2/3	IOR20B		
	14	J4	2	Depend on VCCIO2/3	IOR22A		
	16	K4	2	Depend on VCCIO2/3	IOR22B		
	18	G2	2	Depend on VCCIO2/3	IOR24A		RPLL1B_T_IN0
	20	G1	2	Depend on VCCIO2/3	IOR24B		
	22	L4	2	Depend on VCCIO2/3	IOR31A		GCLKT_4/RPLL1A_T_IN0
	24	L3	2	Depend on VCCIO2/3	IOR31B		GCLKC_4/RPLL1_C_FB1
	26	J1	2	Depend on VCCIO2/3	IOR33A		GCLKT_5/RPLL1_T_IN1
	28	J2	2	Depend on VCCIO2/3	IOR33B		GCLKC_5/RPLL1_C_FBO
	30	G4	3	Depend on VCCIO2/3	IOB89A		GCLKT_7/BPLL_T_IN0
	32	H4	3	Depend on VCCIO2/3	IOB89B		GCLKC_7
	34	H1	3	Depend on VCCIO2/3	IOB91A		GCLKT_6A
	36	H2	3	Depend on VCCIO2/3	IOB91B		GCLKC_6A
	38	VDD_1V8 Output					
	40	VDD_1V8 Output					
	42	VDD_2V5 Output					
	44	VDD_2V5 Output					
	46	VDD_3V3 Output					
	48	VDD_3V3 Output					
	50	VDD_3V3 Output					
	52	VDD_5V0 Input					
	54	VDD_5V0 Input					
	56	VDD_5V0 Input					
	58	VDD_5V0 Input					
	60	VDD_5V0 Input					



Pin59

Pin1

CoreBoard Schematic	BTB Pin number	SOC pin	Bank	Bank Voltage	Pin Name	Configuration Pin	GCLK/PLL
J1 BTB Connector	1	GND					
	3	L9	0	Depend on VCCIO0/1	IOT31A		
	5	K9	0	Depend on VCCIO0/1	IOT31B		
	7	J8	0	Depend on VCCIO0/1	IOT56A		GCLKT_0/TPLL_T_IN1
	9	K8	0	Depend on VCCIO0/1	IOT56B		GCLKC_0/TPLL_C_FB1
	11	F7	0	Depend on VCCIO0/1	IOT58A		GCLKT_1/TPLL_T_IN2
	13	F6	0	Depend on VCCIO0/1	IOT58B		GCLKC_1/TPLL_C_FB0
	15	GND					
	17	E8	4	3.3V	IOB37A	READY	
	19	B3	4	3.3V	IOB56A		
	21	C3	4	3.3V	IOB56B		
	23	E3	4	3.3V	IOB60A		
	25	D7	4	3.3V	IOB64A	DONE	
	27	GND					
	29	VCCIO6/7 Input					
	31	VCCIO6/7 Input					
	33	J11	7	Depend on VCCIO6/7	IOT1A		GCLKT_15/LPLL0_T_IN0
	35	J10	7	Depend on VCCIO6/7	IOT1B		GCLKC_15
	37	H11	7	Depend on VCCIO6/7	IOT3A		GCLKT_16
	39	H10	7	Depend on VCCIO6/7	IOT3B		GCLKC_16
	41	G11	7	Depend on VCCIO6/7	IOT7A		
	43	G10	7	Depend on VCCIO6/7	IOT7B		
	45	GND					
	47	D11	6	Depend on VCCIO6/7	IOL9A		
	49	D10	6	Depend on VCCIO6/7	IOL9B		
	51	C11	6	Depend on VCCIO6/7	IOL5A		GCLKT_13/LPLL0_T_IN1
	53	C10	6	Depend on VCCIO6/7	IOL5B		GCLKC_13/LPLL0_C_FB1
	55	B11	6	Depend on VCCIO6/7	IOL12A		
	57	B10	6	Depend on VCCIO6/7	IOL12B		
	59	GND					



CoreBoard Schematic	BTB Pin number	SOC pin	Bank	Bank Voltage	Pin Name	Configuration Pin	GCLK/PLL
J1 BTB Connector	2	GND					
	4	H5	1	Depend on VCCIO0/1	IOT61A		GCLKT_2/TPLL_T_IN0
	6	J5	1	Depend on VCCIO0/1	IOT61B		GCLKC_2
	8	L5	1	Depend on VCCIO0/1	IOT63A		GCLKT_3/RPLL0_T_IN0
	10	K5	1	Depend on VCCIO0/1	IOT63B		GCLKC_3
	12	H8	1	Depend on VCCIO0/1	IOT66A		
	14	H7	1	Depend on VCCIO0/1	IOT66B		
	16	G7	1	Depend on VCCIO0/1	IOT68A		
	18	G8	1	Depend on VCCIO0/1	IOT68B		
	20	F5	1	Depend on VCCIO0/1	IOT72A		
	22	G5	1	Depend on VCCIO0/1	IOT72B		
	24	VCCIO0/1 Input					
	26	VCCIO0/1 Input					
	28	GND					
	30	L6	7	Depend on VCCIO6/7	IOT23A		
	32	K6	7	Depend on VCCIO6/7	IOT23B		
	34	K7	7	Depend on VCCIO6/7	IOT21A		
	36	J7	7	Depend on VCCIO6/7	IOT21B		
	38	L7	7	Depend on VCCIO6/7	IOT19A		
	40	L8	7	Depend on VCCIO6/7	IOT19B		
	42	L10	7	Depend on VCCIO6/7	IOT15A		
	44	K10	7	Depend on VCCIO6/7	IOT15B		
	46	K11	7	Depend on VCCIO6/7	IOT11A		
	48	L11	7	Depend on VCCIO6/7	IOT11B		
	50	GND					
	52	E11	6	Depend on VCCIO6/7	IOL3A		GCLKT_14A/LPLL0_T_IN2/LPLL1B_T_IN0
	54	E10	6	Depend on VCCIO6/7	IOL3B		GCLKC_14/LPLL0_C_FBO
	56	A11	6	Depend on VCCIO6/7	IOL14A		LPLL1A_T_IN0
	58	A10	6	Depend on VCCIO6/7	IOL14B		
	60	GND					

4. Notice

Item	Description
ESD protection	Please pay attention to avoid ESD hitting the PCBA. Please discharge the human static electricity before touching PCBA
IO voltage	Please don't let the actual working voltage of IO exceed the rated value, otherwise it will cause permanent damage to PCBA
Avoid short circuit	Please avoid any liquid or metal touching the pads of components on PCBA during power on, otherwise it will cause short circuit and damage the PCBA
Removing Core Board	Please pull out the Core Board from both sides at the same time, otherwise there is a high probability of damaging the BTB connector. If conditions permit, please use dedicated IC puller
Installing Core Board	Before installing the core board, please check that the appearance of the BTB connector of the core board and the base board are normal. If there is any deviation, it needs to be aligned before installation. If forcibly installed, it may cause damage to the BTB connector

5. Resources

Item	Description
Official website	www.sipeed.com
Github	https://github.com/Sipeed
BBS	http://bbs.sipeed.com
Wiki	wiki.sipeed.com
Sipeed model platform	https://maixhub.com/
SDK /HDK	https://dl.sipeed.com/
E-mail (For Technical support & Business cooperation)	support@sipeed.com



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