ALTERA Cyclone IV Development & Education Board (DE0-Nano)

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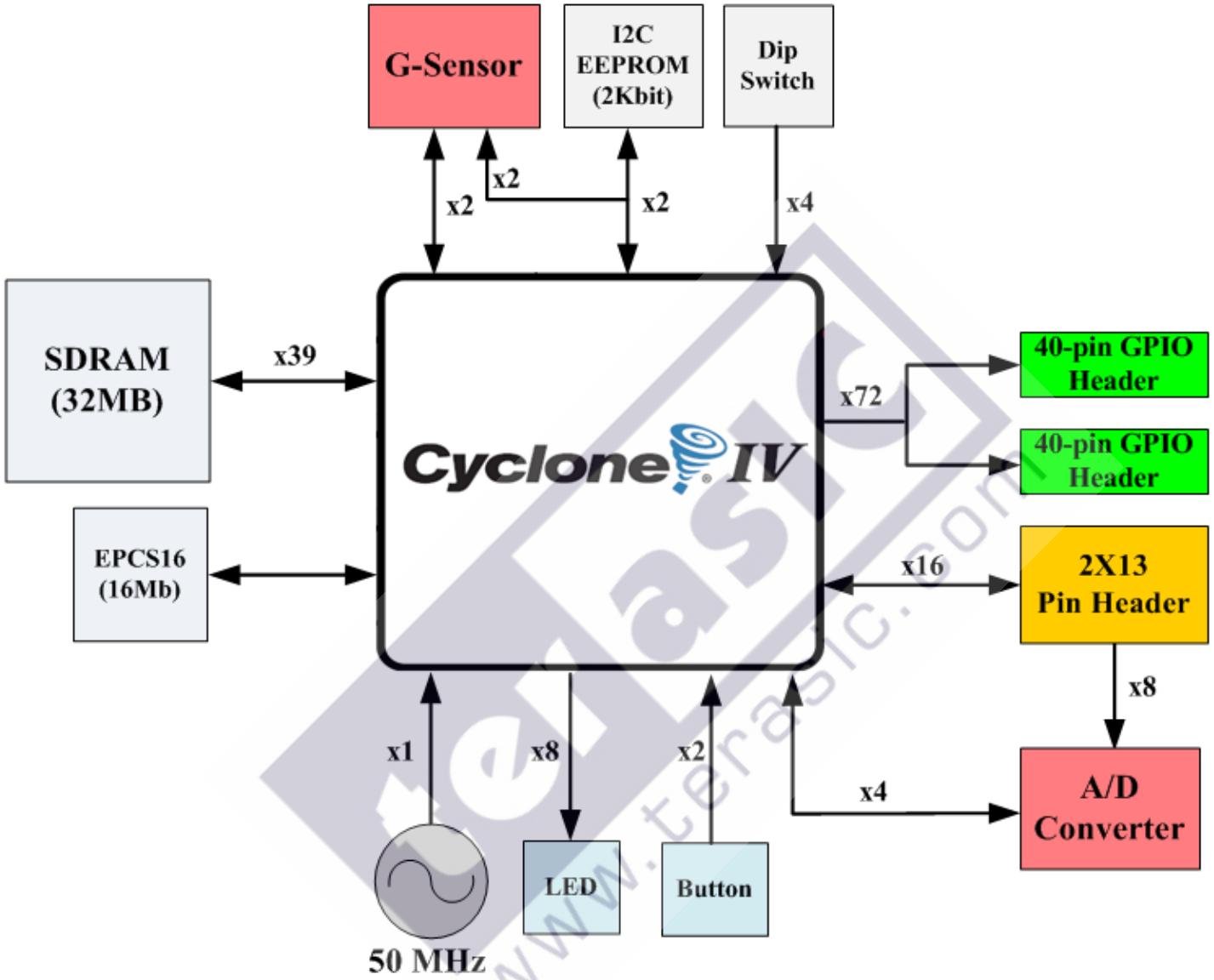
Title: **DE0-Nano Board**

Size	Document Number	Rev
B	COVER PAGE	C

Date: Thursday, July 12, 2012 Sheet 1 of 14



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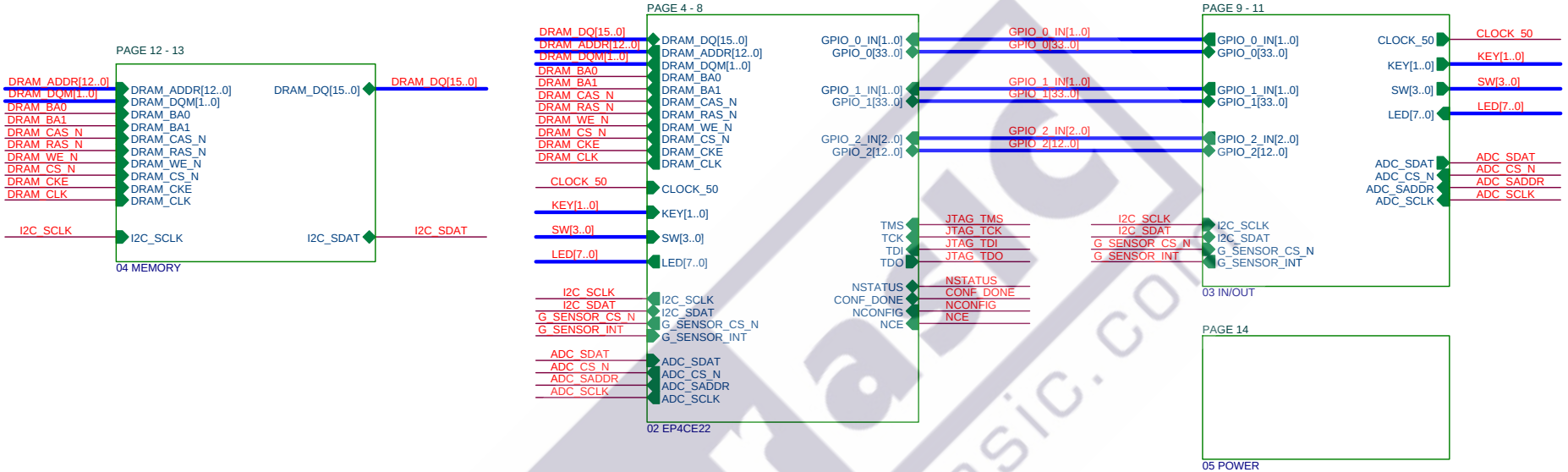
Title: **DE0-Nano Board**

Size	Document Number	Rev
B	PLACEMENT	C

Date: Thursday, July 12, 2012 Sheet 2 of 14



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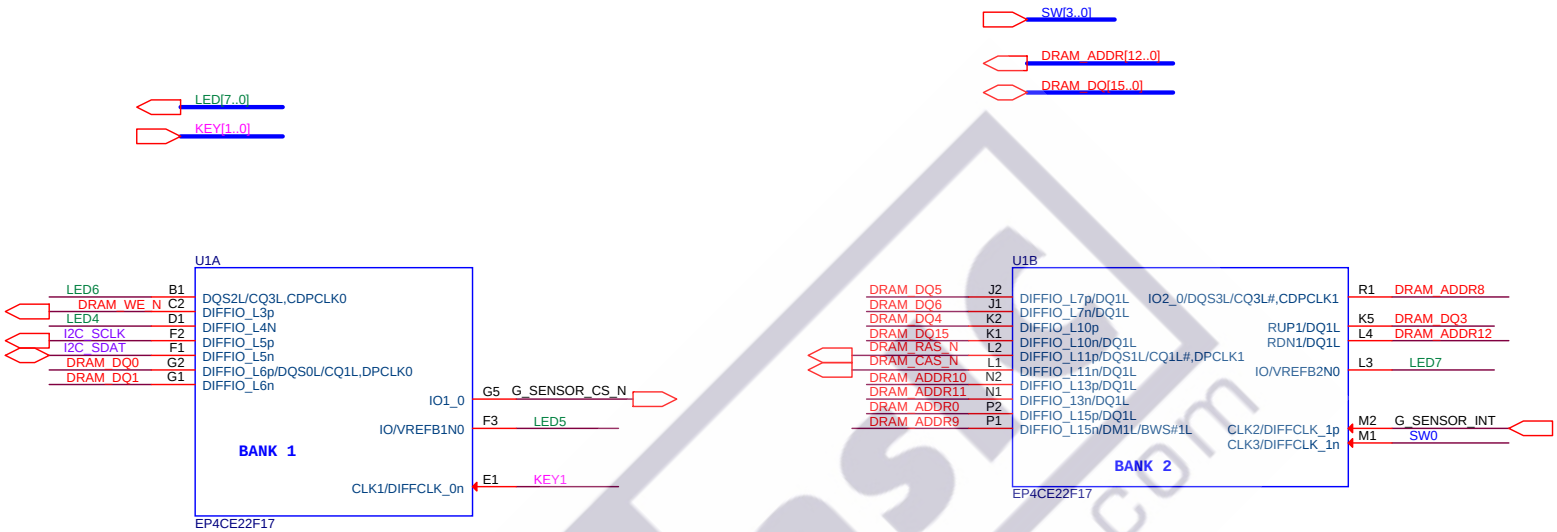
Title: **DE0-Nano Board**

Size	Document Number	Rev
B	TOP	C

Date: Thursday, July 12, 2012 Sheet 3 of 14



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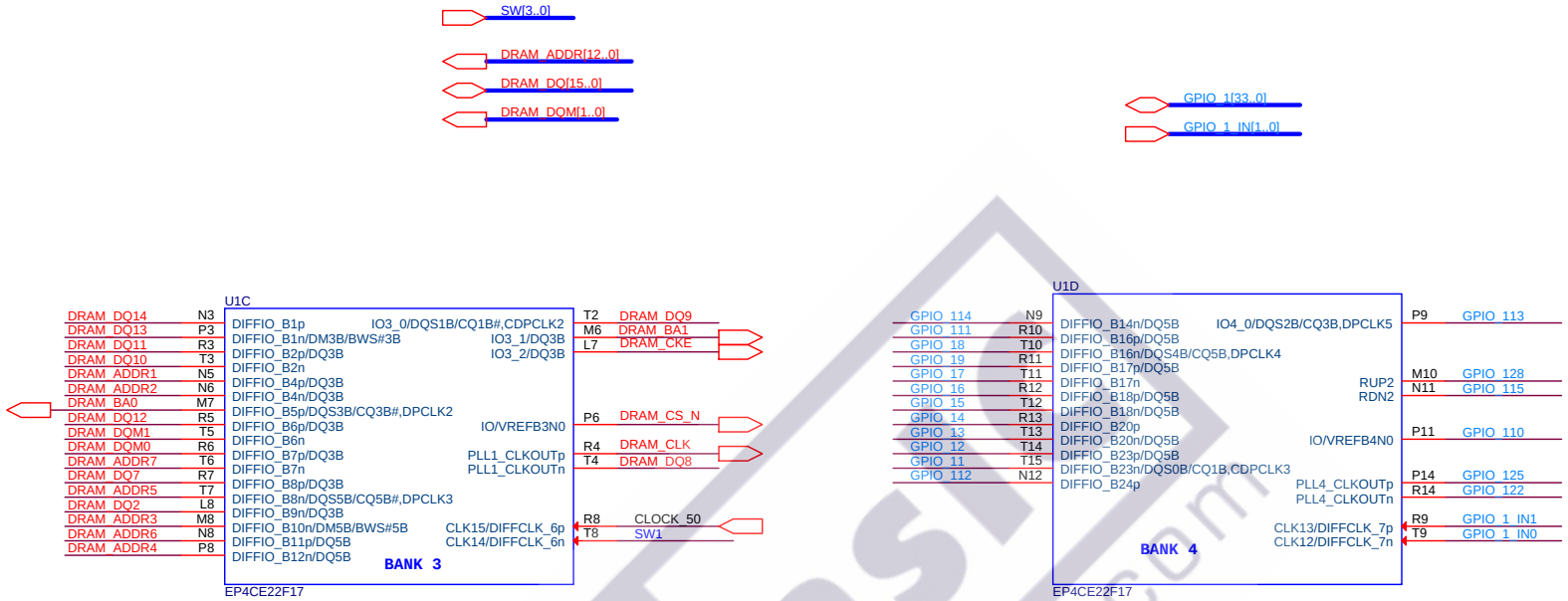
Title
DE0-Nano Board

Size	Document Number	Rev
B	EP4CE22 BANK1 & BANK2	C

Date: Thursday, July 12, 2012 Sheet 4 of 14



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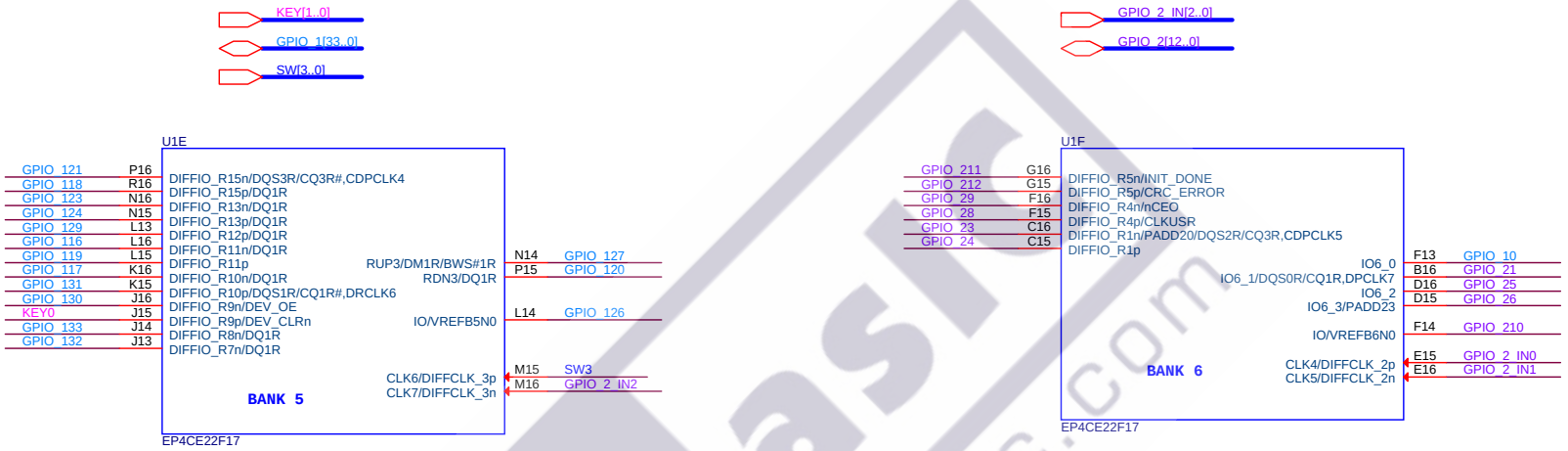
Title: **DE0-Nano Board**

Size	Document Number	Rev
B	EP4CE22 BANK3 & BANK4	C

Date: Thursday, July 12, 2012 Sheet 5 of 14



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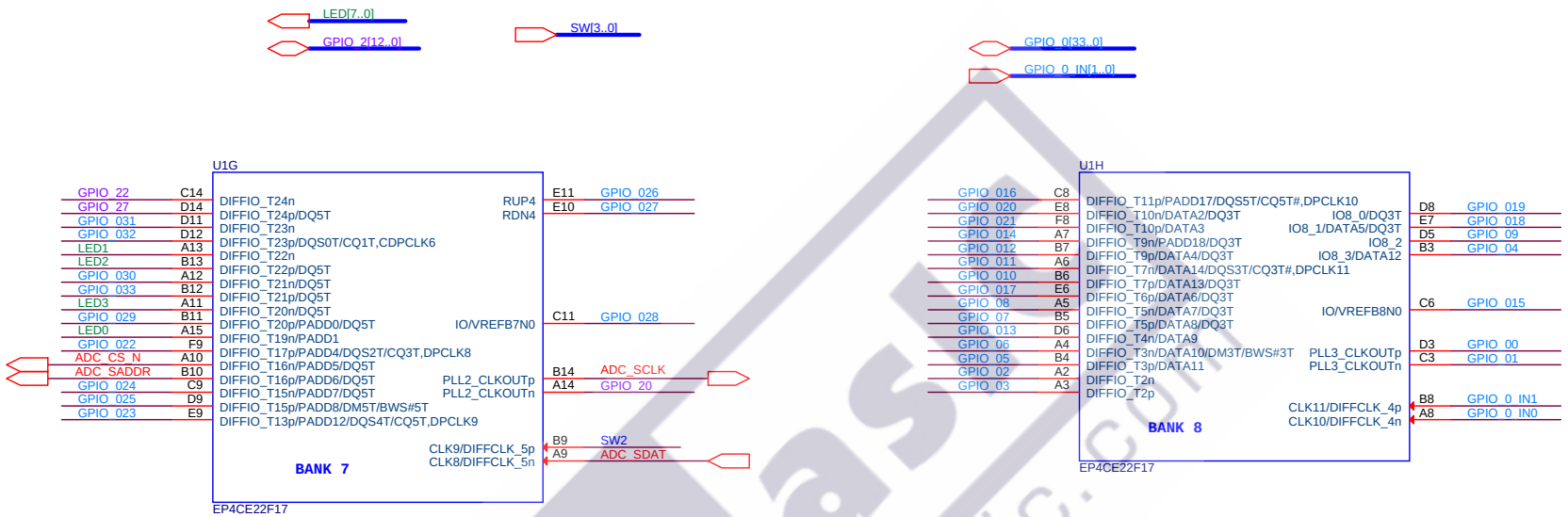
Title: **DE0-Nano Board**

Size	Document Number	Rev
B	EP4CE22 BANK5 & BANK6	C

Date: Thursday, July 12, 2012 Sheet 6 of 14



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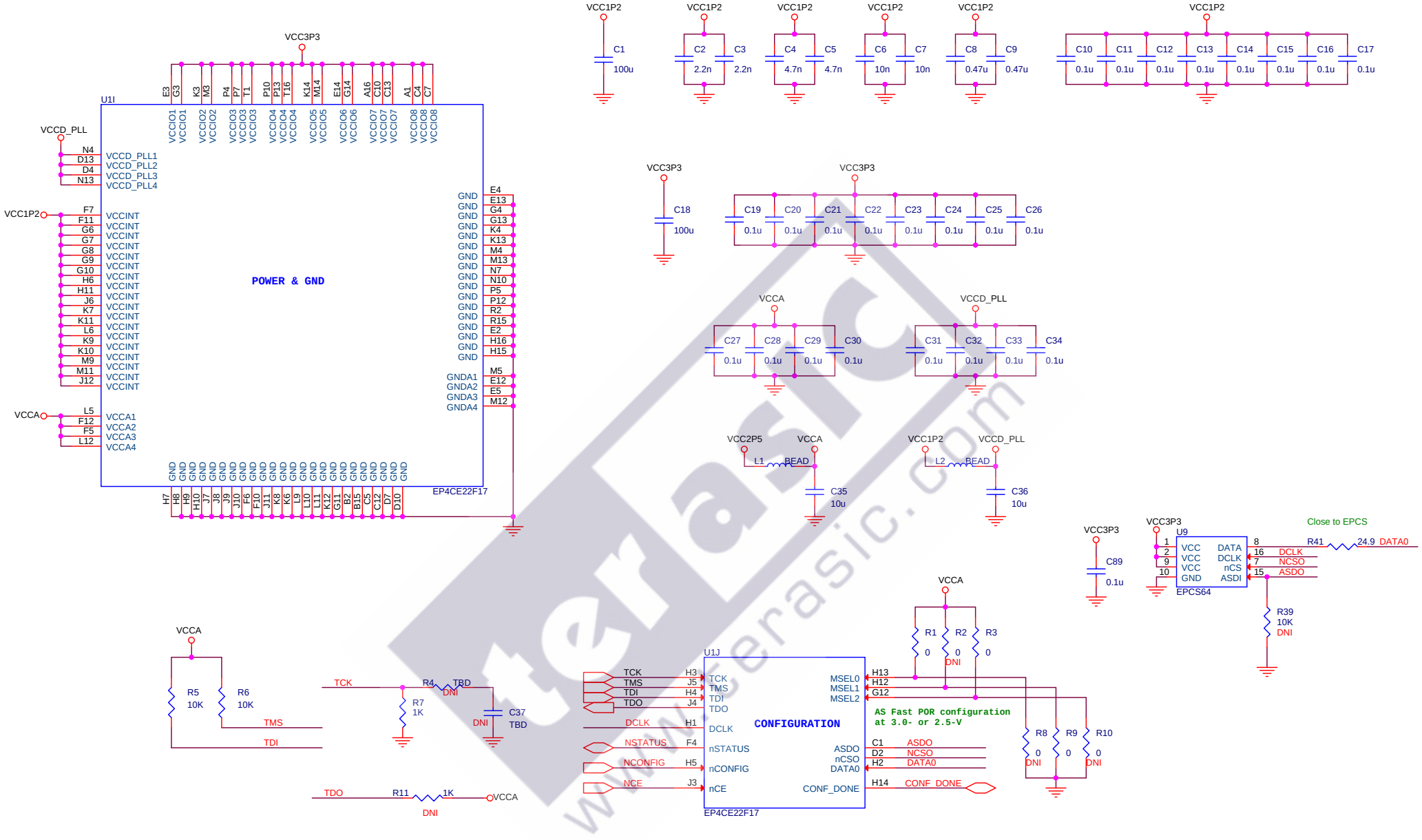
Title: **DE0-Nano Board**

Size	Document Number	Rev
B	EP4CE22 BANK7 & BANK8	C

Date: Thursday, July 12, 2012 Sheet 7 of 14



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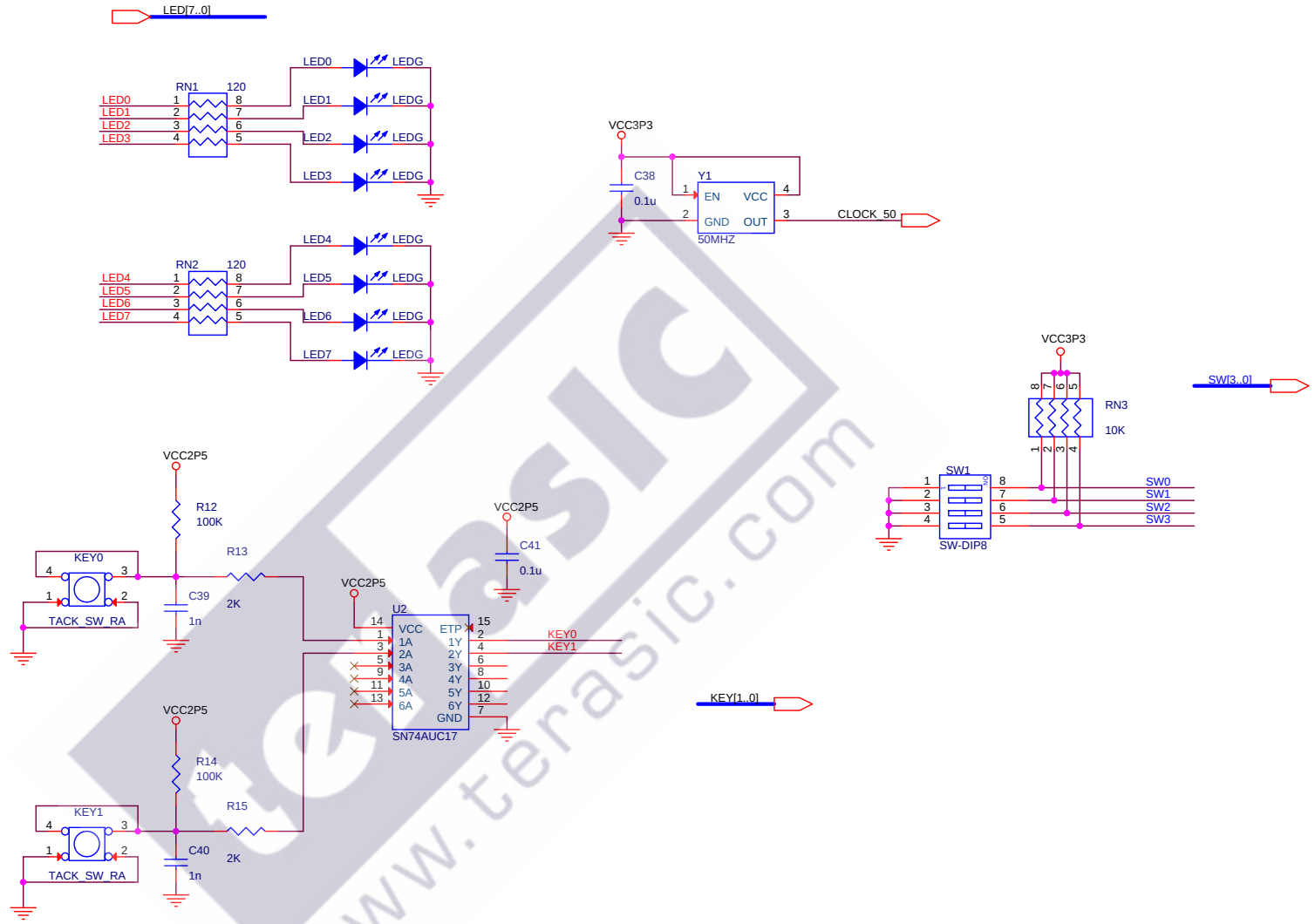
Title: **DE0-Nano Board**

Size	Document Number	Rev
B	EP4CE22 POWER and CONFIGURATION	C

Date: Thursday, July 12, 2012 Sheet 8 of 14



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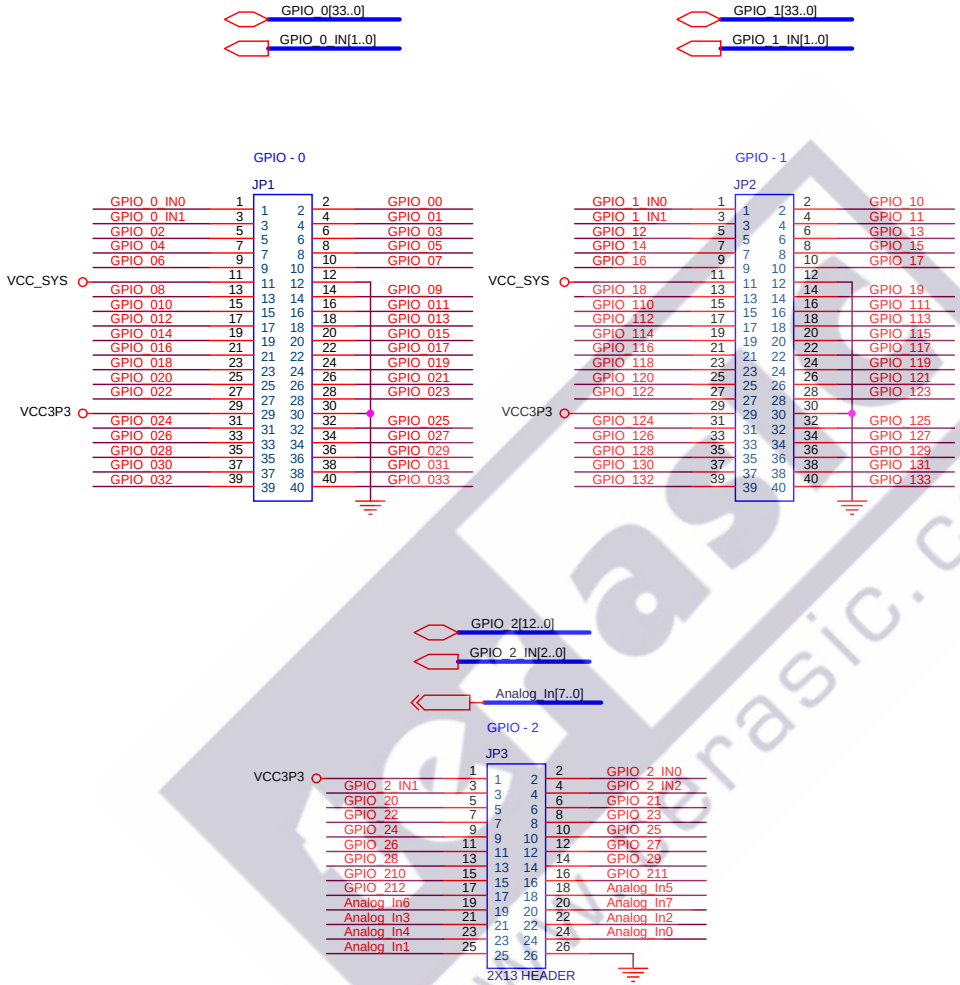
Title
DE0-Nano Board

Size	Document Number	Rev
B	CLOCK & LED & BUTTON & SWITCH	C

Date: Thursday, July 12, 2012 Sheet 9 of 14



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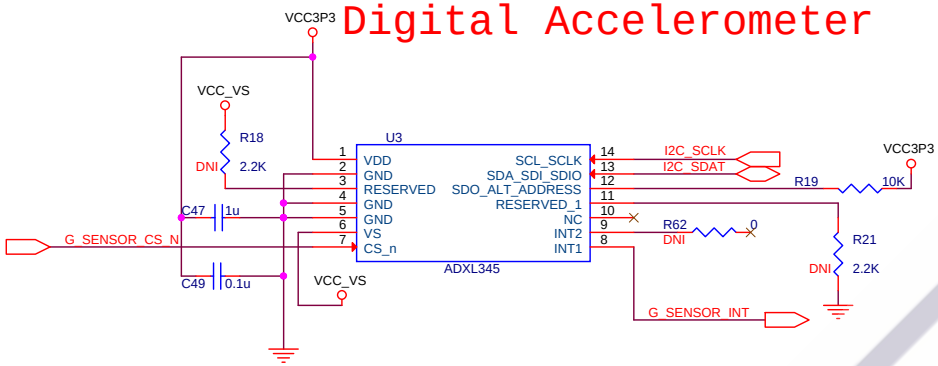
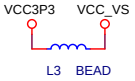
Title: **DE0-Nano Board**

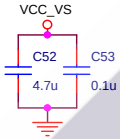
Size	Document Number	Rev
B	GPIOs & 2X13 Header	C

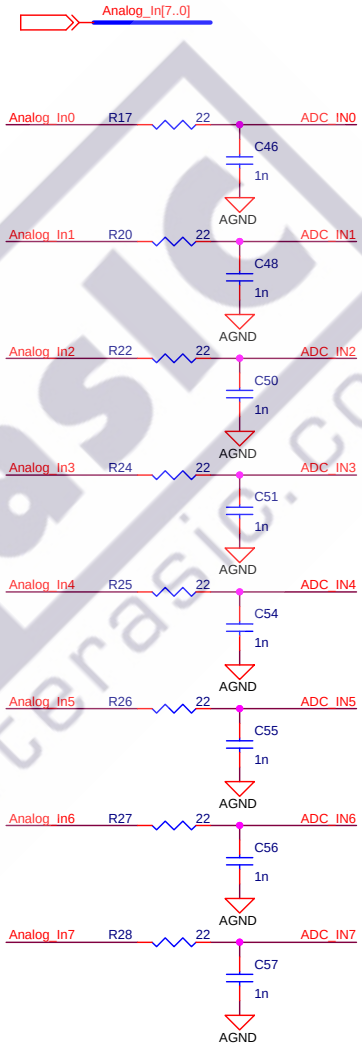
Date: Thursday, July 12, 2012 Sheet 10 of 14

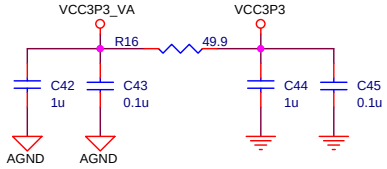
Digital Accelerometer

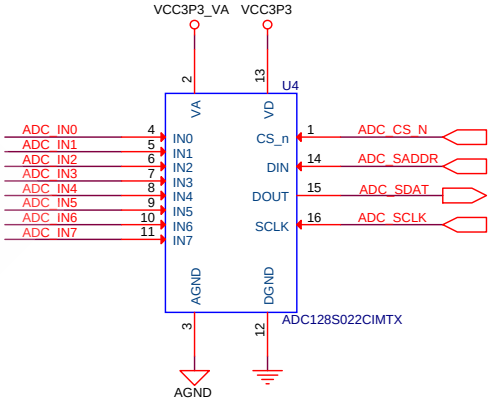


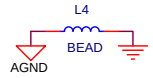












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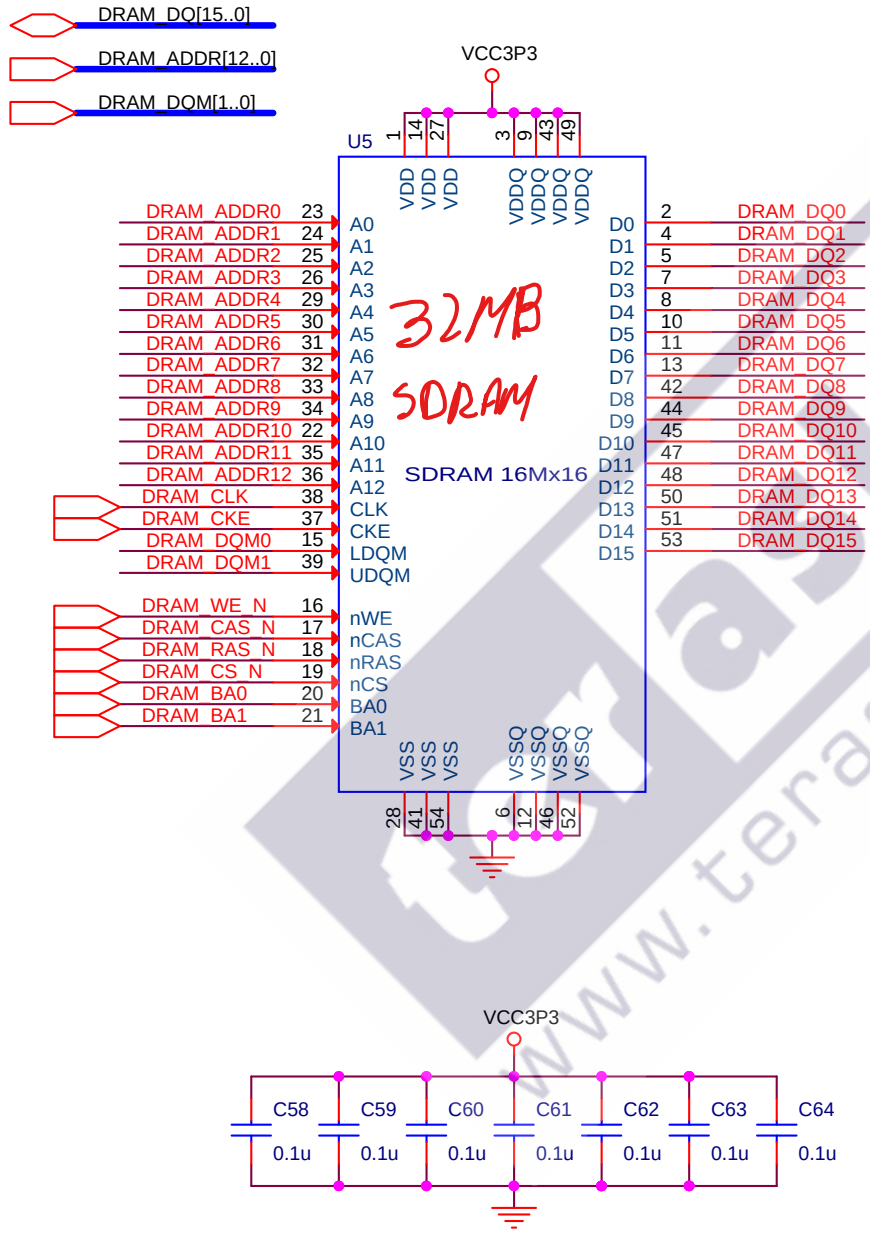
Title	DE0-Nano Board	
Size B	Document Number G-Sensor & ADC	Rev C
Date: Thursday, July 12, 2012	Sheet 11 of 14	



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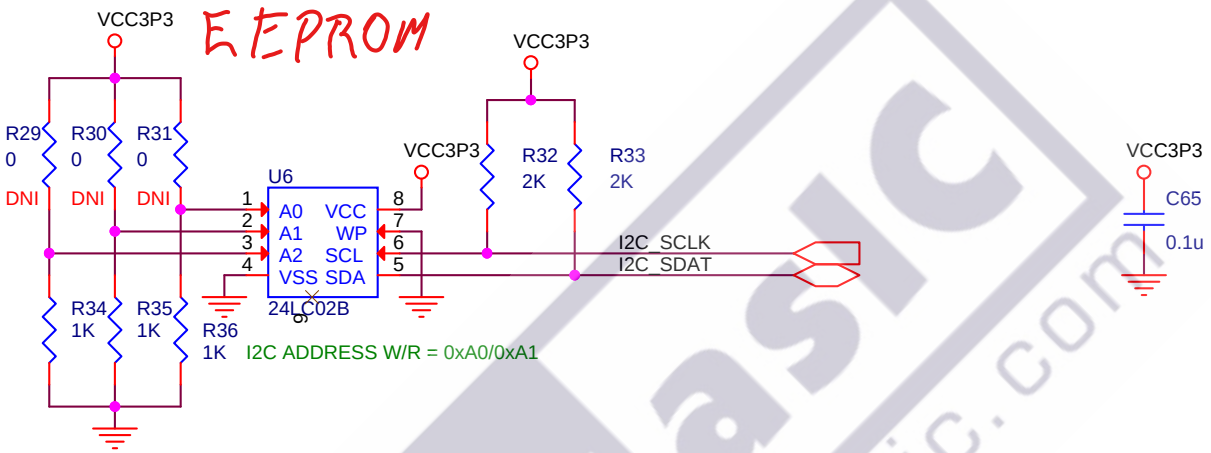
Title
DE0-Nano Board

Size	Document Number	Rev
A	SDRAM	C

Date: Thursday, July 12, 2012 Sheet 12 of 14



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Title: **DE0-Nano Board**

Size	Document Number	Rev
A	EEPROM	C

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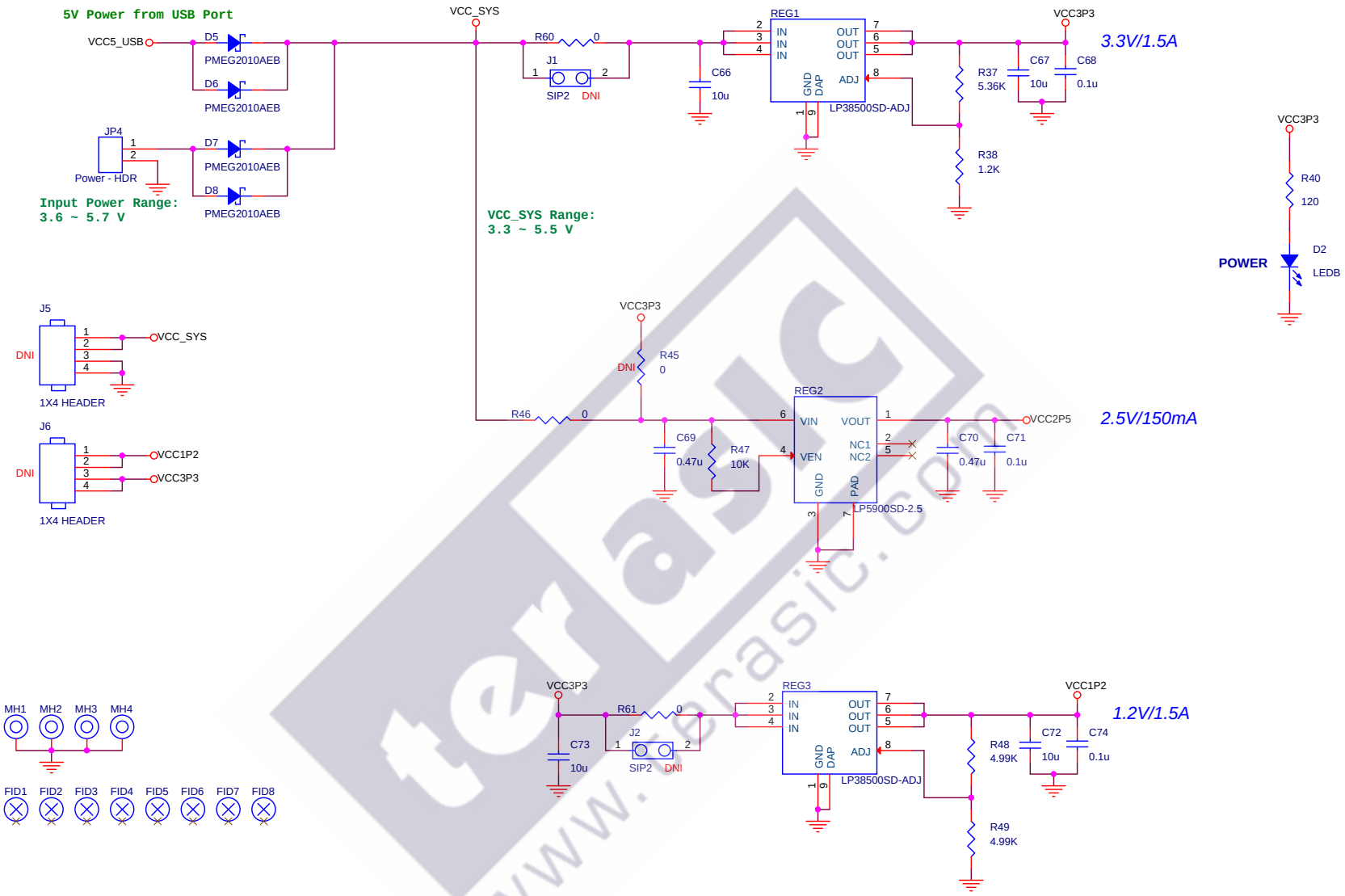

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Title: **DE0-Nano Board**

Size	Document Number	Rev
B	1.2V & 2.5V & 3.3V	C

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