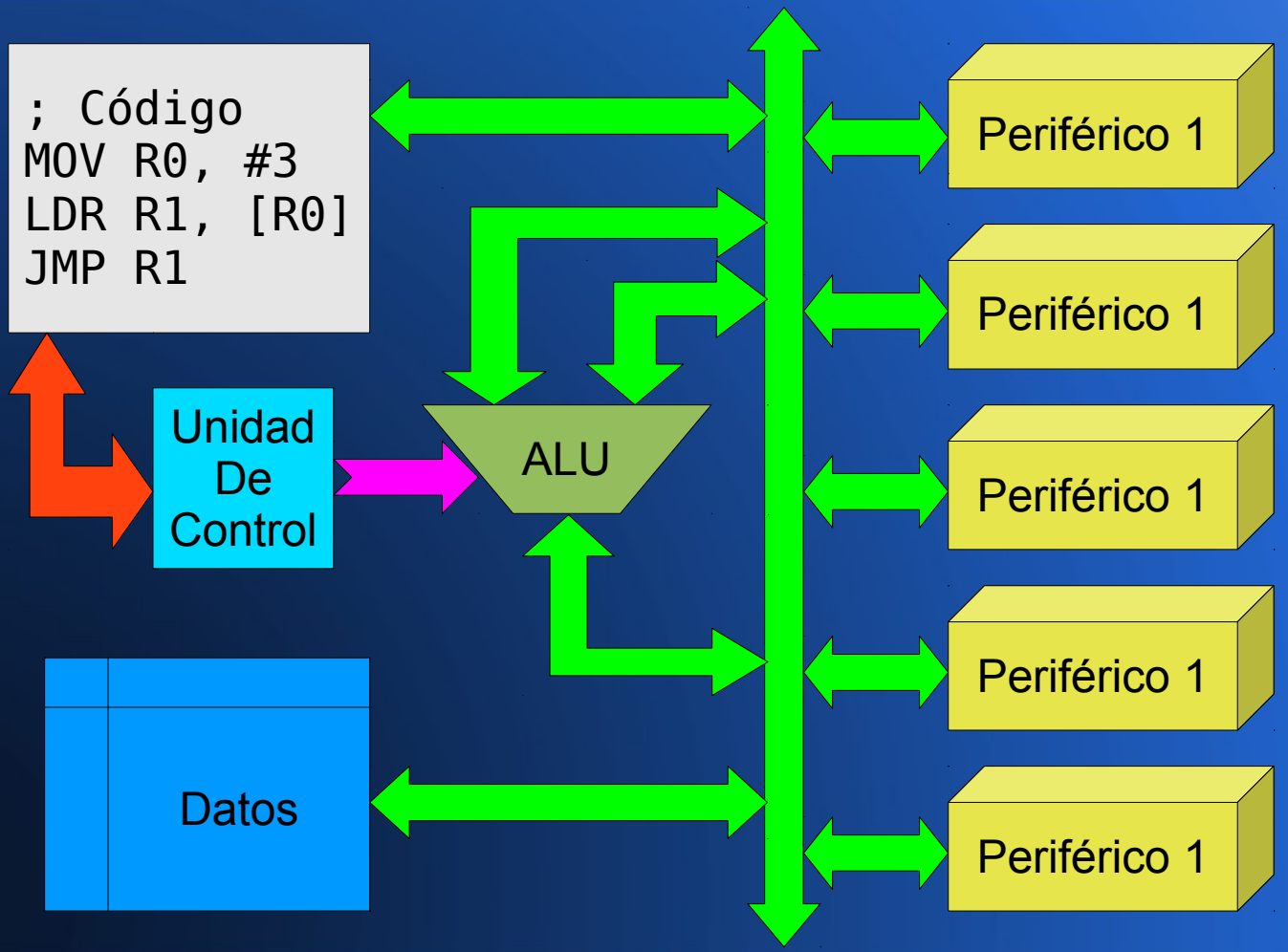
Curso ARM Cortex M3

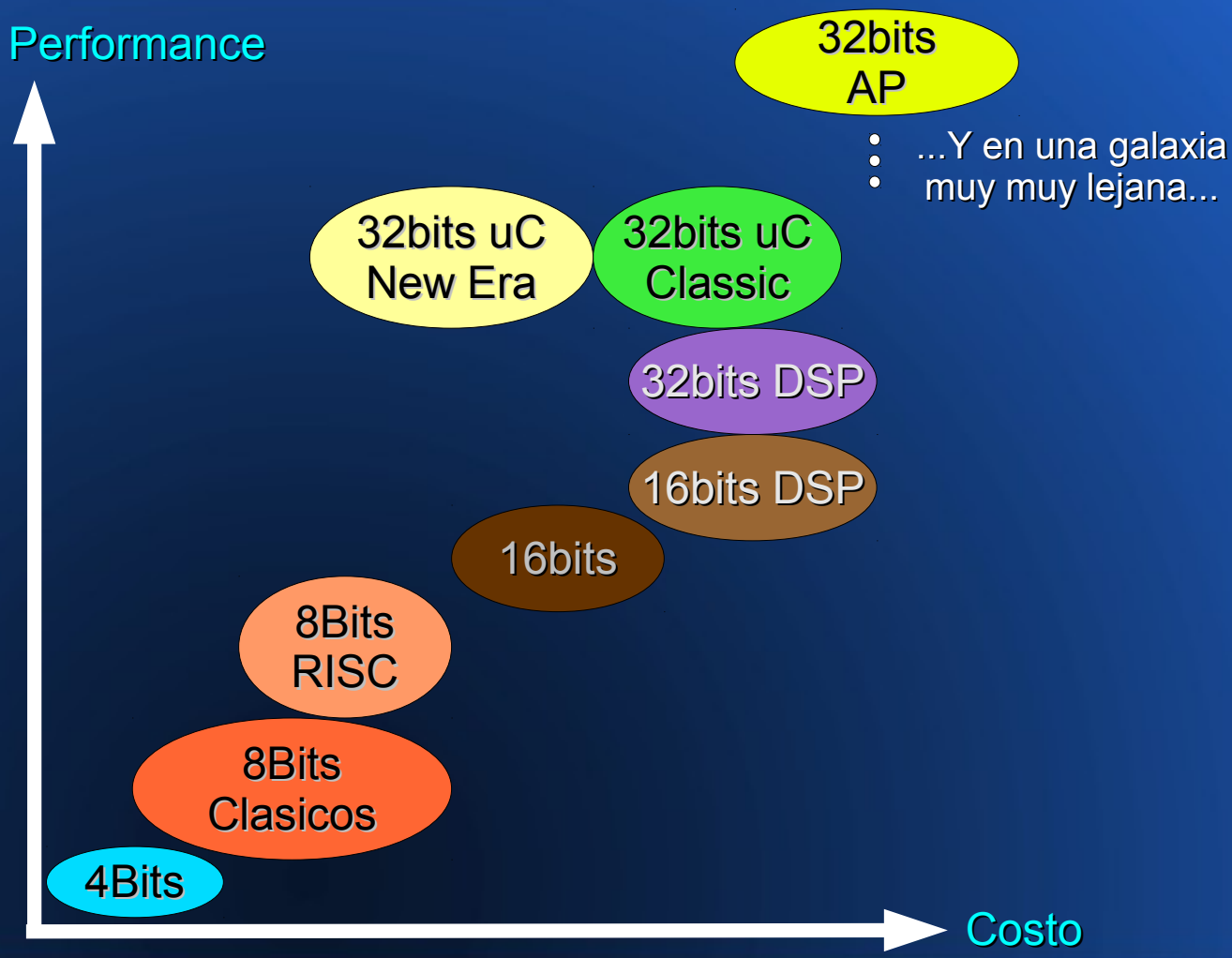
Temario Día 1

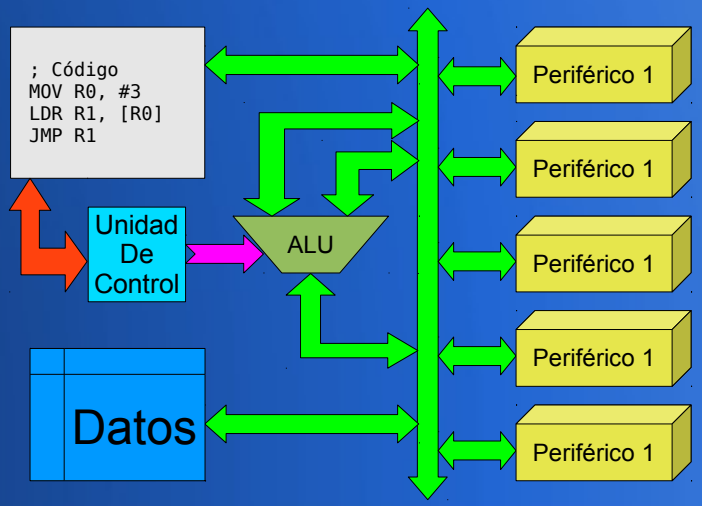
- Microcontroladores
- Advanced RISC Machines
  - Cortex M Series
  - Arquitectura Cortex M3
  - Periféricos, IP Cores y partner hardware
- Herramientas de desarrollo
  - Compiladores, IDEs y Programadores
  - Programación.
  - Programa tipo 1: Blink Led.
  - Programa tipo 2: Comunicación serial+SPI

Microcontroladores



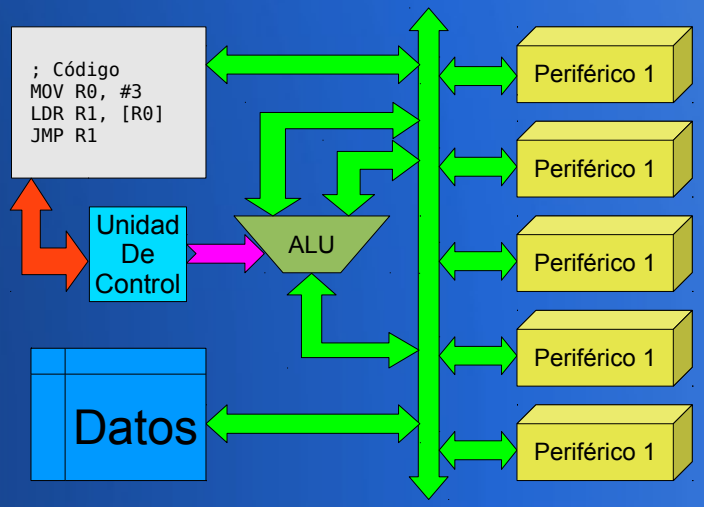
Microcontroladores





Microcontroladores

- Atmel: MCS51, AVR8, AVR32, ARM7/9, Cortex M3
- Microchip: PIC, dsPIC, MIPS m4k (PIC32)
- Freescale: Coldfire, HCS08, HC11/12, PPC, Cortex M3/4
- Hitachi: SuperH, SH8, ARM9
- NXP: MCS51, ARM7/9, Cortex M3
- ST: STR7/8, ARM7/9, Cortex M3
- Texas: TMS320, ARM9, Cortex M3, Cortex A8/9
- ...y un largo etc...



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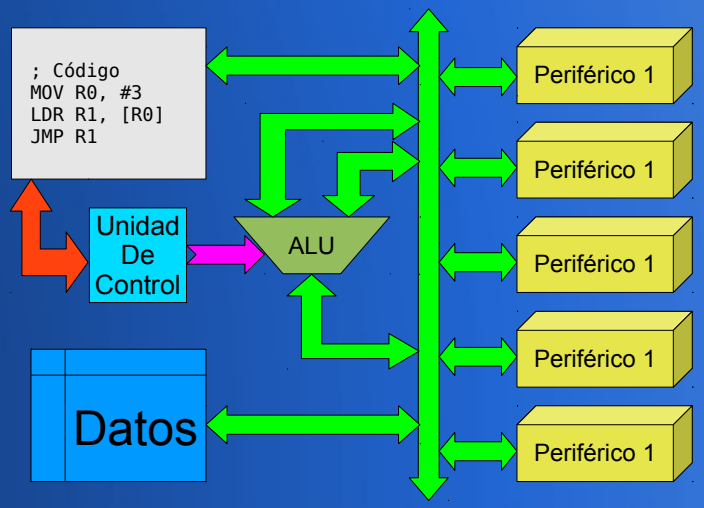
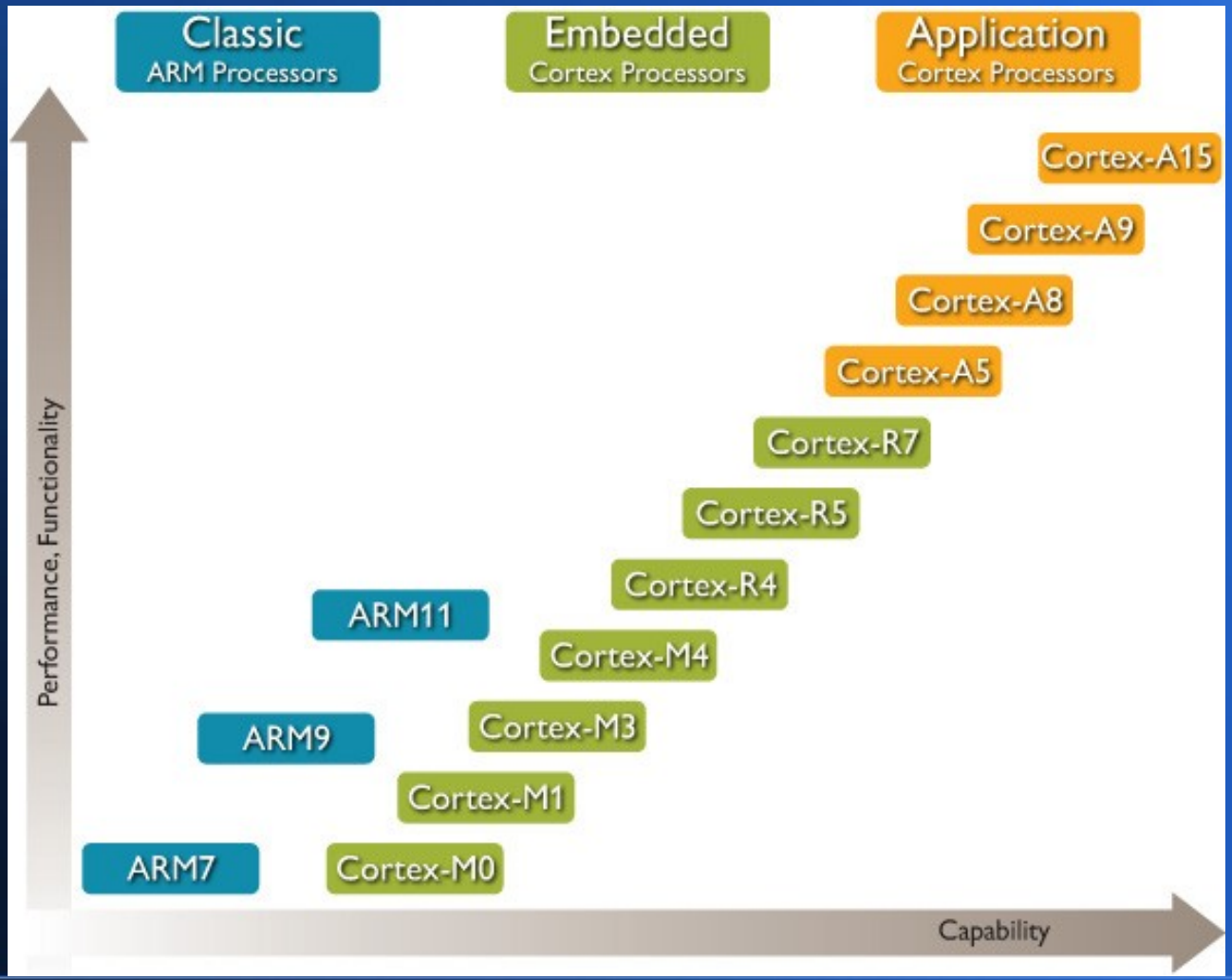


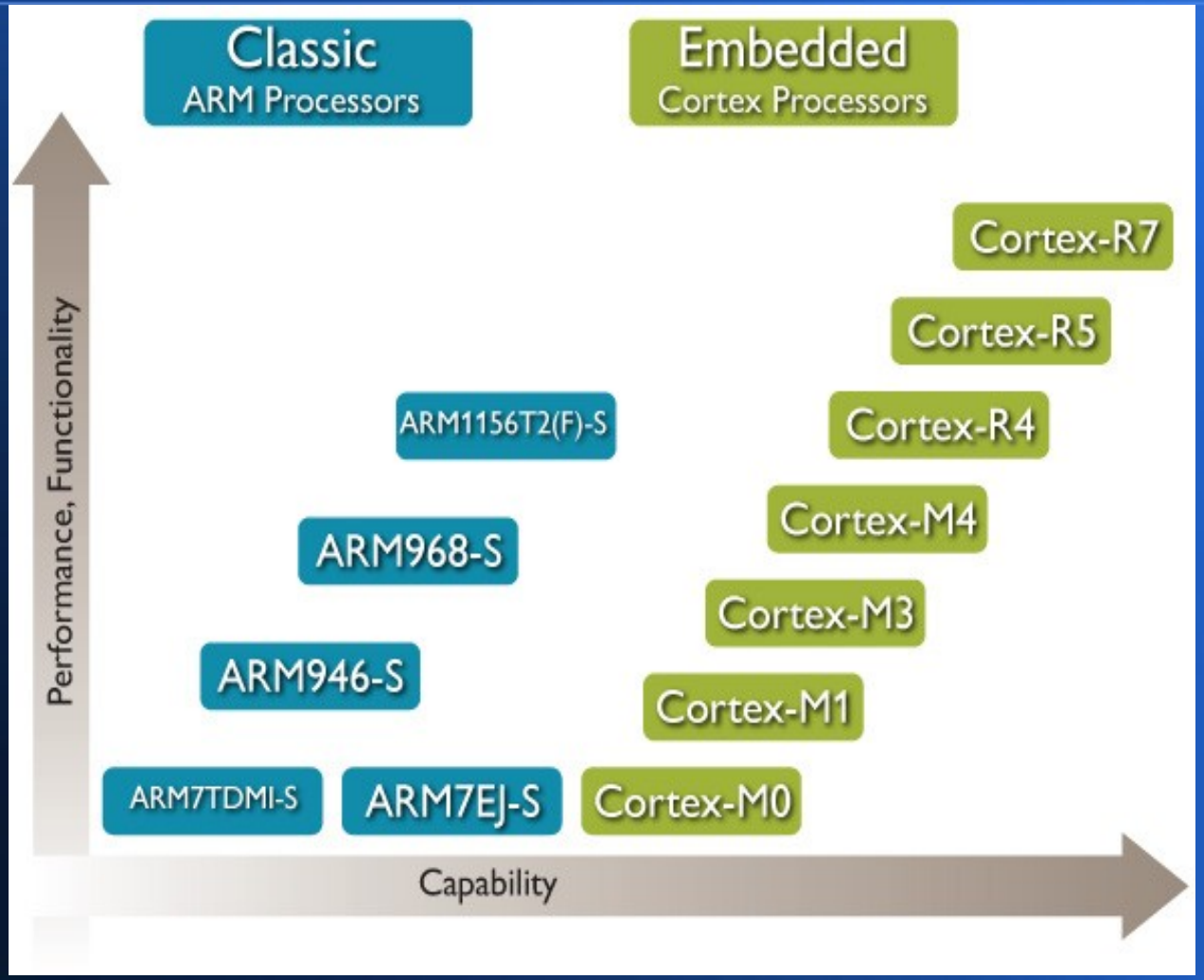
Advanced RISC Machines

- Primer diseño data de los 80's (ARMv1), actualmente existe la linea ARMv 6/7
- Basado en el 6502 (Commodore, MSX, Apple II, etc.)
- RISC
- Sin microcodigo (todo en logica convinacional)
- Target en procesadores embebidos
  - Application processor (Smart phones, HDTV)
  - Device processor (camaras, jugetes, etc.)
- No fabrica nada, licencia el nucleo a otros

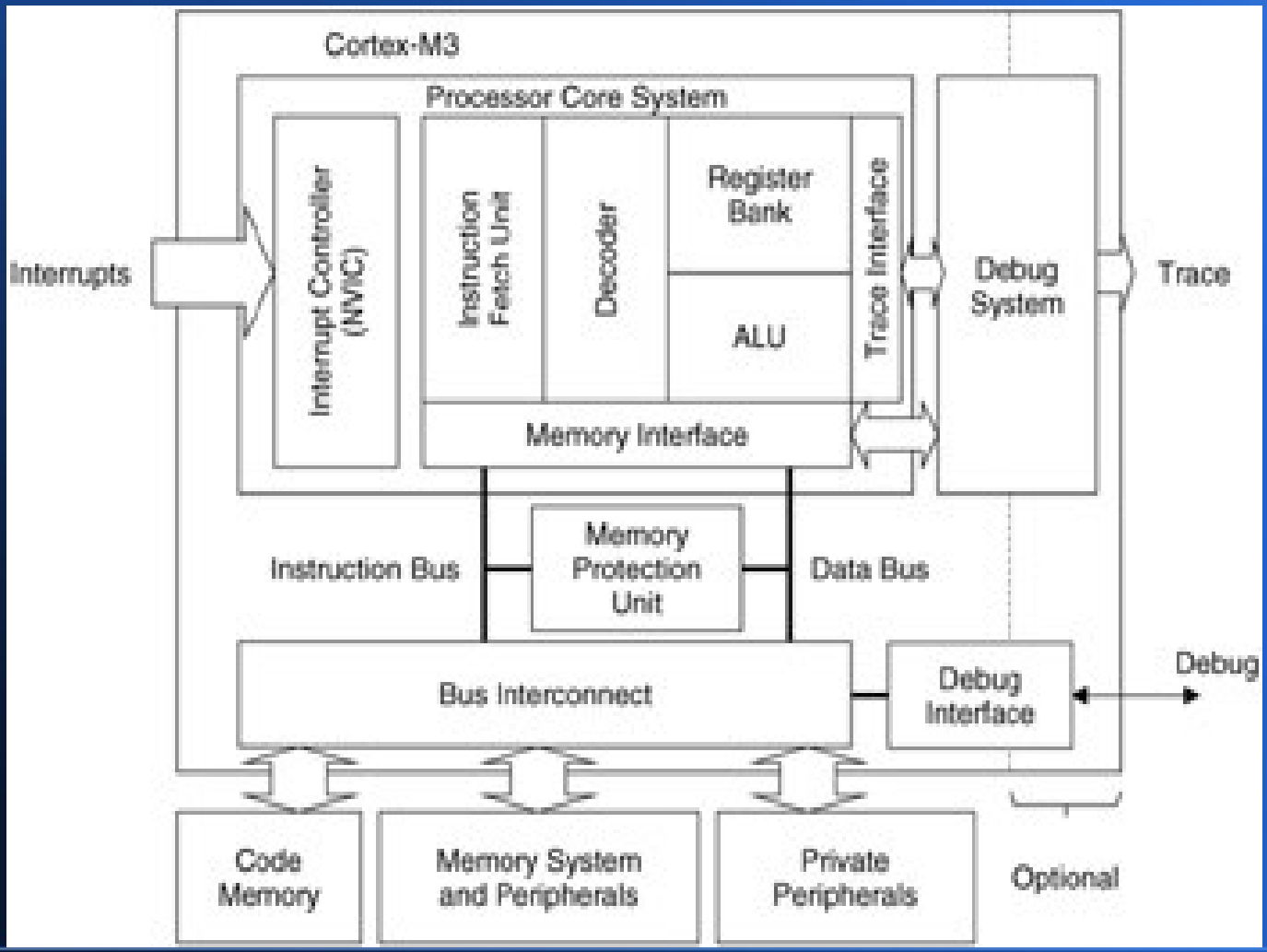
Advanced RISC Machines



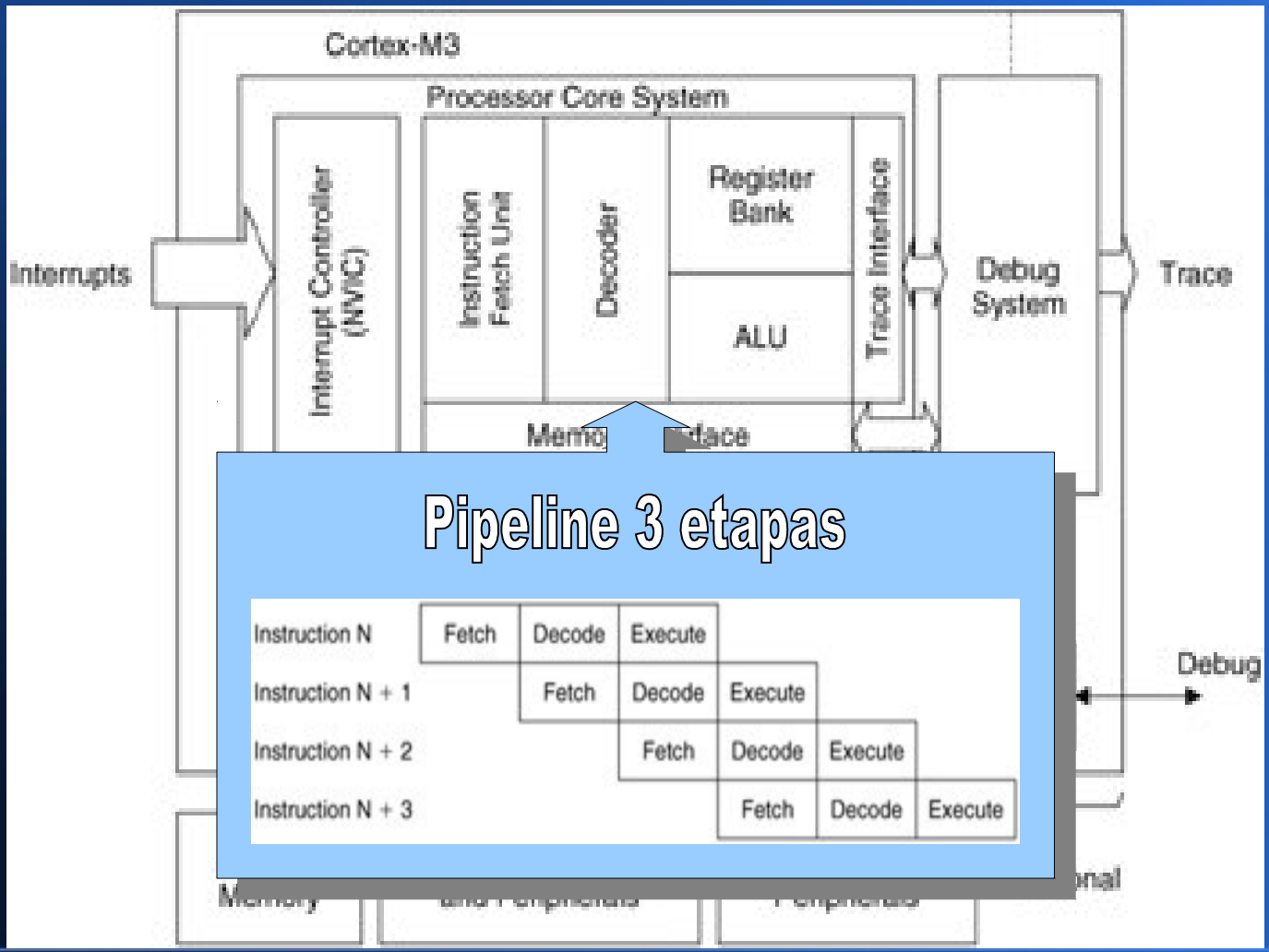
Cortex M Series



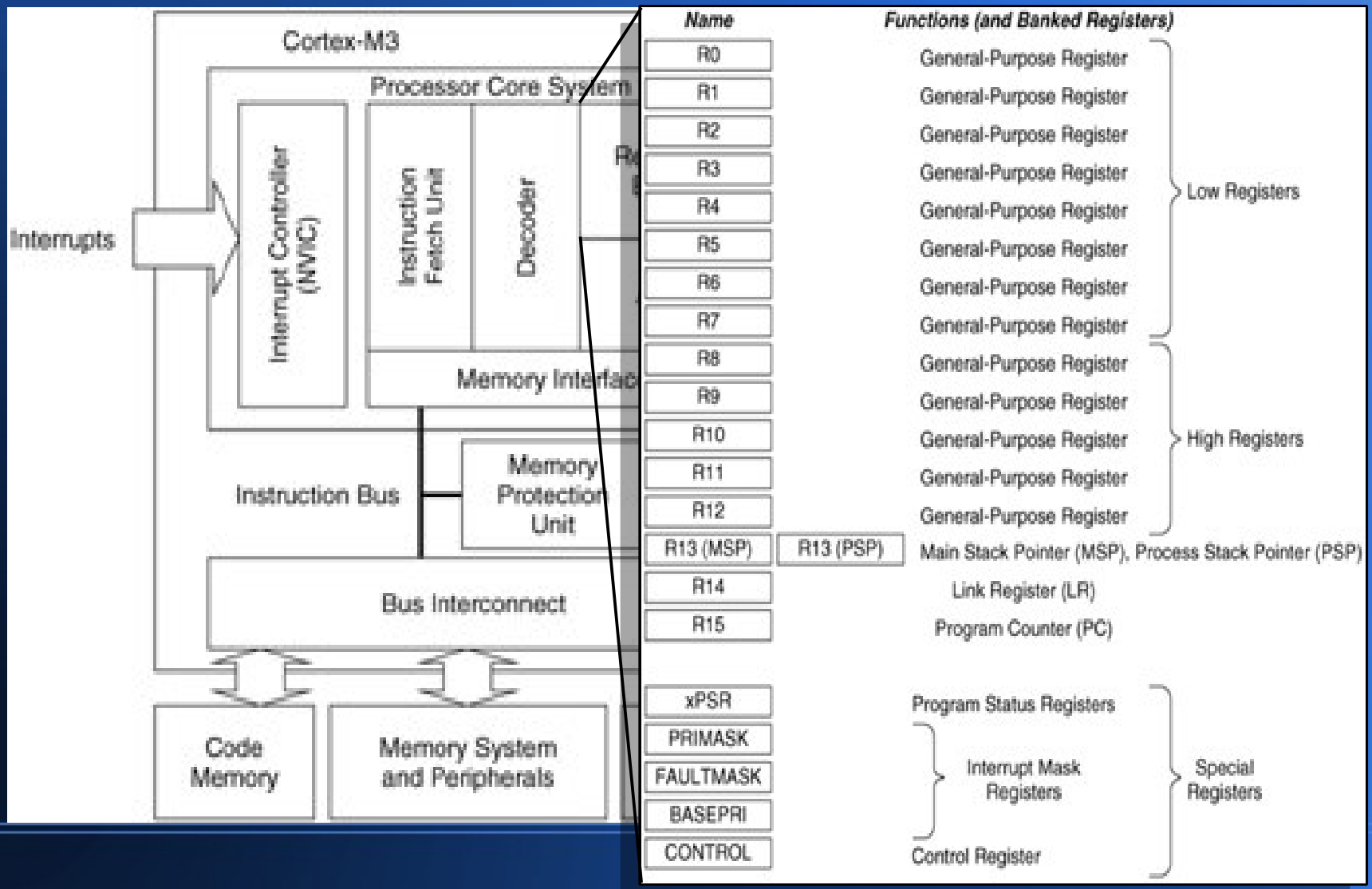
Cortex M Series



Cortex M Series



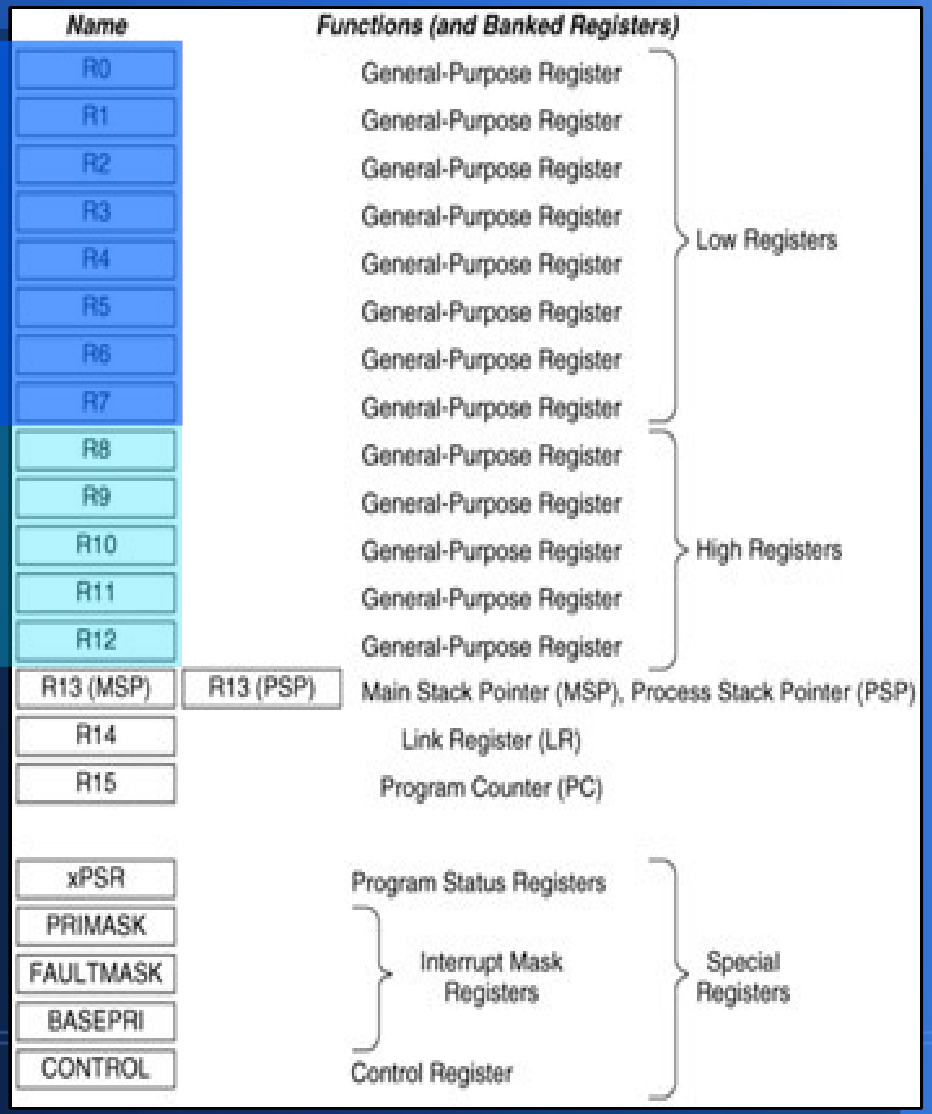
Cortex M Series



Cortex M Series

Registros de proposito general

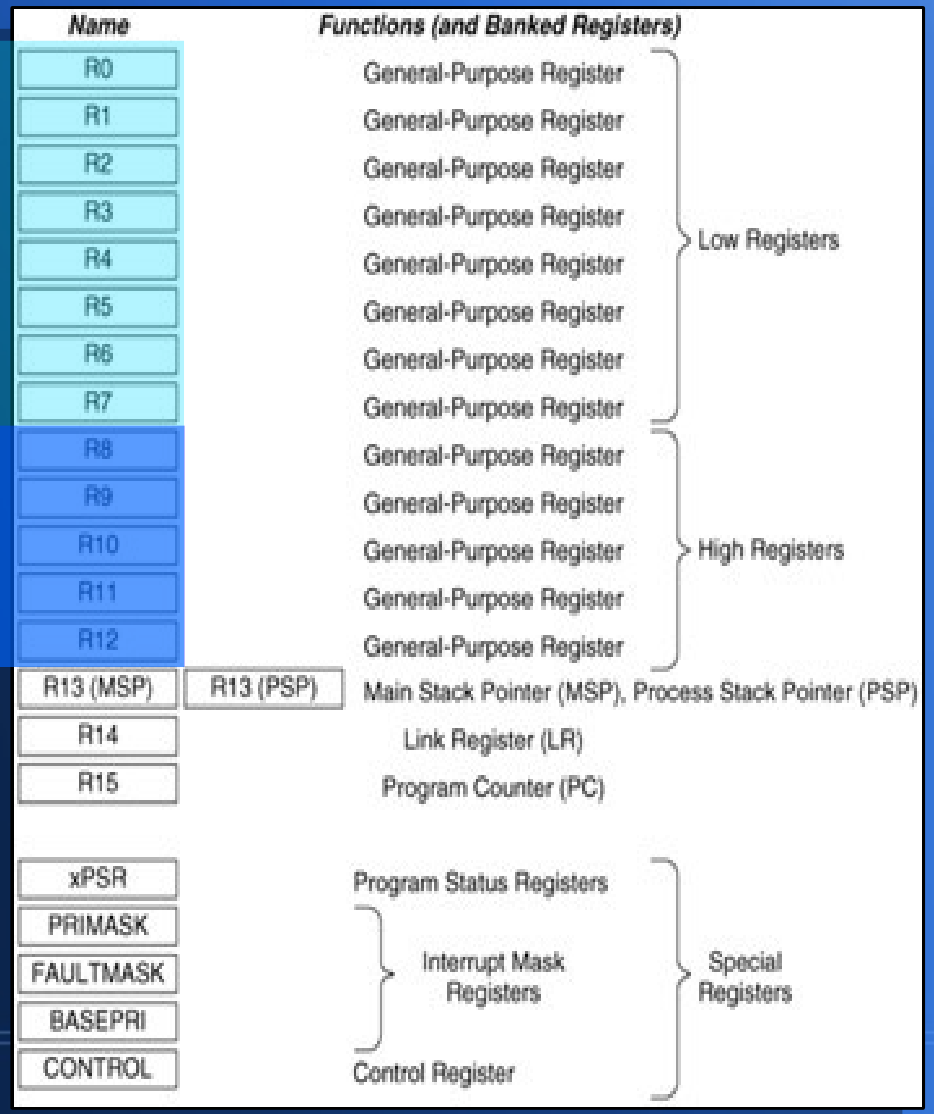
Ocho registros de proposito general accesibles por todas las instrucciones



Cortex M Series

Registros de proposito general

Cinco registros de proposito general accesibles por instrucciones extendidas



Cortex M Series

Código privilegiado

```
void serial_send(...) {
  SERIAL_BUF = ...;
  while(!serial_busy())
    ;
}
```

```
void print_led(int n) {
  PORTA = n<<8;
}
```

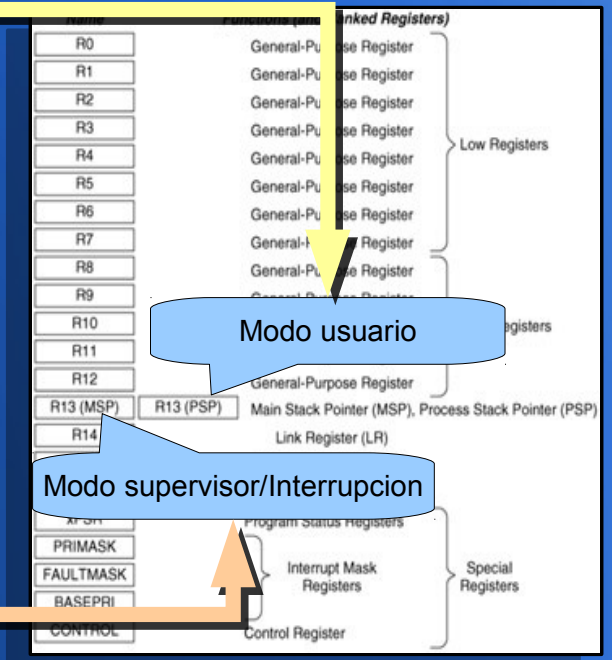
```
read_adc(void) {
  while(!adc_busy())
    ;
  return ADC_VAL;
}
```

Puertas de llamada

Código de aplicación

```
A = b + x;
serial_send("valor");
....
print_led(LED0);
...
V = read_adc()/2.2;
...
```

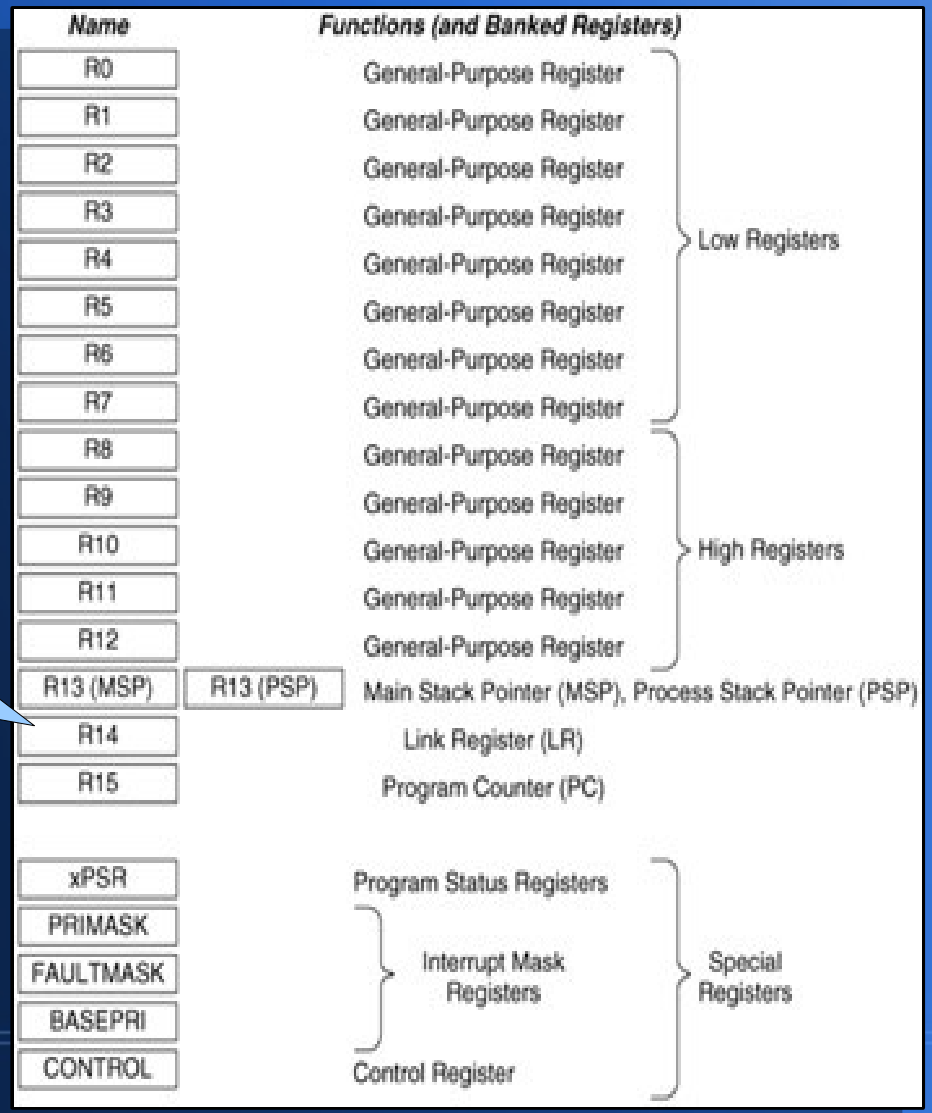
Usa



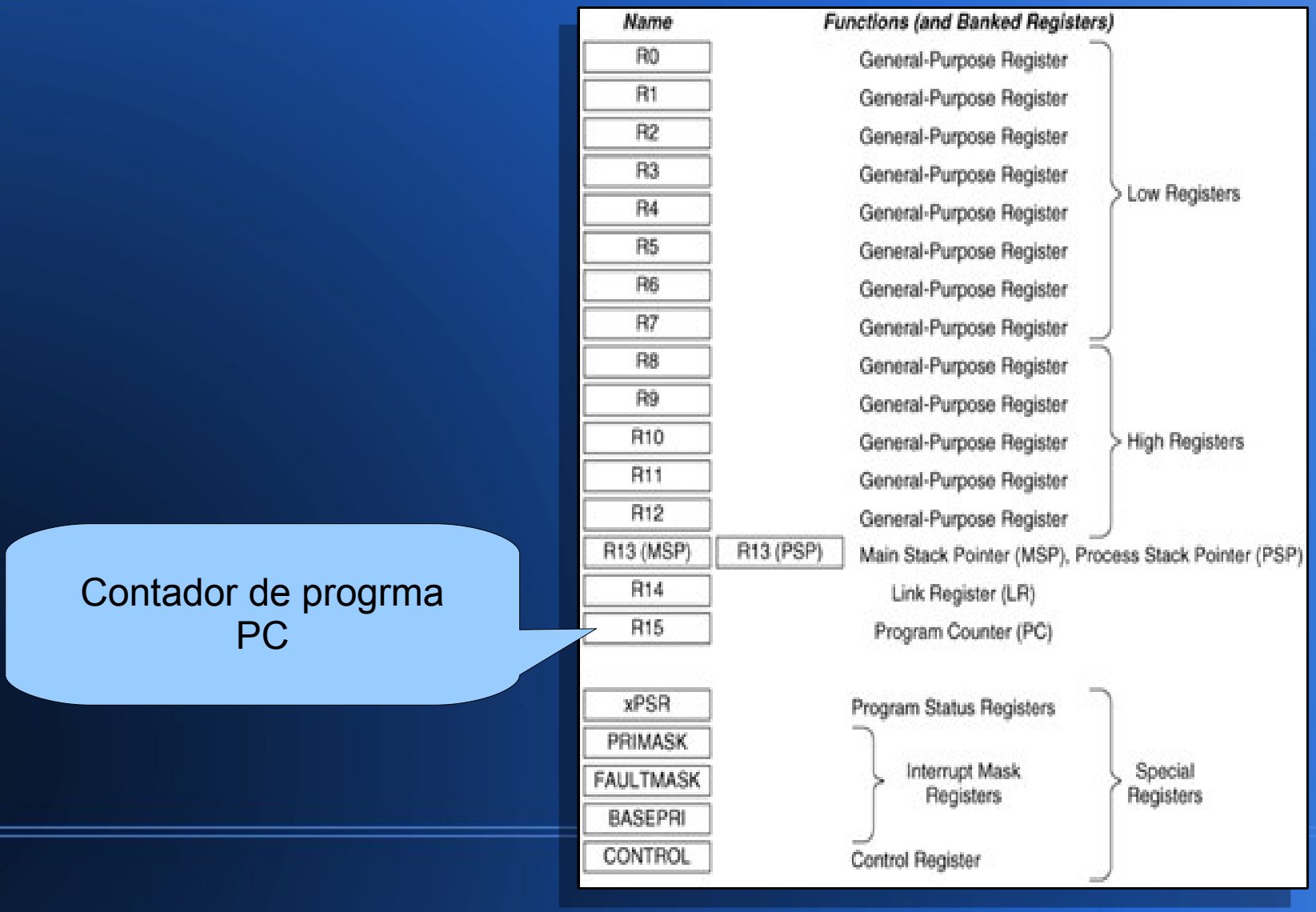
Usa

Cortex M Series

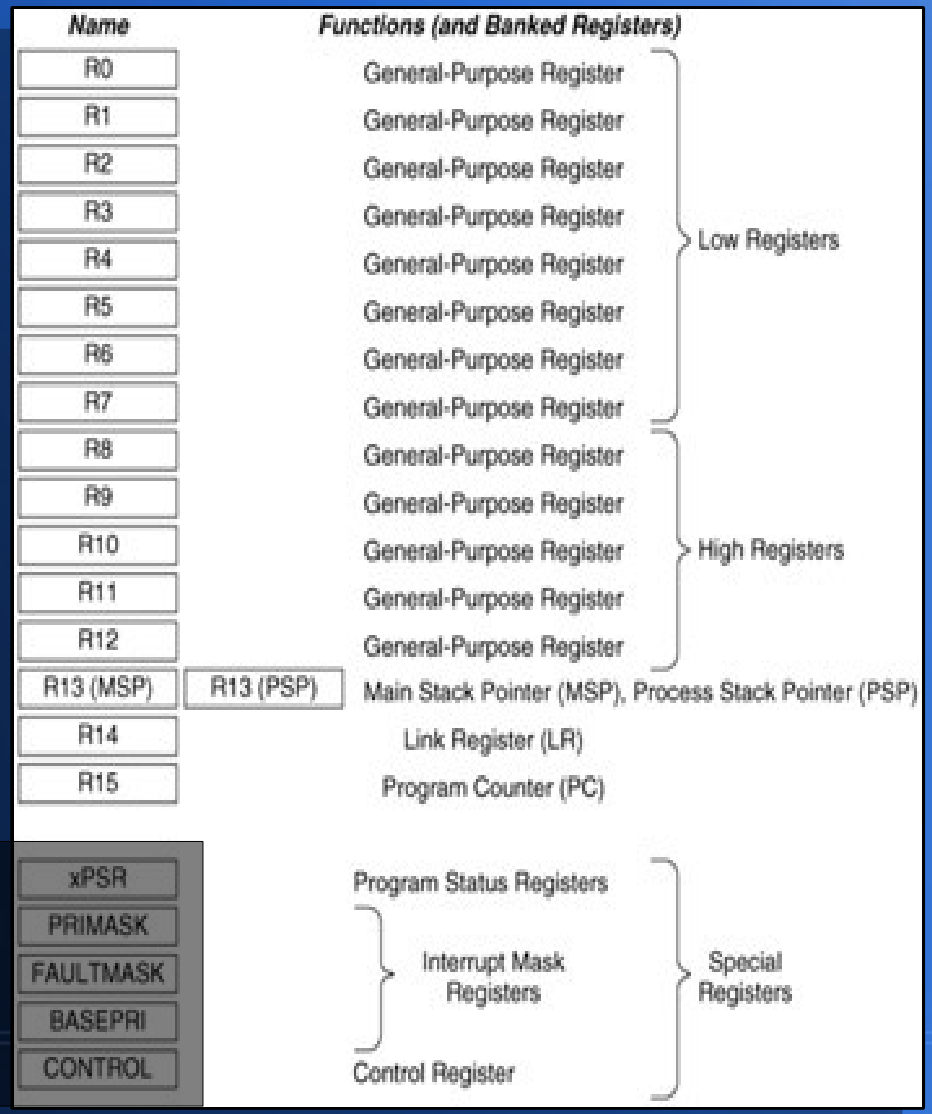
Usado par guardar PC en llamadas a subrutinas



Cortex M Series



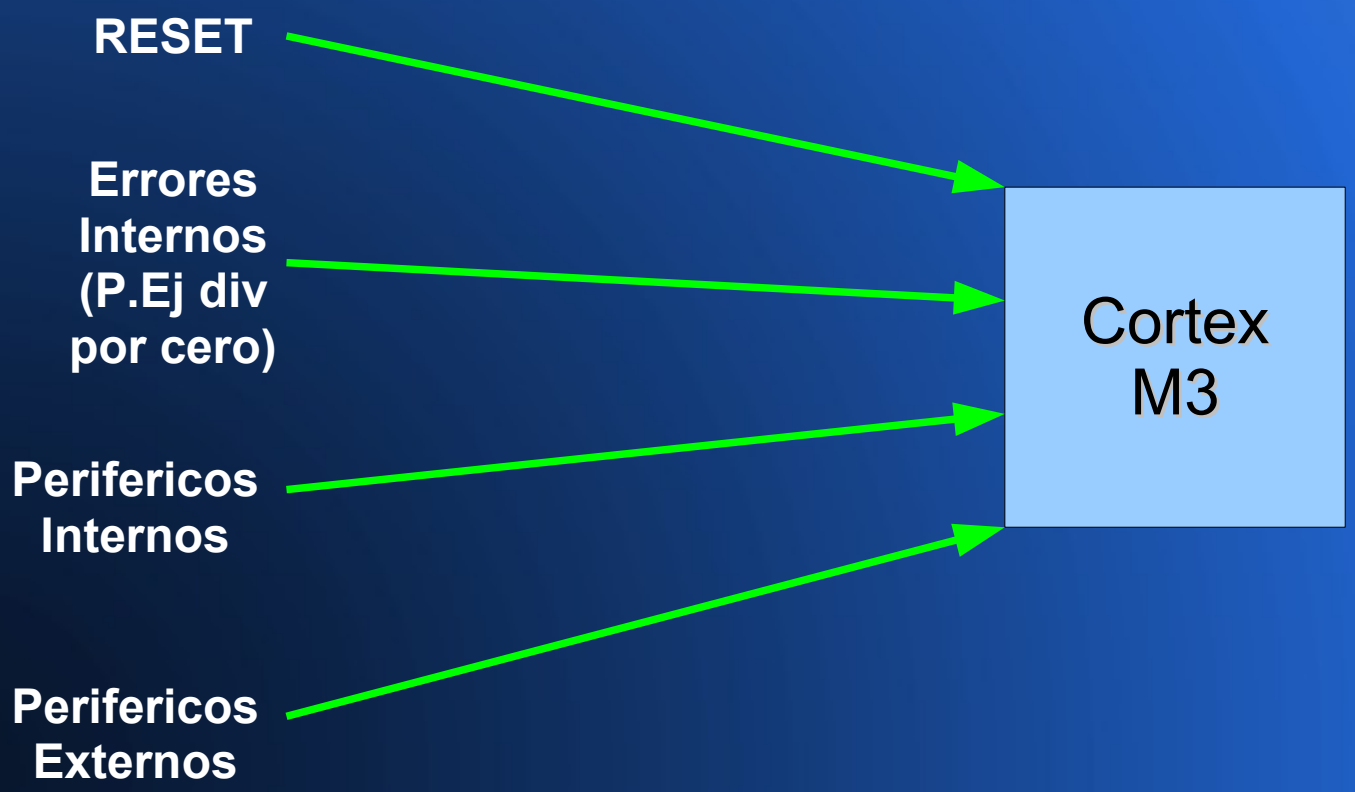
Cortex M Series



Registros de control
Accesibles por instrucciones privilegiadas

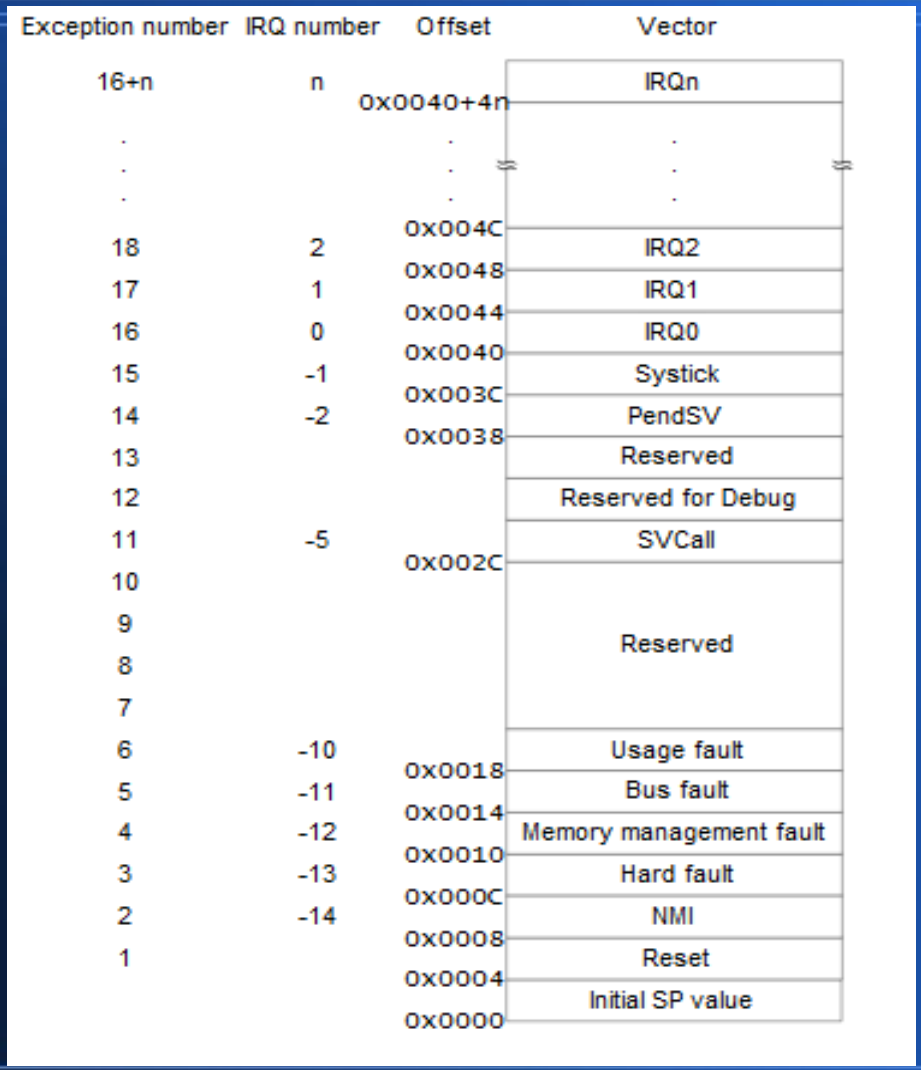
Cortex M Series

Interrupciones



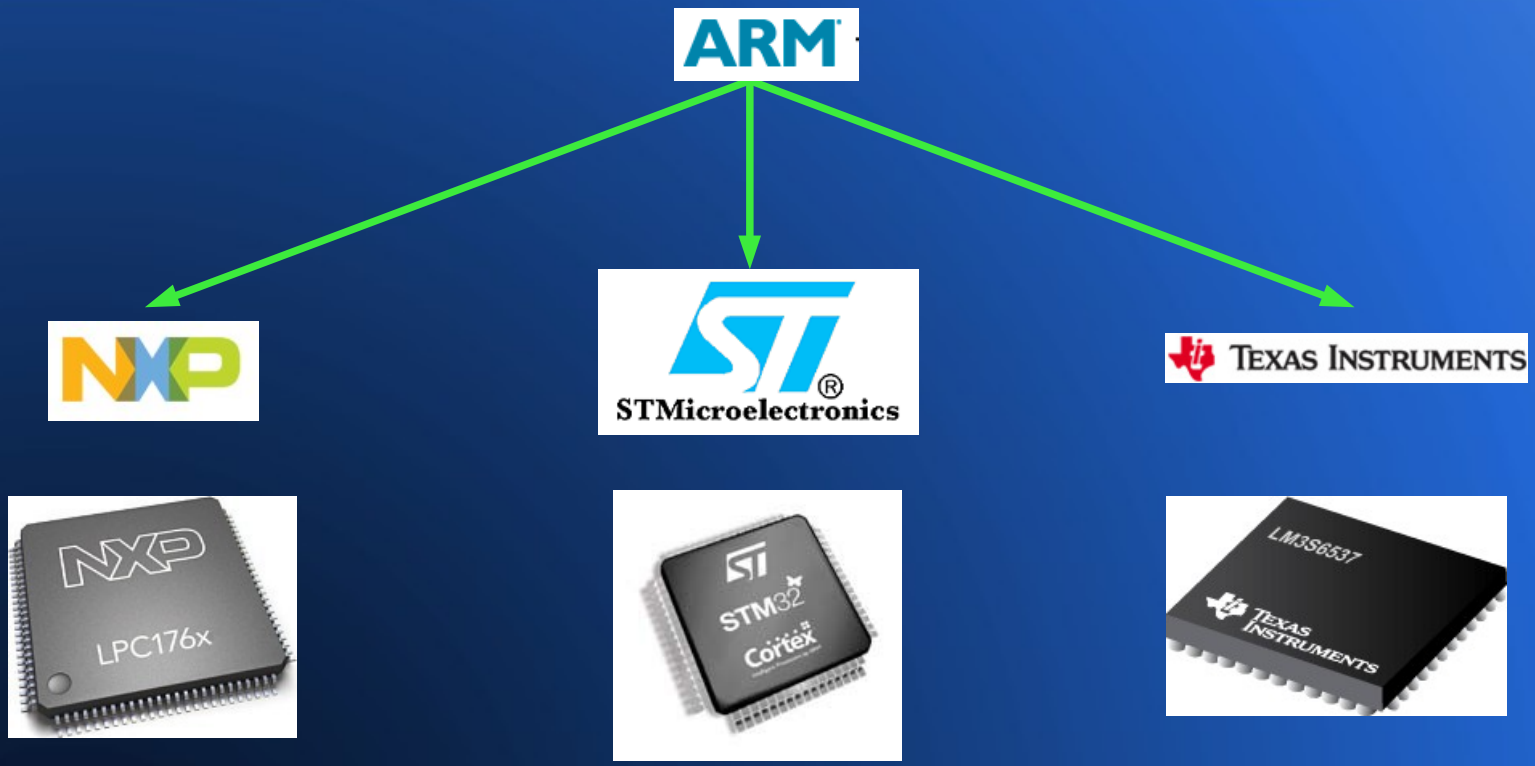
Cortex M Series

Interrupciones



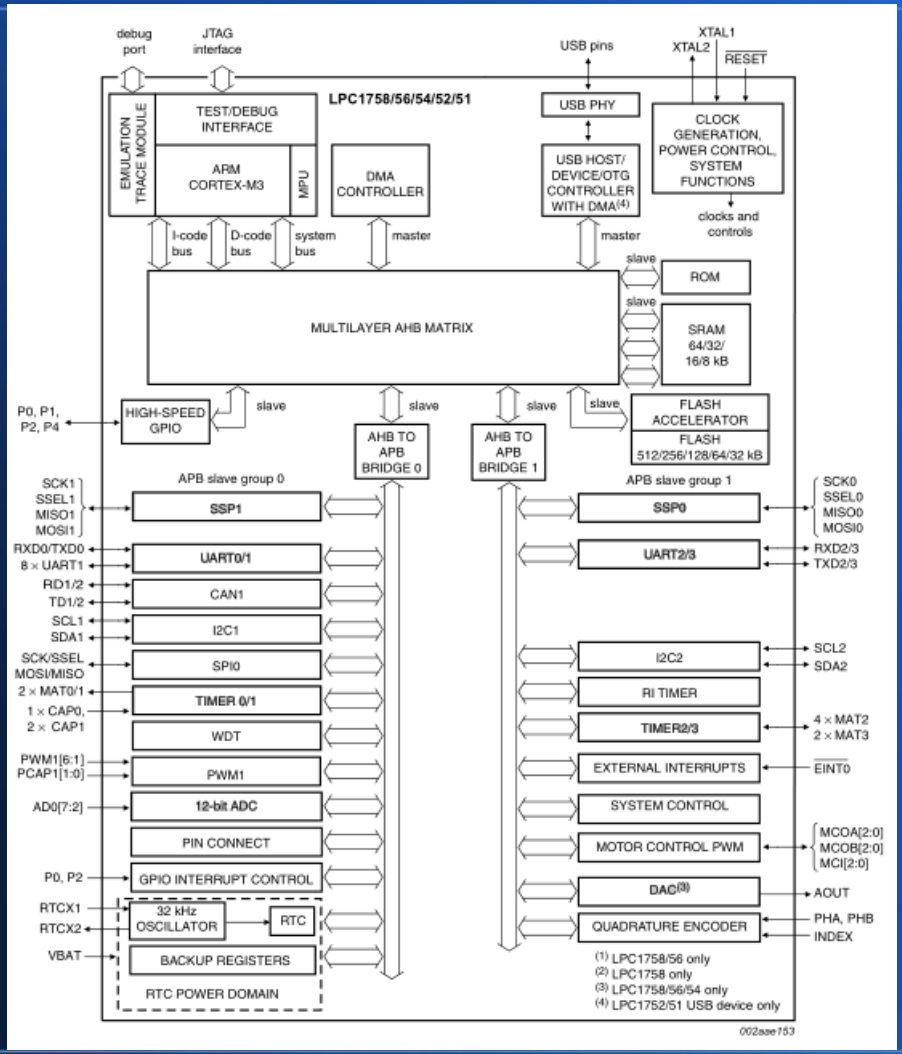
Exception number	IRQ number	Offset	Vector
16+n	n	0x0040+4n	IRQn
.	.	.	.
.	.	.	.
.	.	.	.
18	2	0x004C	IRQ2
17	1	0x0048	IRQ1
16	0	0x0044	IRQ0
15	-1	0x0040	Systick
14	-2	0x003C	PendSV
13		0x0038	Reserved
12			Reserved for Debug
11	-5		SVCall
10		0x002C	Reserved
9			
8			
7			
6	-10		Usage fault
5	-11	0x0018	Bus fault
4	-12	0x0014	Memory management fault
3	-13	0x0010	Hard fault
2	-14	0x000C	NMI
1		0x0008	Reset
		0x0004	Initial SP value
		0x0000	

Cortex M Series



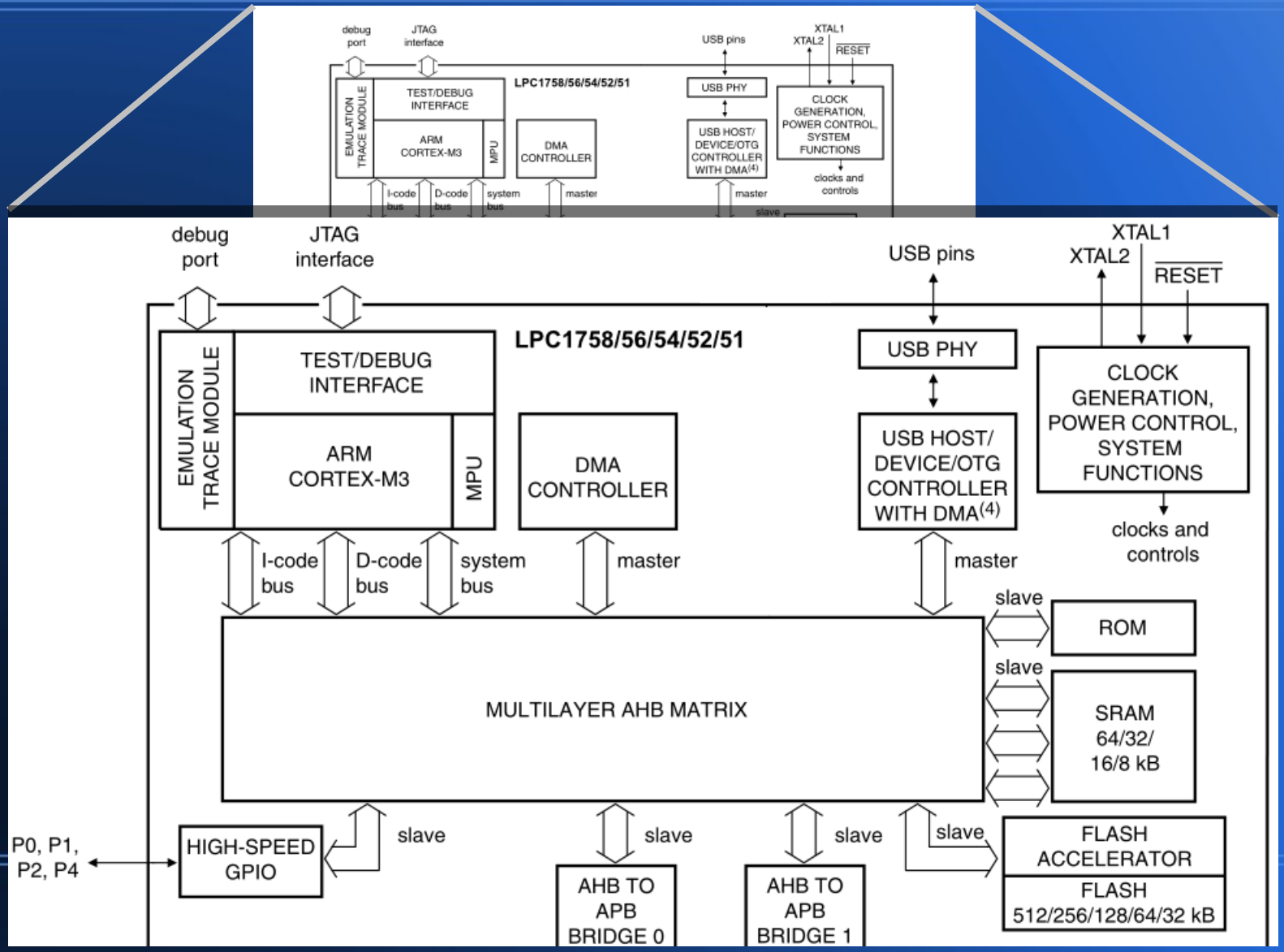
NXP LPC1754


NXP
LPC176x


debug port
JTAG interface
USB pins
XTAL1
XTAL2
RESET
LPC1758/56/54/52/51
EMULATION TRACE MODULE
TEST/DEBUG INTERFACE
ARM CORTEX-M3
MPU
DMA CONTROLLER
USB PHY
USB HOST/ DEVICE/OTG CONTROLLER WITH DMA(4)
CLOCK GENERATION, POWER CONTROL, SYSTEM FUNCTIONS
clocks and controls
I-code bus
D-code bus
system bus
master
master
slave
ROM
MULTILAYER AHB MATRIX
SRAM 64/32/ 16/8 kB
P0, P1, P2, P4
HIGH-SPEED GPIO
slave
slave
slave
slave
FLASH ACCELERATOR
FLASH 512/256/128/64/32 kB
AHB TO APB BRIDGE 0
AHB TO APB BRIDGE 1
APB slave group 0
APB slave group 1
SCK1
SSEL1
MISO1
MOSI1
SSP1
SSP0
SCK0
SSEL0
MISO0
MOSI0
RXD0/TXD0
8 × UART1
UART0/1
UART2/3
RXD2/3
TXD2/3
RD1/2
TD1/2
CAN1
SCL1
SDA1
I2C1
I2C2
SCL2
SDA2
SCK/SSEL
MOSI/MISO
SPI0
RI TIMER
2 × MAT0/1
TIMER 0/1
TIMER2/3
4 × MAT2
2 × MAT3
1 × CAP0,
2 × CAP1
WDT
PWM1[6:1]
PCAP1[1:0]
PWM1
EXTERNAL INTERRUPTS
EINT0
AD0[7:2]
12-bit ADC
SYSTEM CONTROL
PIN CONNECT
MOTOR CONTROL PWM
MCOA[2:0]
MCOB[2:0]
MCI[2:0]
P0, P2
GPIO INTERRUPT CONTROL
DAC(3)
AOUT
RTCX1
RTCX2
32 kHz OSCILLATOR
RTC
QUADRATURE ENCODER
PHA, PHB
INDEX
VBAT
BACKUP REGISTERS
RTC POWER DOMAIN
(1) LPC1758/56 only
(2) LPC1758 only
(3) LPC1758/56/54 only
(4) LPC1752/51 USB device only
002aae153

NXP LPC1754


NXP
LPC176x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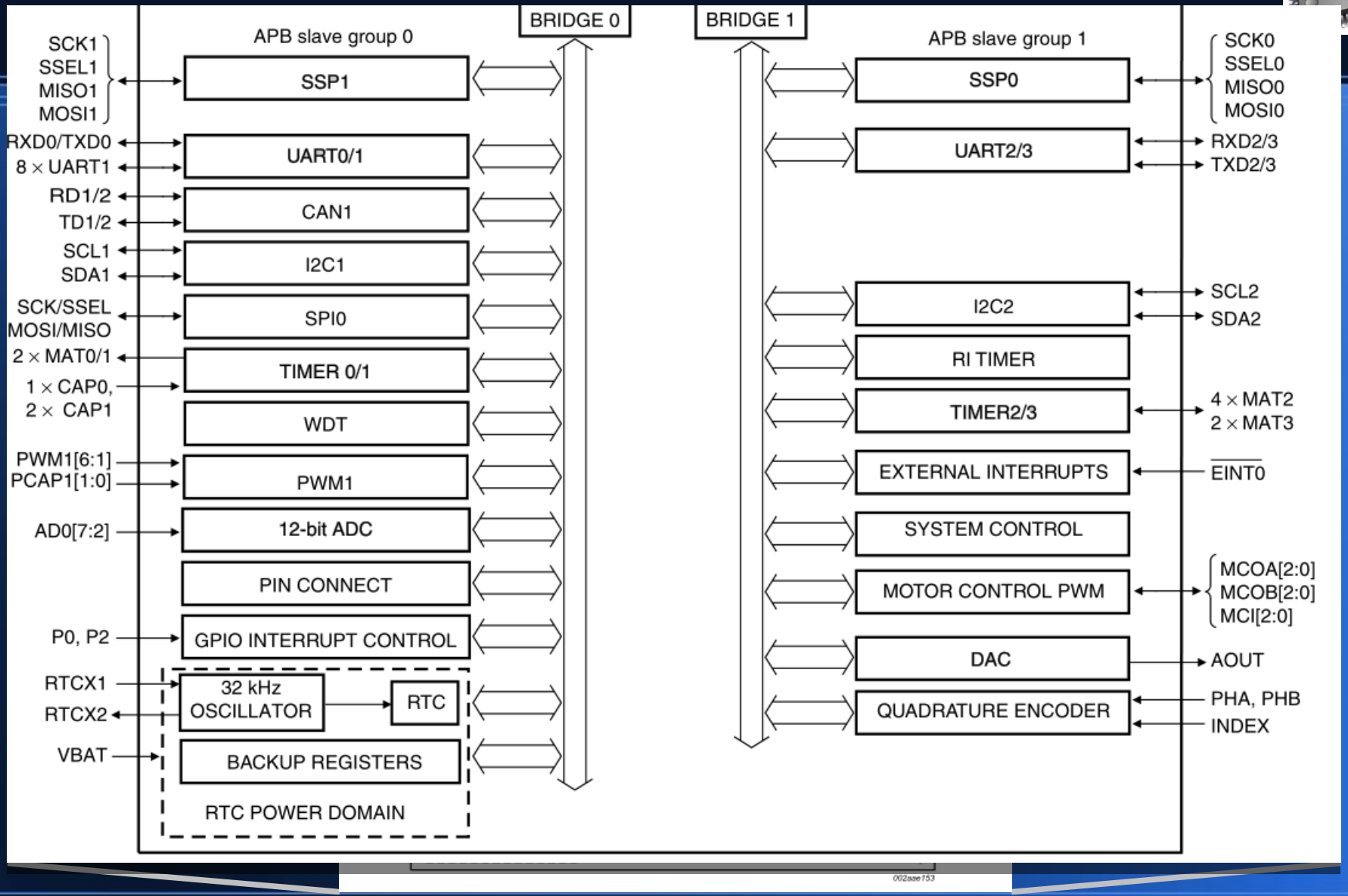
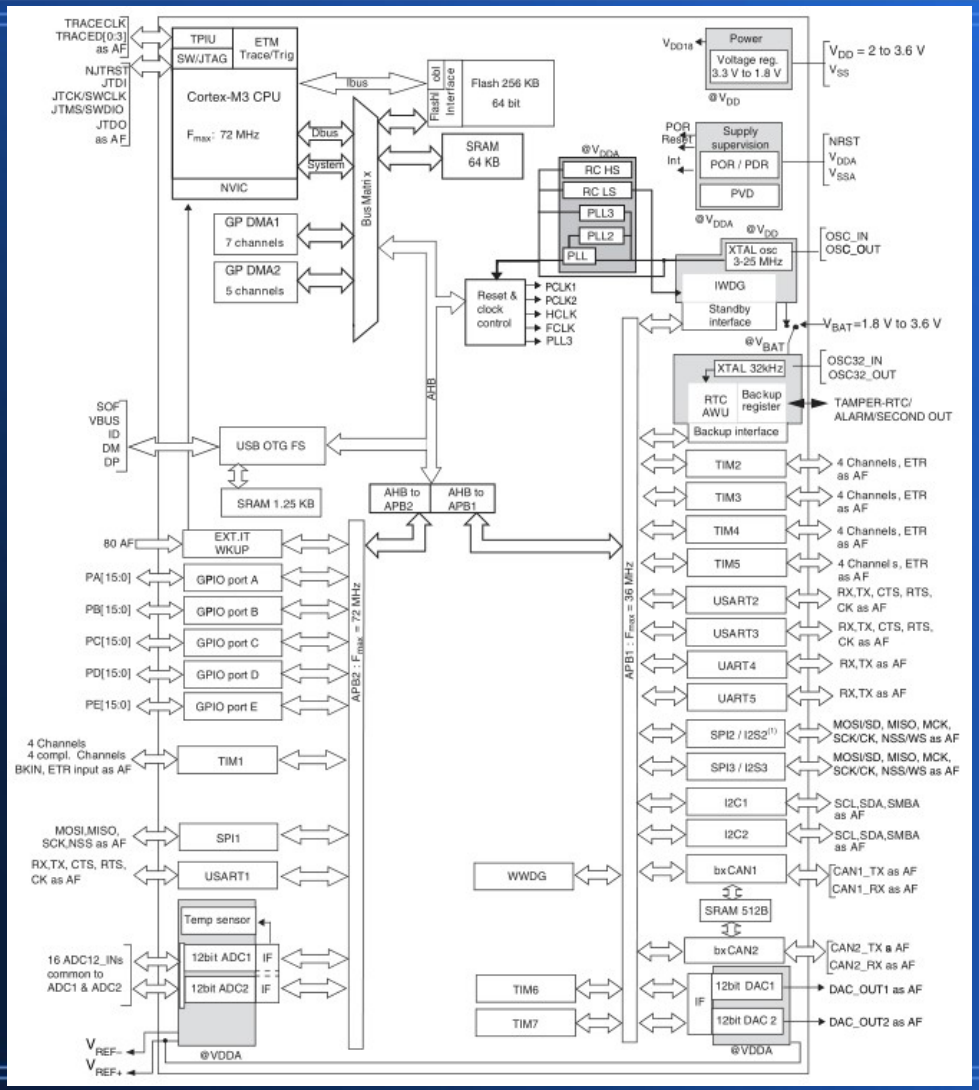
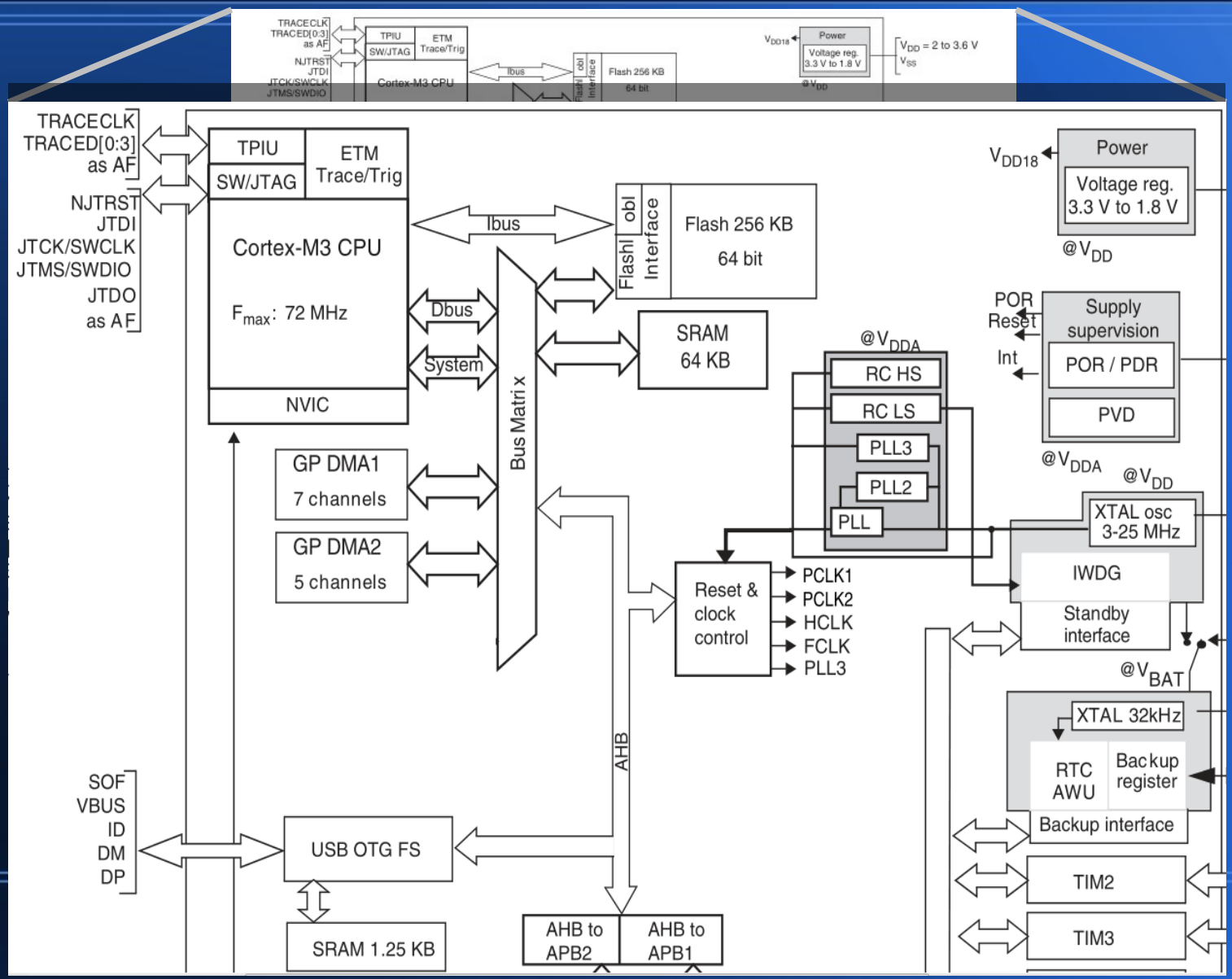

BRIDGE 0
BRIDGE 1
APB slave group 0
APB slave group 1
SCK1
SSEL1
MISO1
MOSI1
SSP1
SSP0
SCK0
SSEL0
MISO0
MOSI0
RXD0/TXD0
8 × UART1
UART0/1
UART2/3
RXD2/3
TXD2/3
RD1/2
TD1/2
CAN1
SCL1
SDA1
I2C1
I2C2
SCL2
SDA2
SCK/SSEL
MOSI/MISO
SPI0
2 × MAT0/1
TIMER 0/1
RI TIMER
1 × CAP0,
2 × CAP1
WDT
TIMER2/3
4 × MAT2
2 × MAT3
PWM1[6:1]
PCAP1[1:0]
PWM1
EXTERNAL INTERRUPTS
EINT0
AD0[7:2]
12-bit ADC
SYSTEM CONTROL
PIN CONNECT
MOTOR CONTROL PWM
MCOA[2:0]
MCOB[2:0]
MCI[2:0]
P0, P2
GPIO INTERRUPT CONTROL
DAC
AOUT
RTCX1
RTCX2
32 kHz
OSCILLATOR
RTC
QUADRATURE ENCODER
PHA, PHB
INDEX
VBAT
BACKUP REGISTERS
RTC POWER DOMAIN
002aae153

STMicroelectronics

STM32F105

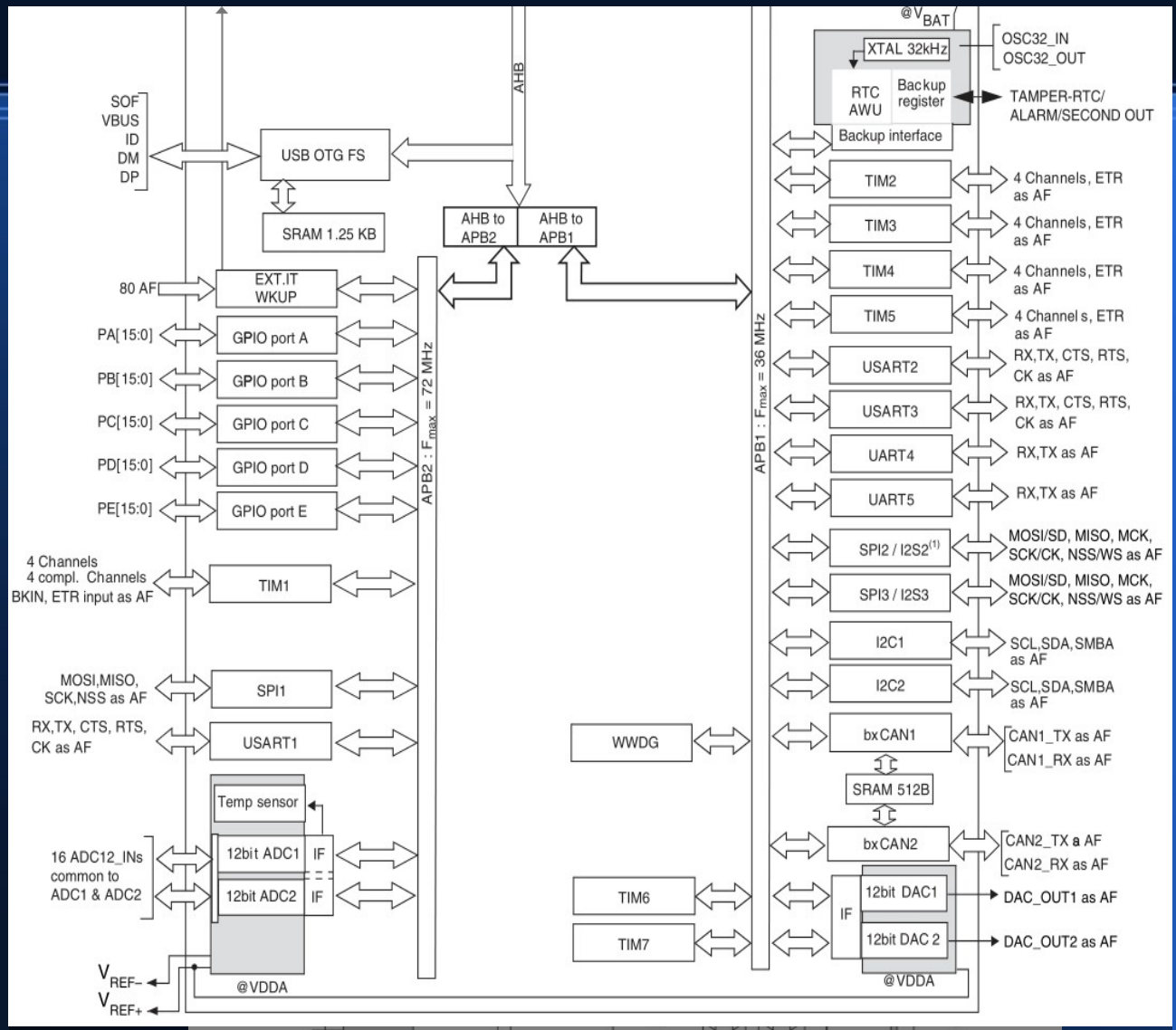


STM32F105


TRACECLK
TRACED[0:3]
as AF
NJTRST
JTDI
JTCK/SWCLK
JTMS/SWDIO
JTDO
as AF
TPIU
SW/JTAG
ETM
Trace/Trig
Cortex-M3 CPU
Fmax: 72 MHz
NVIC
Ibus
Dbus
System
Flash 256 KB
64 bit
obl
Flashl Interface
SRAM
64 KB
Bus Matrix
GP DMA1
7 channels
GP DMA2
5 channels
VDD18
Power
Voltage reg.
3.3 V to 1.8 V
@VDD
POR
Reset
Int
Supply
supervision
POR / PDR
PVD
@VDDA
RC HS
RC LS
PLL3
PLL2
PLL
XTAL osc
3-25 MHz
IWDG
Standby
interface
@VBAT
XTAL 32kHz
RTC
AWU
Backup
register
Backup interface
Reset &
clock
control
PCLK1
PCLK2
HCLK
FCLK
PLL3
AHB
SOF
VBUS
ID
DM
DP
USB OTG FS
SRAM 1.25 KB
AHB to
APB2
AHB to
APB1
TIM2
TIM3

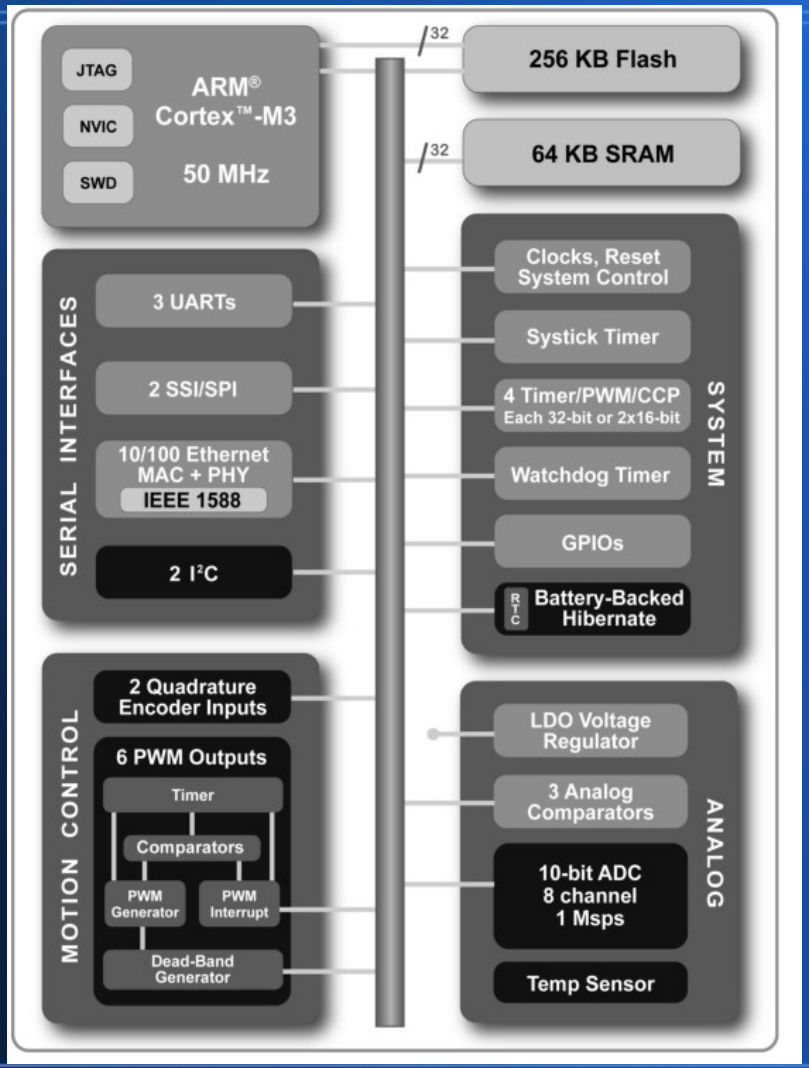
STMicroelectronics

STM32F105



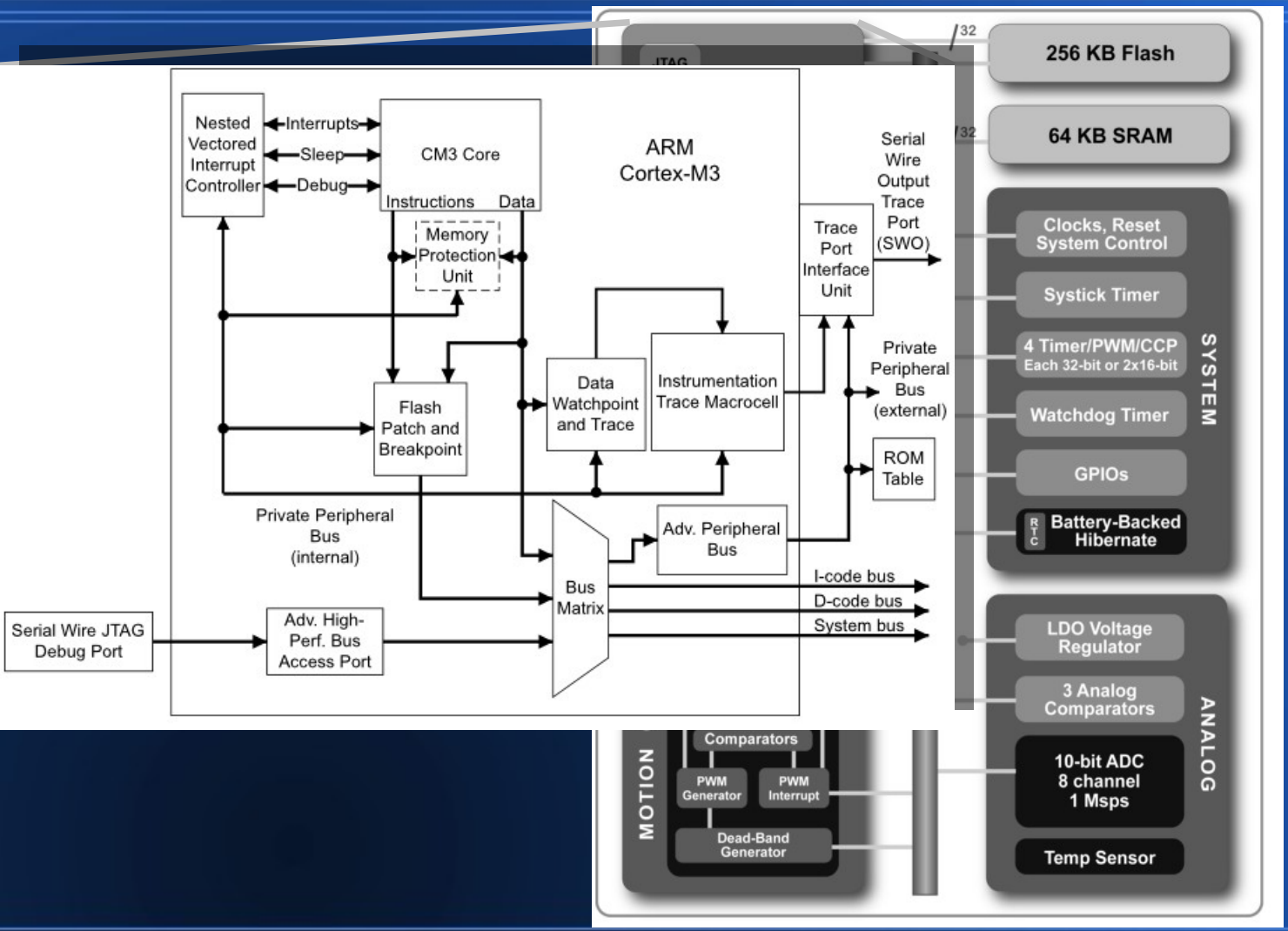
LM3S6537


LM3S6537
Texas Instruments


JTAG
NVIC
SWD
ARM® Cortex™-M3
50 MHz
32
256 KB Flash
32
64 KB SRAM
SERIAL INTERFACES
3 UARTs
2 SSI/SPI
10/100 Ethernet MAC + PHY
IEEE 1588
2 I²C
SYSTEM
Clocks, Reset System Control
Systick Timer
4 Timer/PWM/CCP
Each 32-bit or 2x16-bit
Watchdog Timer
GPIOs
RTC
Battery-Backed Hibernate
MOTION CONTROL
2 Quadrature Encoder Inputs
6 PWM Outputs
Timer
Comparators
PWM Generator
PWM Interrupt
Dead-Band Generator
ANALOG
LDO Voltage Regulator
3 Analog Comparators
10-bit ADC
8 channel
1 Msps
Temp Sensor

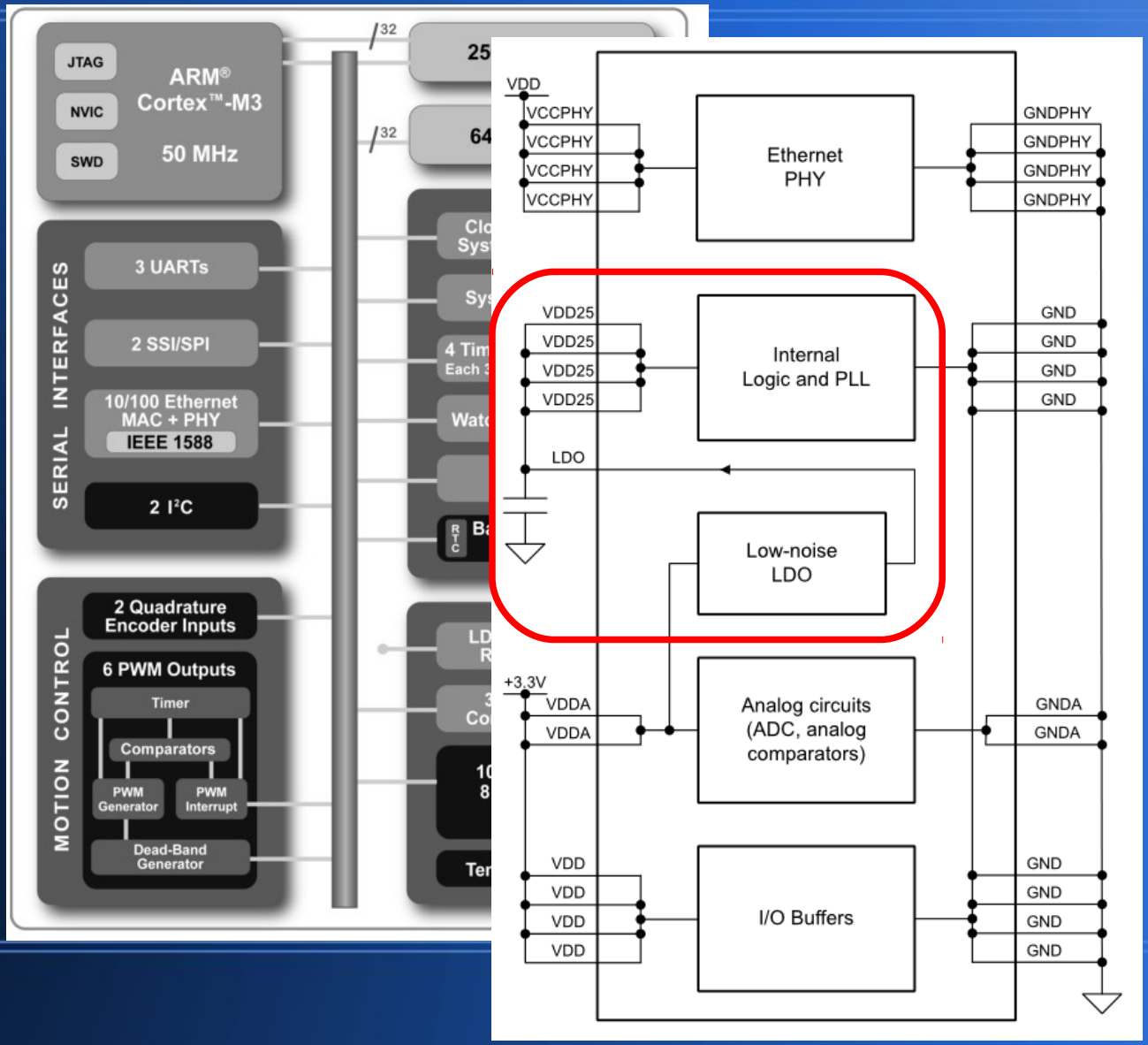
LM3S6537


LM3S6537
Texas Instruments


Nested Vectored Interrupt Controller
Interrupts
Sleep
Debug
CM3 Core
Instructions
Data
ARM Cortex-M3
Memory Protection Unit
Flash Patch and Breakpoint
Data Watchpoint and Trace
Instrumentation Trace Macrocell
Trace Port Interface Unit
Serial Wire Output Trace Port (SWO)
Private Peripheral Bus (external)
ROM Table
Private Peripheral Bus (internal)
Adv. Peripheral Bus
Bus Matrix
I-code bus
D-code bus
System bus
Serial Wire JTAG Debug Port
Adv. High-Perf. Bus Access Port
32
256 KB Flash
32
64 KB SRAM
SYSTEM
Clocks, Reset System Control
Systick Timer
4 Timer/PWM/CCP
Each 32-bit or 2x16-bit
Watchdog Timer
GPIOs
RTC
Battery-Backed Hibernate
ANALOG
LDO Voltage Regulator
3 Analog Comparators
10-bit ADC
8 channel
1 Msps
Temp Sensor
MOTION
Comparators
PWM Generator
PWM Interrupt
Dead-Band Generator

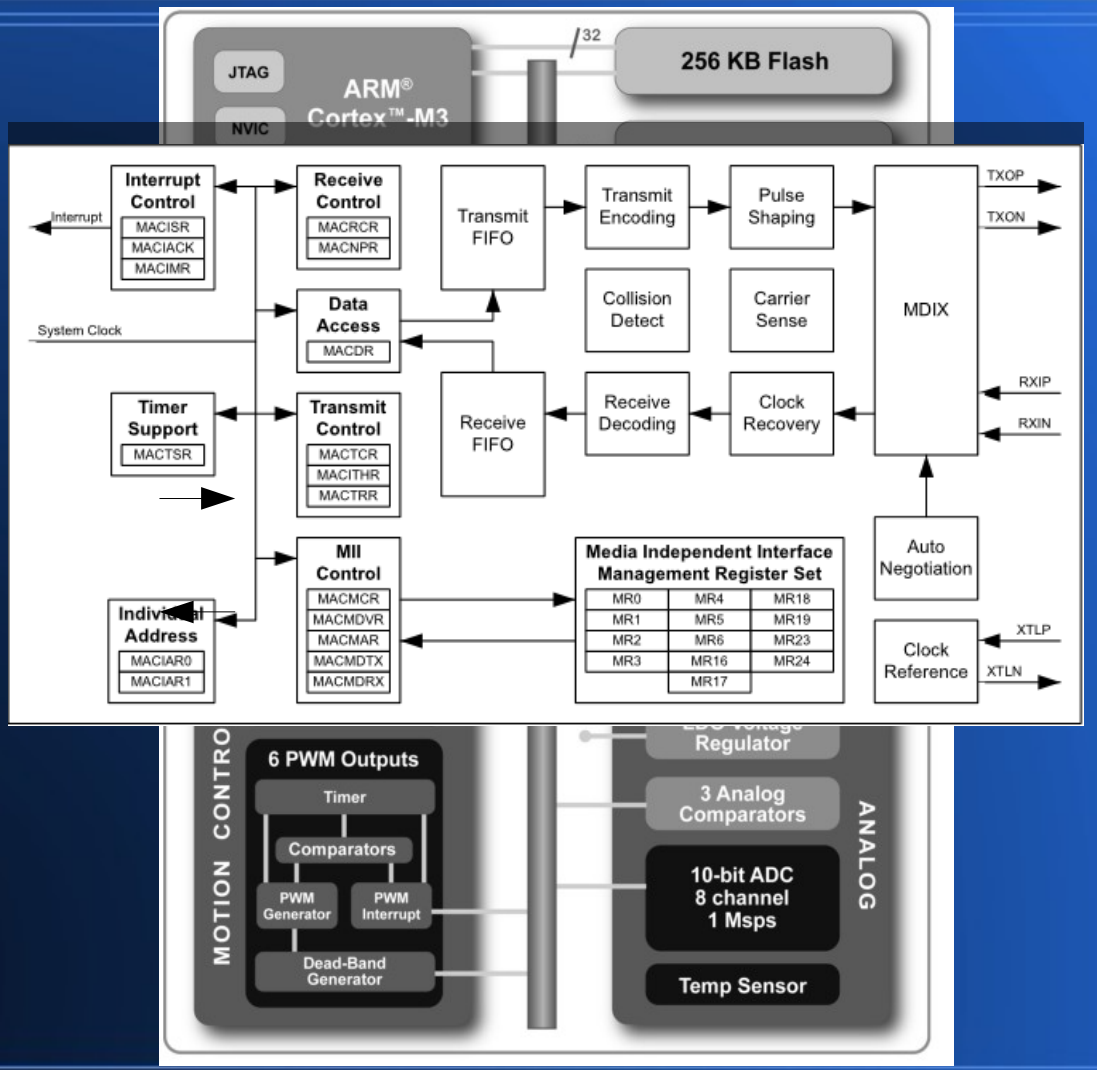
LM3S6537


LM3S6537
Texas Instruments


JTAG
NVIC
SWD
ARM® Cortex™-M3
50 MHz
32
32
SERIAL INTERFACES
3 UARTs
2 SSI/SPI
10/100 Ethernet MAC + PHY
IEEE 1588
2 I²C
MOTION CONTROL
2 Quadrature Encoder Inputs
6 PWM Outputs
Timer
Comparators
PWM Generator
PWM Interrupt
Dead-Band Generator
VDD
VCCPHY
VCCPHY
VCCPHY
VCCPHY
Ethernet PHY
GNDPHY
GNDPHY
GNDPHY
GNDPHY
VDD25
VDD25
VDD25
VDD25
Internal Logic and PLL
GND
GND
GND
GND
LDO
Low-noise LDO
+3.3V
VDDA
VDDA
Analog circuits (ADC, analog comparators)
GNDA
GNDA
VDD
VDD
VDD
VDD
I/O Buffers
GND
GND
GND
GND

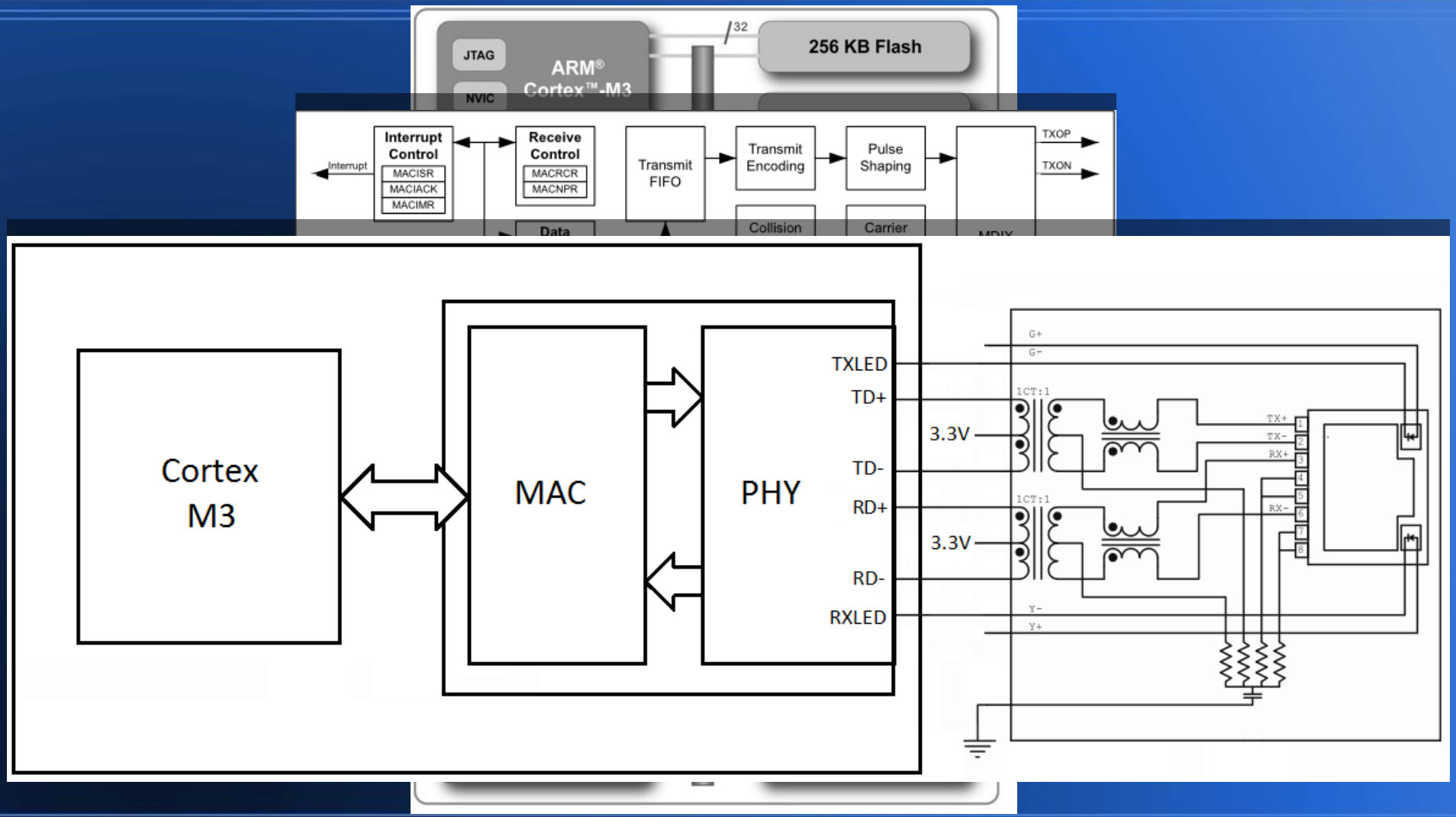
LM3S6537


LM3S6537
Texas Instruments

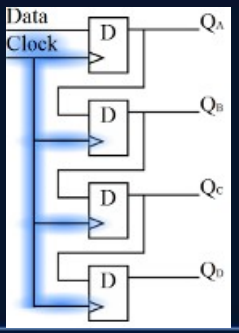

JTAG
NVIC
ARM® Cortex™-M3
32
256 KB Flash
Interrupt Control
MACISR
MACIACK
MACIMR
Interrupt
System Clock
Receive Control
MACRCR
MACNPR
Data Access
MACDR
Transmit Control
MACTCR
MACITHR
MACTRR
Timer Support
MACTSR
Individual Address
MACIAR0
MACIAR1
MII Control
MACMCR
MACMDVR
MACMAR
MACMDTX
MACMDRX
Transmit FIFO
Receive FIFO
Transmit Encoding
Receive Decoding
Collision Detect
Clock Recovery
Carrier Sense
Pulse Shaping
MDIX
TXOP
TXON
RXIP
RXIN
Auto Negotiation
Clock Reference
XTLP
XTLN
Media Independent Interface Management Register Set
MR0
MR1
MR2
MR3
MR4
MR5
MR6
MR16
MR17
MR18
MR19
MR23
MR24
MOTION CONTRO
6 PWM Outputs
Timer
Comparators
PWM Generator
PWM Interrupt
Dead-Band Generator
Regulator
3 Analog Comparators
10-bit ADC 8 channel 1 Msps
Temp Sensor
ANALOG

LM3S6537

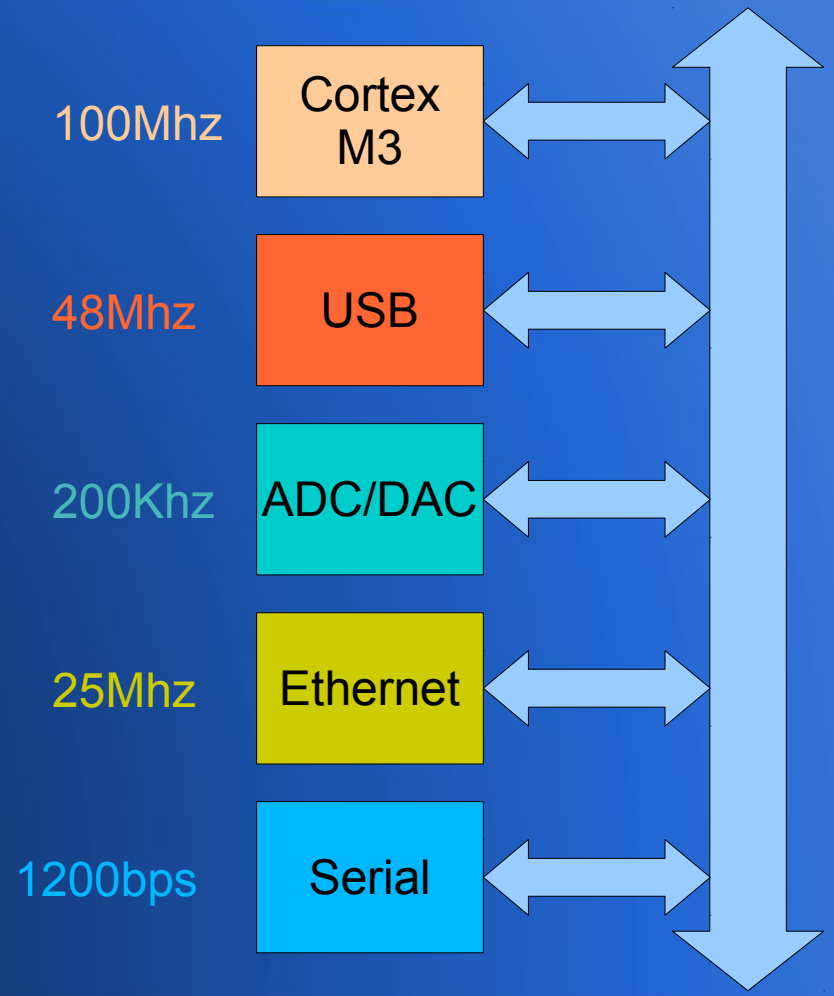

LM3S6537
Texas Instruments


JTAG
NVIC
ARM® Cortex™-M3
32
256 KB Flash
Interrupt
Interrupt Control
MACISR
MACIACK
MACIMR
Receive Control
MACRCR
MACNPR
Transmit FIFO
Transmit Encoding
Pulse Shaping
TXOP
TXON
Collision
Carrier
Data
Cortex M3
MAC
PHY
TXLED
TD+
TD-
RD+
RD-
RXLED
3.3V
3.3V
1CT:1
1CT:1
G+
G-
Y-
Y+
TX+
TX-
RX+
RX-

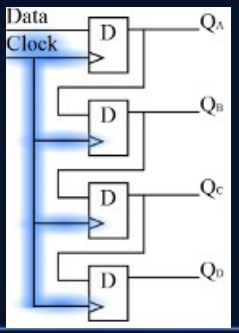
Cortex M3 Clocks



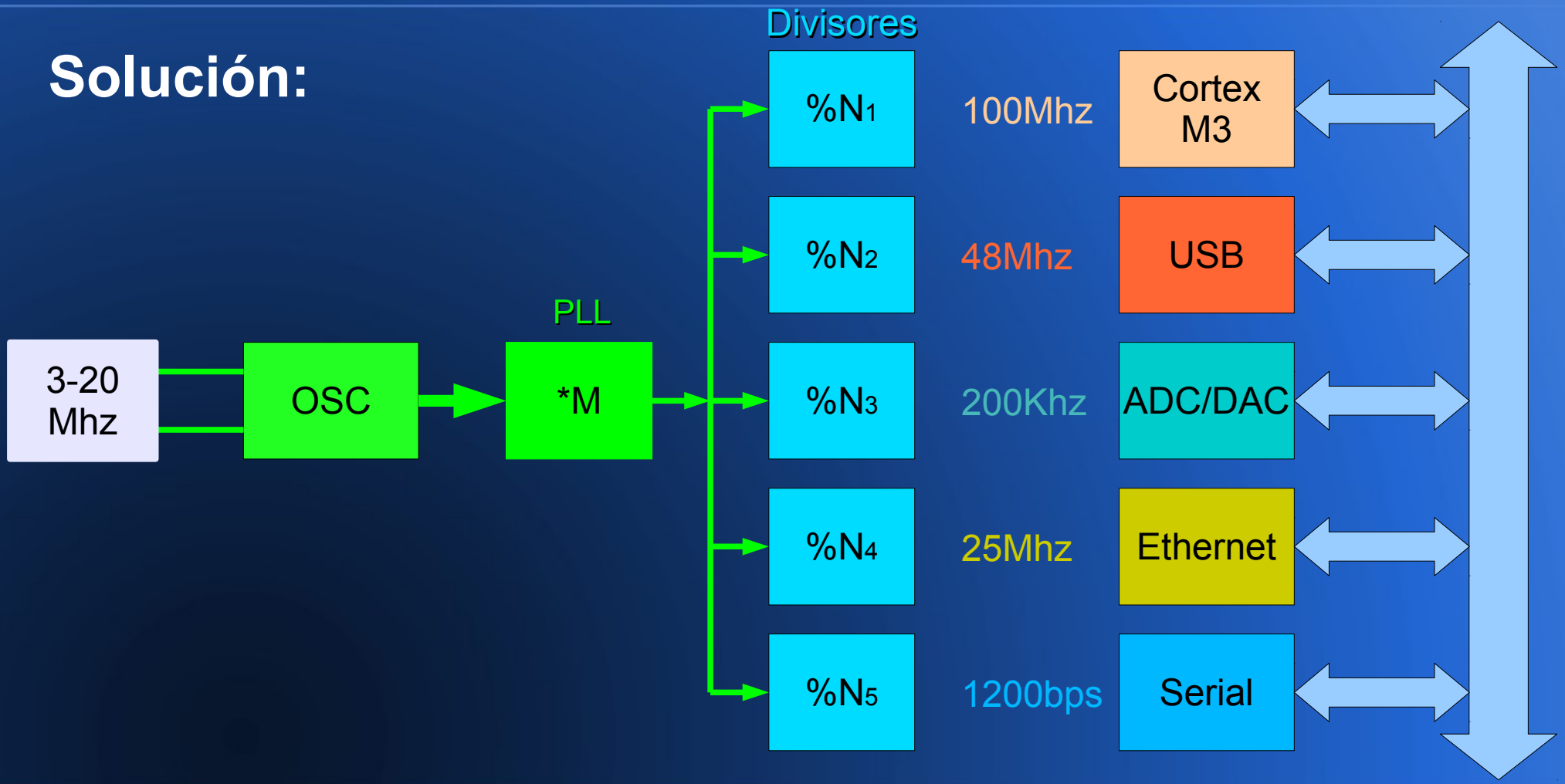
Problema:



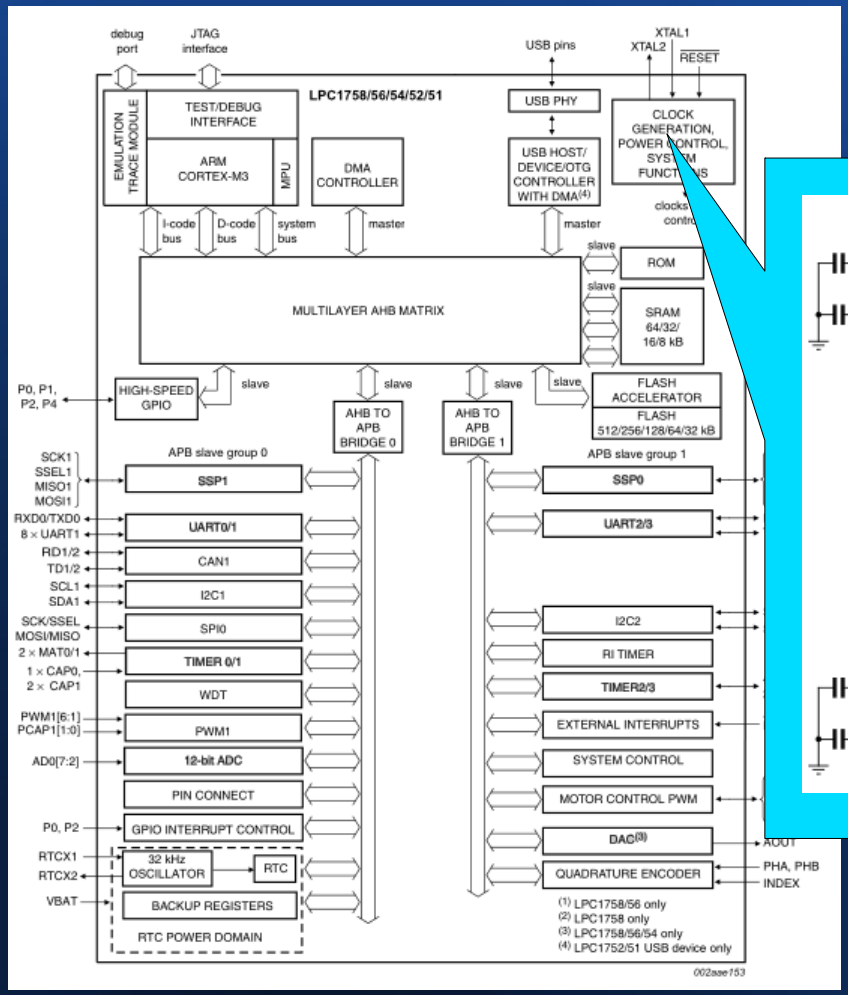
Cortex M3 Clocks

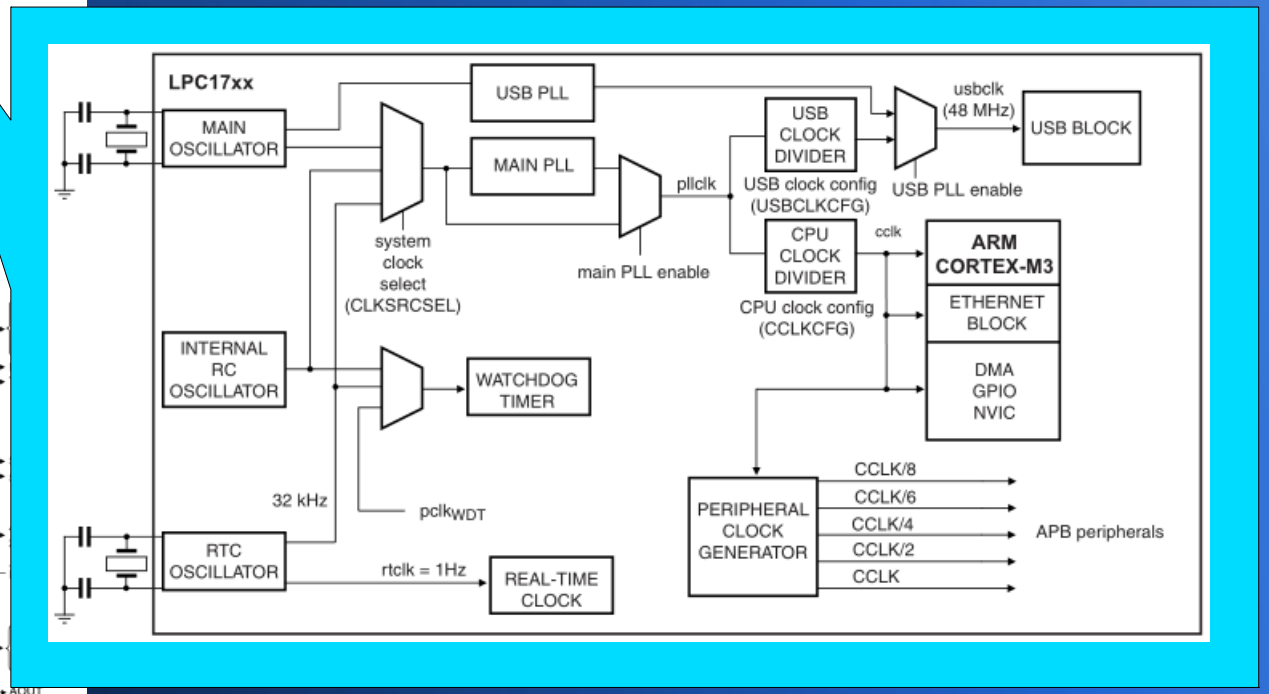


Solución:



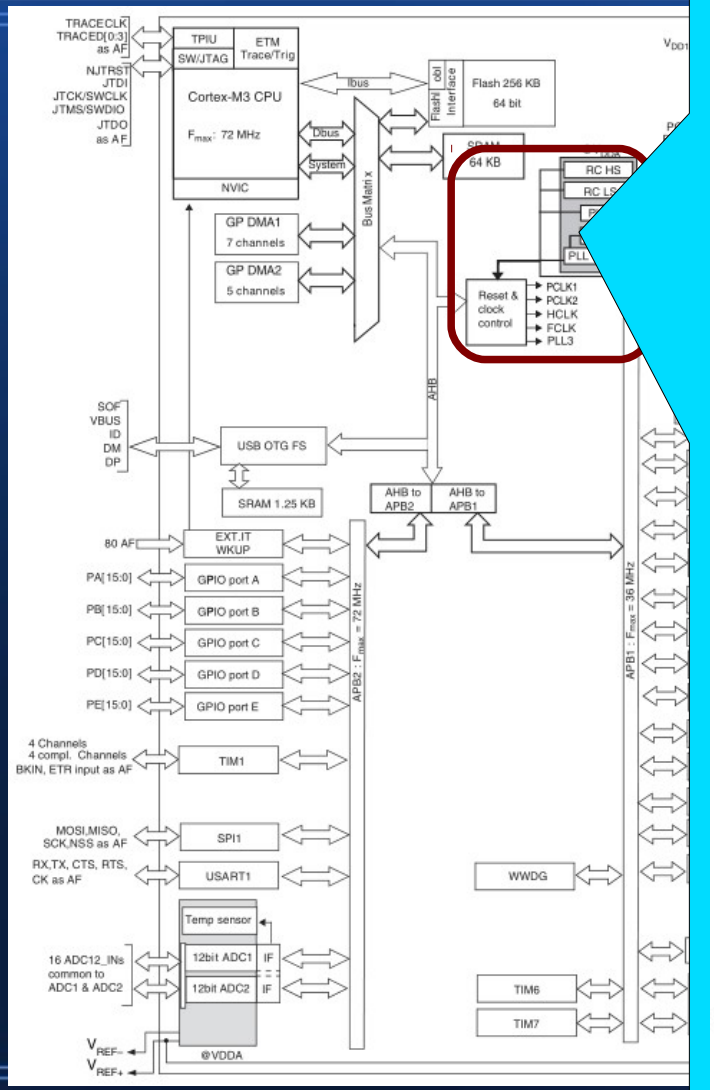
LPC1754 Clock

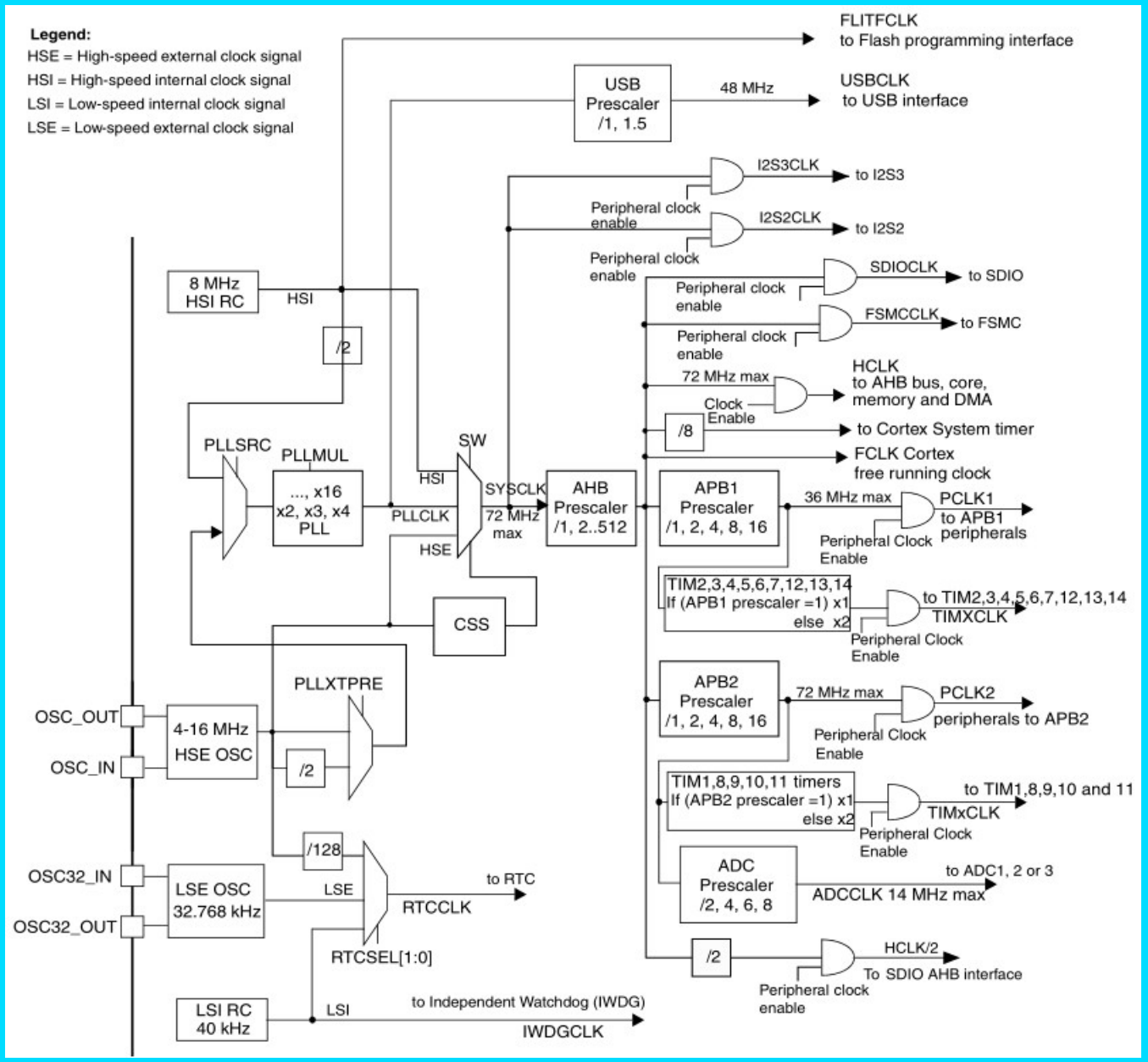




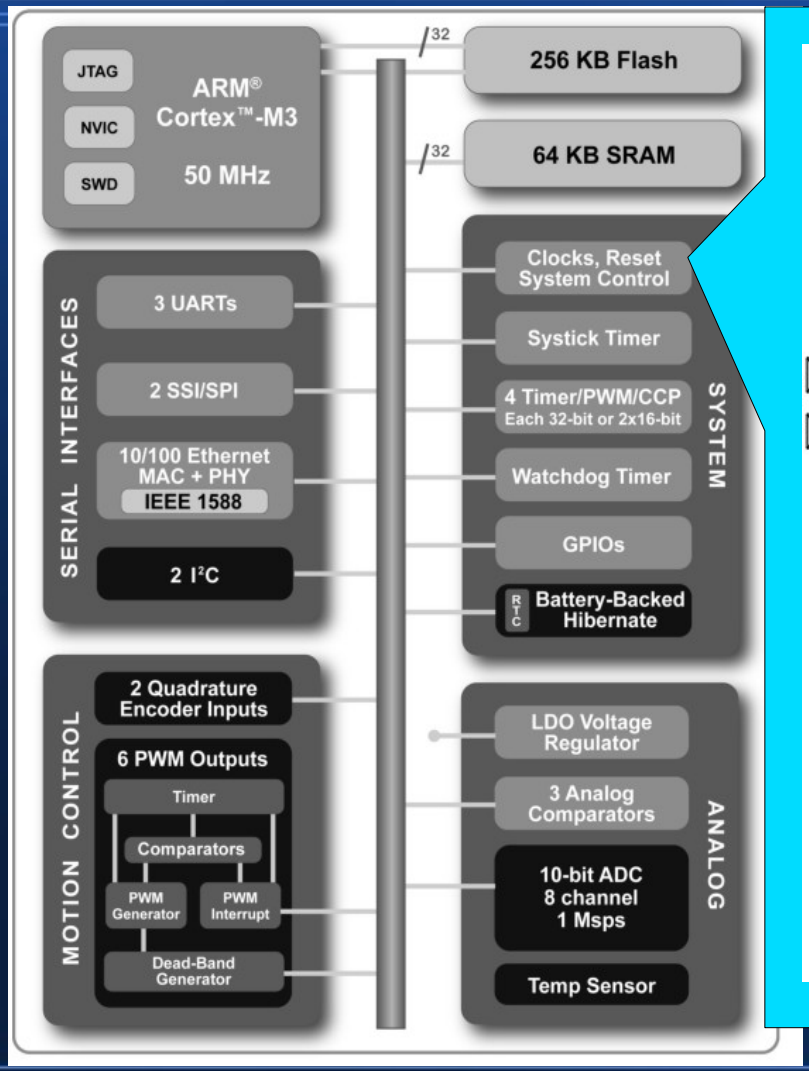
STM32F105 Clock

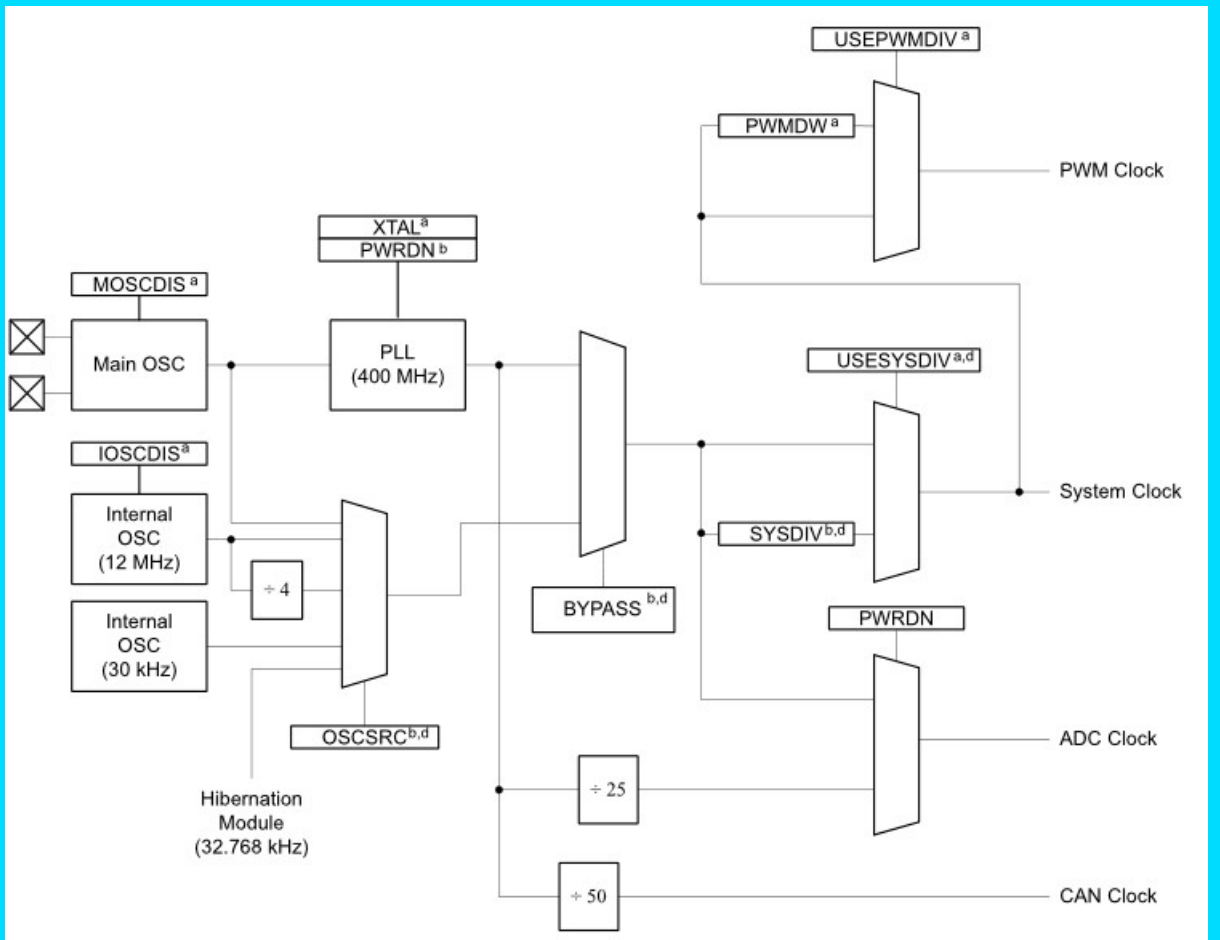
STMicroelectronics



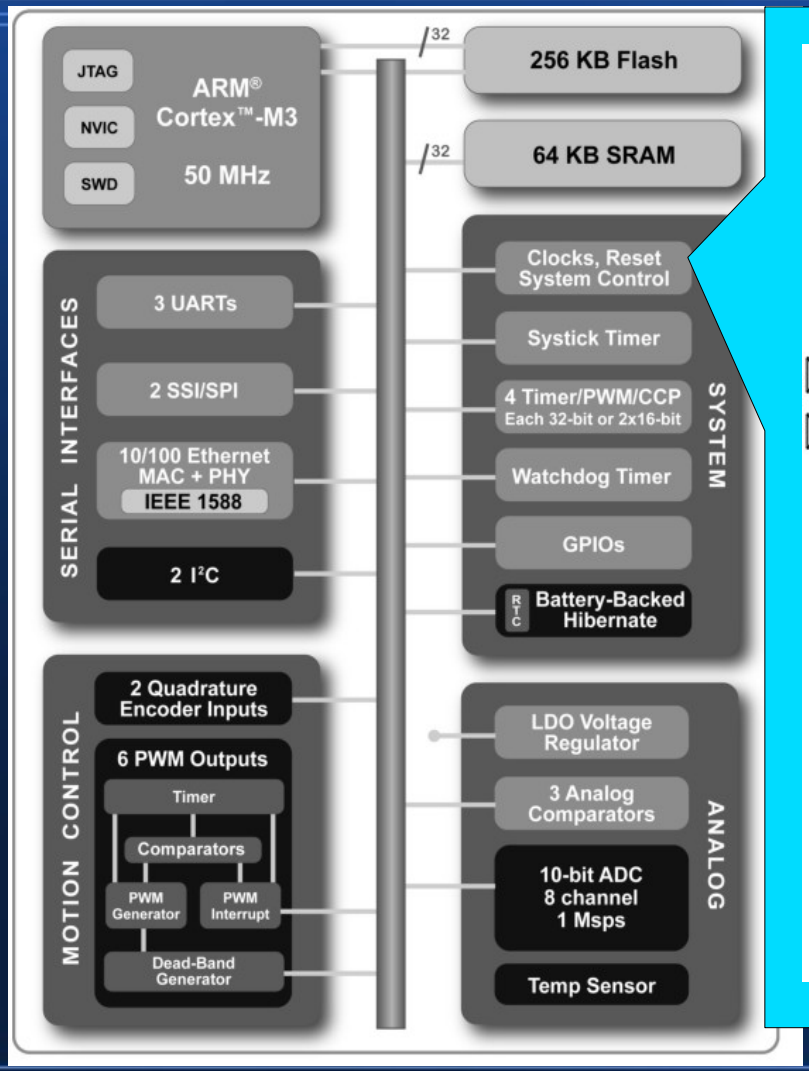


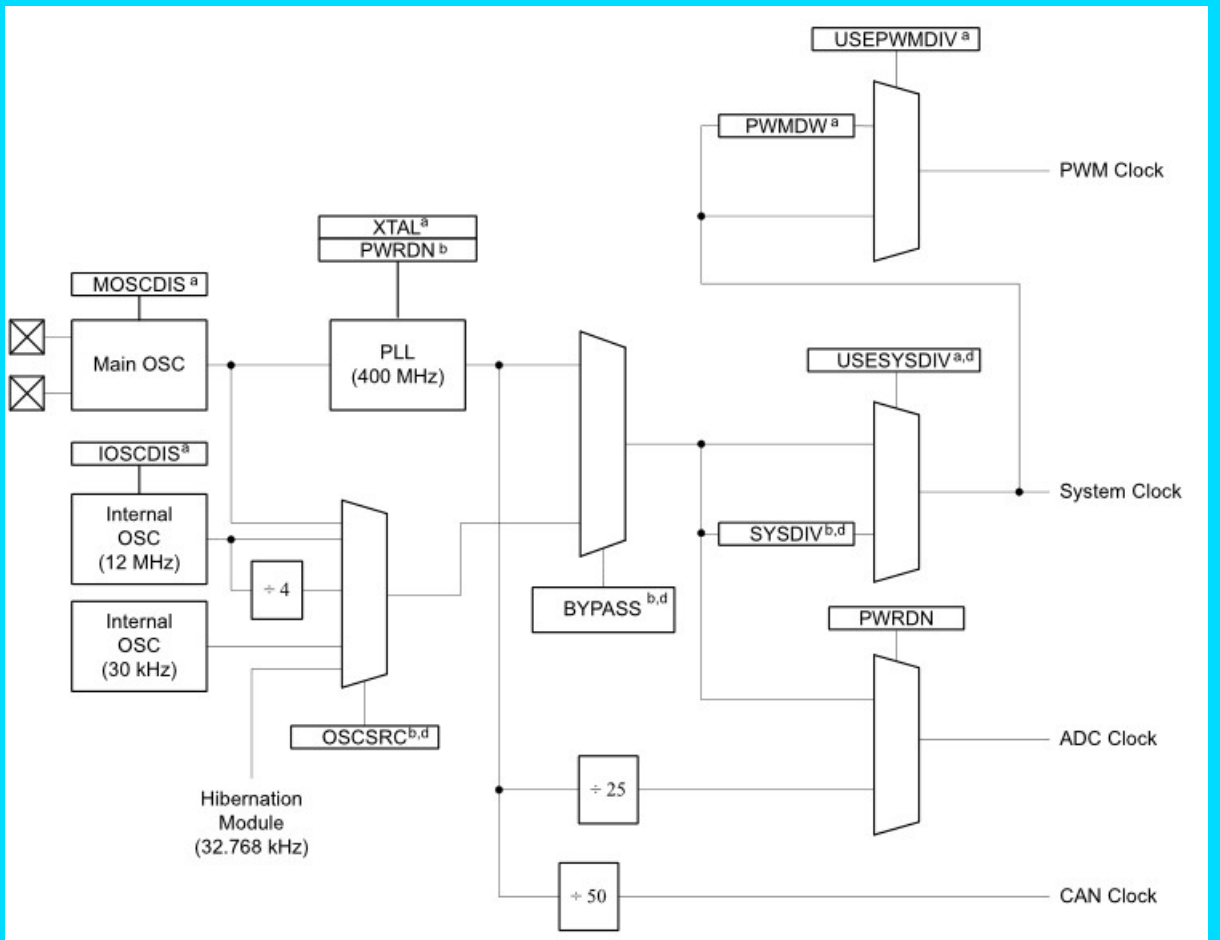
LM3S6537 Clock





LM3S6537 Clock





Compiladores, IDEs y Programadores

Entorno de desarrollo

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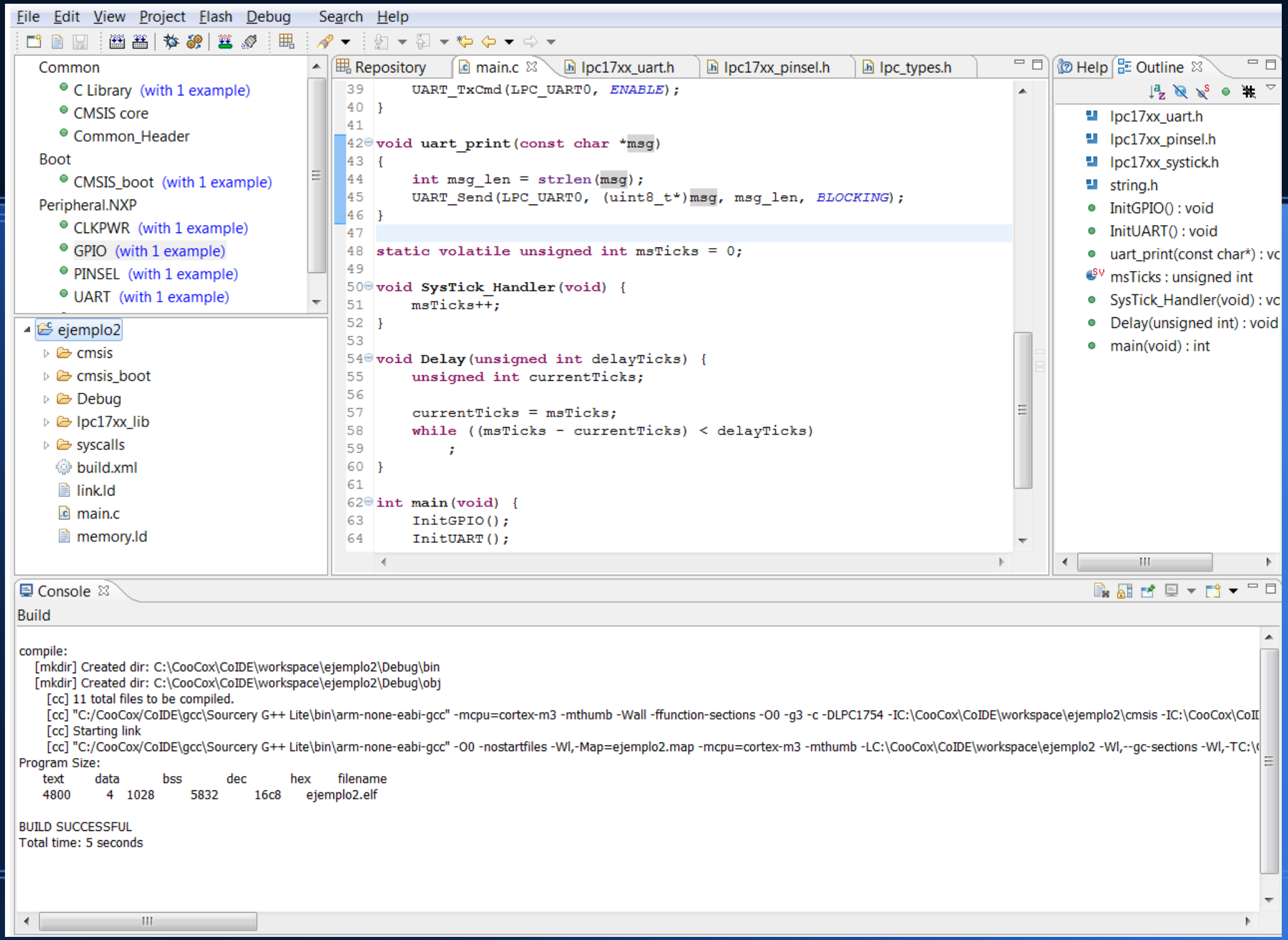
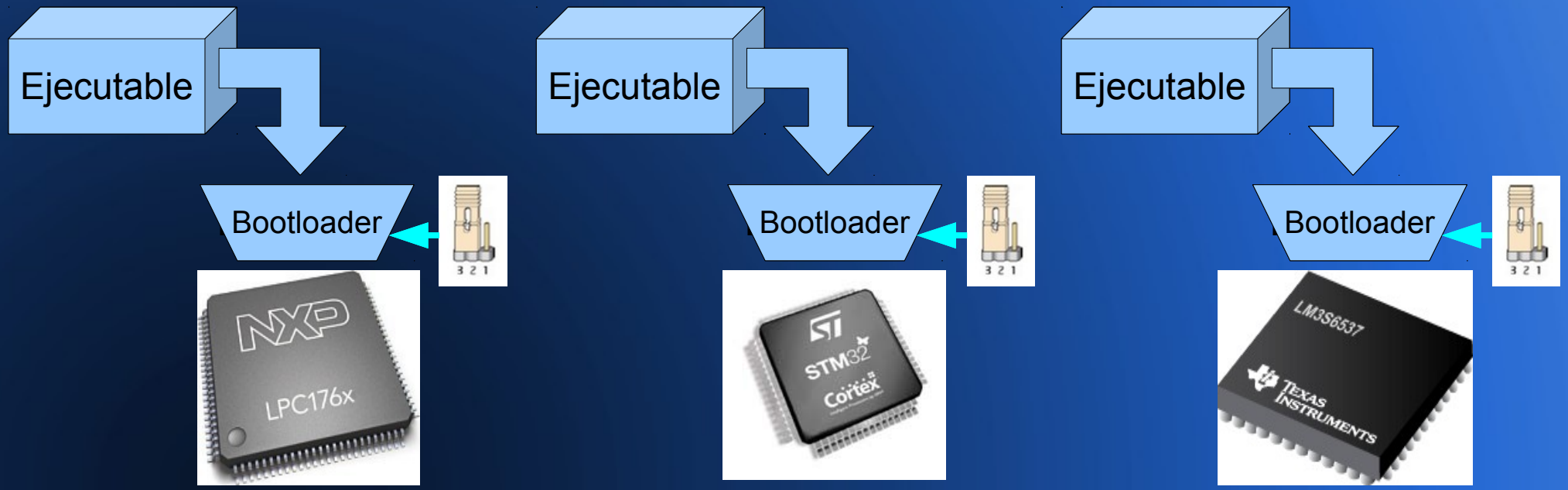
CooCox

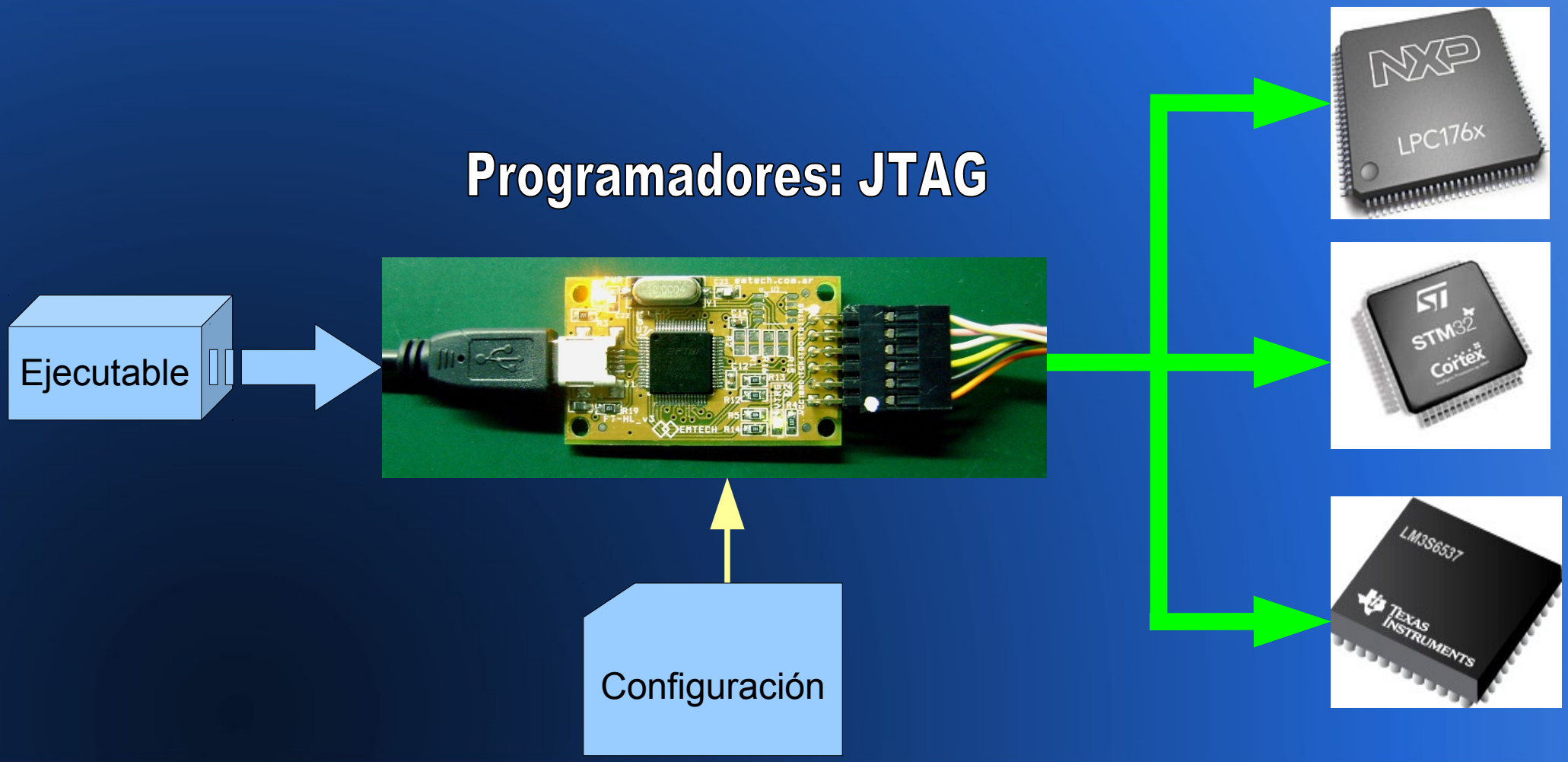

File Edit View Project Flash Debug Search Help
Common
C Library (with 1 example)
CMSIS core
Common_Header
Boot
CMSIS_boot (with 1 example)
Peripheral.NXP
CLKPWR (with 1 example)
GPIO (with 1 example)
PINSEL (with 1 example)
UART (with 1 example)
ejemplo2
cmsis
cmsis_boot
Debug
lpc17xx_lib
syscalls
build.xml
link.ld
main.c
memory.ld
Repository
main.c
lpc17xx_uart.h
lpc17xx_pinsel.h
lpc_types.h
39 UART_TxCmd(LPC_UART0, ENABLE);
40 }
41
42 void uart_print(const char *msg)
43 {
44 int msg_len = strlen(msg);
45 UART_Send(LPC_UART0, (uint8_t*)msg, msg_len, BLOCKING);
46 }
47
48 static volatile unsigned int msTicks = 0;
49
50 void SysTick_Handler(void) {
51 msTicks++;
52 }
53
54 void Delay(unsigned int delayTicks) {
55 unsigned int currentTicks;
56
57 currentTicks = msTicks;
58 while ((msTicks - currentTicks) < delayTicks)
59 ;
60 }
61
62 int main(void) {
63 InitGPIO();
64 InitUART();
Help
Outline
lpc17xx_uart.h
lpc17xx_pinsel.h
lpc17xx_systick.h
string.h
InitGPIO() : void
InitUART() : void
uart_print(const char*) : vc
msTicks : unsigned int
SysTick_Handler(void) : vc
Delay(unsigned int) : void
main(void) : int
Console
Build
compile:
[mkdir] Created dir: C:\CooCox\CoIDE\workspace\ejemplo2\Debug\bin
[mkdir] Created dir: C:\CooCox\CoIDE\workspace\ejemplo2\Debug\obj
[cc] 11 total files to be compiled.
[cc] "C:/CooCox/CoIDE\gcc\Sourcery G++ Lite\bin\arm-none-eabi-gcc" -mcpu=cortex-m3 -mthumb -Wall -ffunction-sections -O0 -g3 -c -DLPC1754 -IC:\CooCox\CoIDE\workspace\ejemplo2\cmsis -IC:\CooCox\CoI
[cc] Starting link
[cc] "C:/CooCox/CoIDE\gcc\Sourcery G++ Lite\bin\arm-none-eabi-gcc" -O0 -nostartfiles -Wl,-Map=ejemplo2.map -mcpu=cortex-m3 -mthumb -LC:\CooCox\CoIDE\workspace\ejemplo2 -Wl,--gc-sections -Wl,-TC:\
Program Size:
text data bss dec hex filename
4800 4 1028 5832 16c8 ejemplo2.elf
BUILD SUCCESSFUL
Total time: 5 seconds

Compiladores, IDEs y Programadores

Programadores: Vendor Custom



Compiladores, IDEs y Programadores



It's a break time!