Migrating to PSoC® 5 Production Devices

Introduction

This document discusses the known issues that may be encountered when migrating designs that target ES-marked (engineering sample) PSoC 5 devices to production parts. For general guidelines around updating the projects from PSoC Creator 1.0 (Beta, Production or Service Pack release) to version 2.0, refer to document 001-73852, *PSoC® Creator™ 2.0 Migration Guide*. The document is located on disk in the installation "documentation" folder and online at http://www.cypress.com/go/creator_migration.

PSoC Creator 2.0 supports production-qualified PSoC 5 devices. To build projects for production PSoC 5 devices, you must update designs to the latest components available in PSoC Creator 2.0.

Key migration issues discussed in this document include:

- Legacy Support for ES-Marked Devices
- Changes Impacting Components
- Changes to Design-Wide Resources
- Compatibility with PSoC Creator 1.x Bootloaders
- Low Power Operation

Legacy Support for ES-Marked Devices

Only two ES-marked devices were sampled to customers.

Software support for the two sample-only parts remain available from the Device Selector for use with early PSoC 5 kits:

- CY8C5588AXI-060ES1 (100-TQFP in First Touch and PSoC 5 processor module)
- CY8C5588LTI-114ES1 (68-QFN)

These two parts appear in the Device Selector with the suffix “ES1” to match the packaging. All other PSoC 5 parts are production qualified.

Changes Impacting Components

In the following cases, changes to the device datasheet impact the availability and performance of components in product silicon.

Functional Blocks No Longer Supported

Some functional blocks that were available in the ES1 devices have been disabled in the production parts. PSoC Creator 2.0 uses design-rule checks to help users correct designs that attempt to use missing functionality.

Block	Component	Message	Resolution
CAN	CAN component and macro	Error in component: CAN_1. The CAN (CAN_1) component is not supported on the PSoC 5 device.	Remove the CAN component from the design and application. Note that, while CAN is not present in production devices, if you are using it for prototyping purposes on ES1 devices today, it can be enabled in PSoC Creator. Contact Cypress Technical Support for support on expected device availability dates for PSoC 5 devices with CAN support. This use of CAN is currently limited to ES-marked devices and is for prototyping/evaluation only.
Temperature Sensor	Die Temp	Error in component: DieTemp_1. The DieTemp component (DieTemp_1) is incompatible with PSoC 5 silicon.	The die temperature sensor is used by the flash and EEPROM programming algorithms but is not available for use by the application for coarse temperature measurement. Remove the DieTemp component from the design and application.
External Memory Interface	EMIF (ExtMemIntf).	Error in component: EMIF_1. PSoC 5 does not have support for the EMIF functionality, so this component (EMIF_1) cannot be used with this silicon.	Remove the EMIF component from the design and application.
Boost	BoostConv	Error in component: BoostConv_1. PSoC 5 does not have support for the Boost Converter functionality, so this component (BoostConv_1) cannot be used with this silicon.	Remove the BoostConv component from the design and application.

Functional Blocks with New Specifications

Some device blocks have relaxed performance characteristics in production silicon.

IMO Accuracy (Impacts UART, USBFS, and other Components)

The Internal Main Oscillator is 5% accurate at 3 MHz. This impacts designs that require more accurate clocks and so the use of the MHz External Crystal Oscillator (MHzECO) is recommended.

The UART, USBFS, and other components, for example, cannot be clocked from the IMO. For USBFS the bus clock (BUS_CLK) must be 33 MHz or greater.

SAR ADC Sample Rate

The maximum sample rate for the SAR ADC block is 700 ksps. The SAR_ADC component has been updated to ensure the block is not configurable out-of-spec and the following error is generated in the parameter editor:

> Invalid Parameter: (Internal clock frequency must be between 1 MHz and 14 MHz. Please change ADC_Resolution or Sample_Rate).

I2C Bit Rate

The maximum bit rate for the I2C block is 400 kbps when implemented in a fixed function block. The I2C component has been updated to ensure the block is not configurable out-of-spec and the following error is generated:

> Error in component: I2C_1. Fixed-Function implementation supports only standard data rates 50, 100 or 400 kbps for PSoC 3 ES2 and PSoC 5 devices.

Port Reset State (Impacts Pins Component)

Production silicon only supports high-impedance as a port setting on device reset. This drive mode is over-ridden during the boot process to match the Pins component parameters for each port.

Pins components with a port reset drive mode of don’t care, pulled-up or pulled-down will silently assume the correct setting; high-Z analog.

The Reset tab in the Pins parameter dialog is no longer visible.

Changes to Design-Wide Resources

The following sections list the changes in available design-wide resources. Changes impact the Pins, Clocks and System Design-Wide Resources (DWR) editors.

In most cases designs will be migrated to new settings when production parts are targeted. When you open old projects and re-target to production parts PSoC Creator will display a list of applied, and required, changes in the Output window.

Pins Editor

Dedicated XTAL Pins

The MHz ECO pins are dedicated to the XTAL clock source and cannot be configured for GPIO. The editor does not allow Pins components to be placed on these physical pins. Pins components that are locked to the XTAL pins on the device are unlocked when the project is opened and assigned a new location by the fitter on the first build.

Designs using either, or both, p15[0] and p15[1] as locked I/Os produce the following warning.

> The design uses pins p15[0] and p15[1] which are now dedicated to the XTAL (MHz ECO) input.

Pin instances {Pin_1} and {Pin_2} are re-assigned to new physical pins when the application is next built.

Clock Editor

Maximum Operating Frequency

This is now limited to 67 MHz. Designs targeting higher frequencies generate an error message.

Internal Main Oscillator Frequency

This is limited to 48 MHz. Designs targeting higher frequencies generate the following error message.

The IMO clock source was set to {xx} MHz, which exceeds the maximum allowed value of 48 MHz for this device.

Adjust the IMO setting in the Clocks tab of the design-wide resource editor and check that your local and design-wide clocks still meet your requirements.

System Editor (Configuration)

Enable Error Correcting Code (ECC)

This is no longer supported and has been removed from the Editor. The memory is still available for project configuration data and that is controlled by a new “Use dedicated configuration data memory” option. It defaults to true in all cases. Existing projects opened with this feature enabled are automatically corrected and the following warning is issued.

Error Correcting Code (ECC) is no longer supported and has been disabled (it is no longer presented in the System design-wide editor). You may still use this flash memory for configuration data.

Enable Fast IMO during Device Startup

This is no longer supported and has been removed from the Editor. Existing projects opened with this feature enabled are automatically corrected and the following warning is issued.

The option for a Fast IMO during device startup is no longer available and has been disabled.

System Editor (Programming\Debugging)

Debug Port Select (DPS)

Production devices only support SWD and SWV debugging. This DWR item has been shortened to “Debug Select” and now only changes the pin access rules for the design. It no longer modifies on-chip non-volatile latches to control the reset state of the device.

The feature to attach the debugger to a running target is not fully functional on PSoC 5 devices. The menu item remains active and the “Attach to running target” dialog appears; however, in many cases the device will not be displayed. The only circumstance where the

feature is available on these parts is after a “regular” debug session (that is, attach and reset) has completed, and the device has not been reset or powered down prior to opening the dialog.

When existing projects with JTAG debugging enabled are opened, the setting is changed and the following warning is issued.

> JTAG is no longer available as a debugging option. The debug selection has been changed to “SWD+SWV” in the System design-wide editor.

The tool also changes the project setting to “SWD+SWV”.

Enable

It is not possible to set the debug pins to be permanently enabled/disabled and this option has been removed from the Editor. Debug pins default to GPIO and require a debugger (e.g. MiniProg3) connection to enable debugging.

Require XRES Pin

This option is redundant and has been removed from the editor. The editor will always show this pin as XRES.

Use Optional XRES

This option is not supported and has been removed from the Editor. The DWR Pin Editor will always show this pin as GPIO. Existing projects opened with this feature enabled are automatically corrected and the following warning is issued.

> The optional XRES input (p1[2]) is no longer supported and has been disabled (it is no longer presented in the System design-wide editor). You may use this pin as an I/O in your design.

Enable Trace

Embedded Trace is not supported and this option has been removed from the Editor. The pins are now dedicated as GPIO. Existing projects opened with this feature enabled are automatically corrected and the following warning is issued.

> Embedded Trace (ETM) is no longer supported and has been disabled (it is no longer presented in the DWR System Editor). You may use these pins as IOs in your design.

System Editor (Voltage Configuration)

Vdd Settings

Vdd settings below 2.7 V are not legal and produce the following error.

> The device may not be operated below 2.7 V. Please ensure it is suitably powered and adjust the values in the System Editor.

Compatibility with PSoC Creator 1.x Bootloaders

There are no migration issues with bootloader and bootloadable applications if both are migrated to PSoC Creator 2.0 using the information above. Migrating both projects is highly recommended for ES1 parts and is mandatory if you are using production silicon.

If you have bootloaders, built with PSoC Creator 1.0, running on ES-marked devices then you should either update the bootloader to PSoC Creator 2.0 and re-program the device or continue to use PSoC Creator 1.0 to build bootloadable applications. This is because bootloaders check for consistent design-wide resources settings in the bootloadable project and some of these settings are no longer available. The impacted settings are as follows.

- Enable Error Correcting Code (ECC) – unchecked
- Enable Fast IMO During Device Startup – unchecked
- Debug Port Select (DPS) – Debug ports disabled
- Use Optional XRES – unchecked

If your 1.0 bootloader project uses the above settings then you should have no problems updating the system with a bootloadable project created in PSoC Creator 2.0.

Low Power Operation

Wakeup Sources

PSoC 5 supports a reduced functionality low power mode. The wakeup sources are the CTW (from sleep mode) and XRES (from sleep and hibernate mode). Performing an XRES wakeup source causes a device reset. The CTW is controlled by the SleepTimer component and it allows sleep intervals of 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, or 128 ms. However, it is important to remember that the Sleep Timer's clock source, the ILO, has frequency variation that will affect the Sleep Timer's interval. This variation is shown in the device datasheet.

Note that neither the PICU (any interrupt-enabled pin) nor the real-time clock (RTC) can be used to wake up the chip.

When entering sleep mode the Pm* APIs, which are documented in the System Reference Guide, disable all interrupts to ensure that only a CTW event can wake the device from sleep.

Always Use _Stop() APIs to Power Down Analog Components

Some analog resources on PSoC 5 require care when entering a low power state. Simply cutting power through direct register access may leave the resource in a state that does not exit low power modes cleanly. The _Stop() APIs generated by components that use these resources handle the power-down operation cleanly. Starting and stopping components before entering sleep is handled by the APIs to ensure a safe transition between states. Do not modify the registers directly and bypass the sleep APIs.

Document History

Document Title: Migrating to PSoC® 5 Production Devices

Document Number: 001-74087

Revision	Submission Date	Description of Change
**	11/16/2011	New Spec – Initial Release for PSoC Creator 2.0
*A	12/22/2011	Updated the "attach to running target" feature for PSoC 5 devices.
*B	3/9/2012	Updated text in "Wakeup Sources" section.