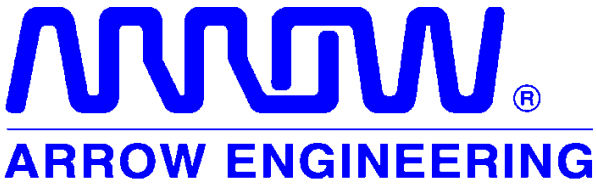
Atmosfire Development Kit
Atmosfire Hardware Reference Guide
Version A01



This page is intentionally left blank.

Revision History		
Version	**Date**	**Updates**
1.0	070415	Document public release.

Arrow Engineering Sweden, Timmernabben, Sweden

1 Overview

Thank you for choosing an Arrow Engineering development kit. We would like to encourage you to honestly feedback anything you want us to improve on future releases to turnkey@arrownordic.com, your input will be forwarded to the makers of this kit.

Atmosfire is an PMEE (see Bitfire documentation for more info on different types of expansion) expansion module that fits on top of the Bitfire V1.12 and above. The board provides a good test vehicle for STMicroelectronics STR710 ARM7 MCU. Board comes with a 1MB onboard configurable SRAM on EMI making it ideal for debugging, USB mini-B connector. All peripherals on Bitfire utilized e.g. CAN connectors, UARTs, LED matrix and debug tools. Further we have fitted a configurable 16Mbit SPI-flash for storage and file system. We have a Zero-Jumper strategy on our kits, the configuration is made without need for moving jumpers and searching documentation for the setup. Either you use pushbutton interface with clearly marked functions on indicators or you use MagicConfig utility that setups the board with built in documentation on settings, see configuration and '*MagicConfig Handbook'* for more details. The kit comes with a complete software package filled with candy see the *'Atmosfire Software Developers Guide'* for more information.

This guide explains the hardware design and various functions on the Atmosfire module itself, for more information on Bitfire functionality please refer to *'Bitfire Hardware Reference Guide'*.

2 Getting Started

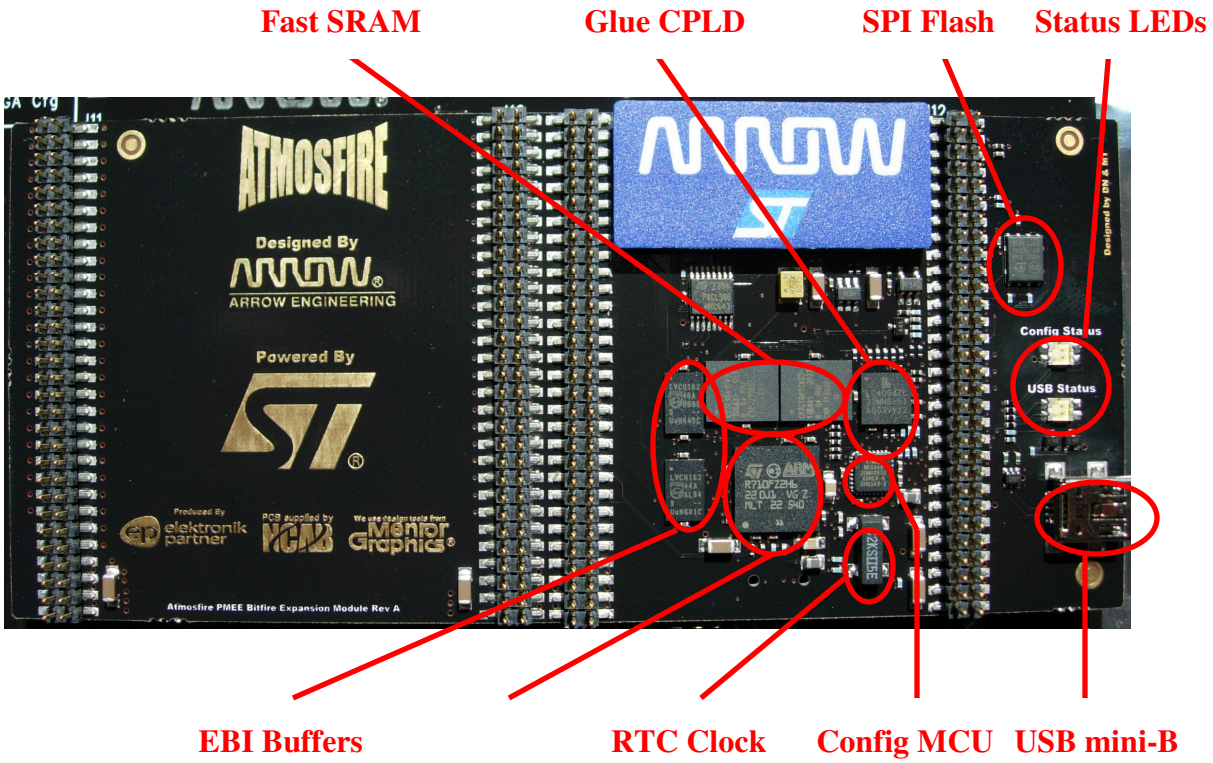
The Atmosfire fits ontop of Bitfire expansion connectors and the two boards together make up a complete system. The MCU fitted on Bitfire is disabled when Atmosfire is plugged in.

Caution: When mounting the Atmosfire onto the Bitfire connectors please make sure that they are correctly aligned and even pressure is applied to each connector. Also make sure that Bitfire is not powered during this operation.

Caution: When using external debug tools on this revision it is prohibited to force reset signal high. The reset should have an open collector configuration (witch is the common approach) and need to pull the reset line below 250mV for a secure reset. Reset signal is clamped to ~0.45V.

Caution: Plug/unplugging PC connectors while powered may damage your PC.

2.1 Board overview



2.1.2 Fast SRAM

The SRAM equipped on Atmosfire, is a high speed SRAM that enables you to run the MCU in full speed and zero wait states on the EBI. However the STR710 support 16-bit data bus in non multiplexed mode as the widest option so executing from SRAM in ARM mode will give two EBI fetches per instruction. You still have the option to run code from internal interleaved high performance flash (256kB) or full speed capable SRAM (64kB). By configuration settings the external SRAM can be mapped to either chip select 0 or chip select 1, you also have the possibility to make it invisible leaving all CS signals unused. Further you can remap memory so that external SRAM is visible from address 0x00000000 and upwards this makes debugging and using the exception vectors convenient in external SRAM.

2.1.3 Glue CPLD

This is a tiny Lattice high speed CPLD handling various glue functions such as memory mapping, clock scaling and control, controlling external EBI, enabling and mapping control lines to SPI Flash. Device is controlled trough a SPI port from the config MCU that uploads the current configuration setting.

2.1.4 SPI Flash

This is a 16Mb data flash in a 6x5mm QFN package segmented into pages down to 256 bytes. The purpose of the flash is to hold file system, bootable images etc. The control lines to the flash can be connected to port pins P1.8 for \W and P1.5 for \S trough configuration settings in configuration MCU trough MagicConfig utility (see separate section). The flash when enabled it is hooked onto the BSPI0 channel of the STR710.

2.1.5 Status LEDs

Status LEDs for indicating different modes, these are red/green bi-color LEDs.

USB Status
Green = 5V is present on the USB connector from the HOST system.
Red = P1.9 of the STR710 for indicating enumeration status.

Config Status
Green = Flashes when activity such as application command or ping pulse
Red = Reset indication

2.1.6 EBI Buffers

These buffers the EBI to external bus connector for utility modules that can be stacked on top of the Atmosfire. This external drive can be disabled trough configuration. The buffers also has internal pulling devices that will ensure that the bus on the Atmosfire is kept at defined logic levels when the bus is floating e.g. at various sleep modes, this reduces current leakage significantly and ensures safe operation in these conditions.

2.1.7 STR710

Fully integrated low cost ARM7TDMI MCU with 256+16kB flash and 64kB SRAM, 4xUART's, CAN, USB 2.0 FS, 2xI2C, 2xBSPI, RTC, 12-bit A/D and EBI. Everything packed in a tiny 10x10mm 144 ball FBGA package and it comes with a number of different sleep and low power modes.

2.1.8 RTC Clock

A 32.768kHz watch crystal is supplied for generating clock signal to the built-in real time clock (RTC) block in STR710.

2.1.9 Config MCU

This MCU handles configuration for memory, clocks, resets and more. The firmware in this MCU is based on the general purpose MagicConfig platform. In the Atmosfire an I2C network is formed with the MagicConfig MCU on the base Bitfire board. Accessing the Bitfire MagicConfig MCU trough UART-0 will give access trough its I2C bridge to Atmosfire configuration. No separate RS232 connection to Atmosfire is needed or even possible. Configuration settings are stored in non volatile EEPROM and commands for wakeup ping, reset etc can be given trough this communication tunnel using the MCF utility. New firmware can also be uploaded and restarted trough the same tunnel. More information can be found under configuration section or in the *'MagicConfig Handbook'*.

3 Board description

The Atmosfire is an expansion module aimed to fit onto the Bitfire platform and replace its own MCU with STR710 as target. The goal was also to add some features giving a good platform for debugging. The USB connector was added on the Atmosfire as Bitfire currently has no USB support itself. We have equipped the module with both a data flash and a medium sized high speed SRAM for making it ideal for operating systems based solutions. By integrating the whole MCU design on 30x25mm with many options to cut space on a custom solution we wanted to demonstrate the small size, very low cost but big potential as a workhorse in full featured operating system solution. STR710's biggest advantages are that it has a wide mix of peripherals, EBI for addressing large SRAM, small size and low current consumption. This module clearly demonstrates these advantages.

3.1 STR710

Following is a summary on the specs of what the STR710 family offers, there is a number of other family offered by STMicroelectronics, please refer to their homepage.

Core
– ARM7TDMI 32-bit RISC CPU
– 59 MIPS @ 66 MHz from SRAM
– 45 MIPS @ 50 MHz from Flash

Memories
– Up to 256Kbytes Flash program memory (10 kcycles endurance, 20 yrs retention)
– 16K bytes Flash data memory (100 kcycles endurance, 20 yrs retention)
– Up to 64 Kbytes RAM
– External Memory Interface (EMI) for up to 4 banks of SRAM, Flash, ROM.
– Multi-boot capability

Clock, Reset and Supply Management
– 3.0 to 3.6V application supply and I/O interface
– Internal 1.8V voltage regulator for core supply
– Clock input from 0 to 16 MHz
– Embedded RTC oscillator running from external 32 kHz crystal
– Embedded PLL for CPU clock
– Realtime Clock for clock-calendar function
– 5 power saving modes: SLOW, WAIT, LPWAIT, STOP and STANDBY modes

Nested interrupt controller
– Fast interrupt handling with multiple vectors
– 32 vectors with 16 IRQ priority levels
– 2 maskable FIQ sources

Up to 48 I/O ports
– 30/32/48 multifunctional bidirectional I/O lines
– Up to 14 ports with interrupt capability

5 Timers
– 16-bit watchdog timer
– 3 16-bit timers with 2 input captures, 2 output compares, PWM and pulse counter modes
– 16-bit timer for timebase functions

10 Communications Interfaces
– 2 I2C interfaces (1 multiplexed with SPI)
– 4 UART asynchronous serial interfaces
– Smart Card ISO7816-3 interface on UART1
– 2 BSPI synchronous serial interfaces
– CAN interface (2.0B Active)
– USB v 2.0 Full Speed (12Mbit/s) Device Function with Suspend and Resume support
– HDLC synchronous communications

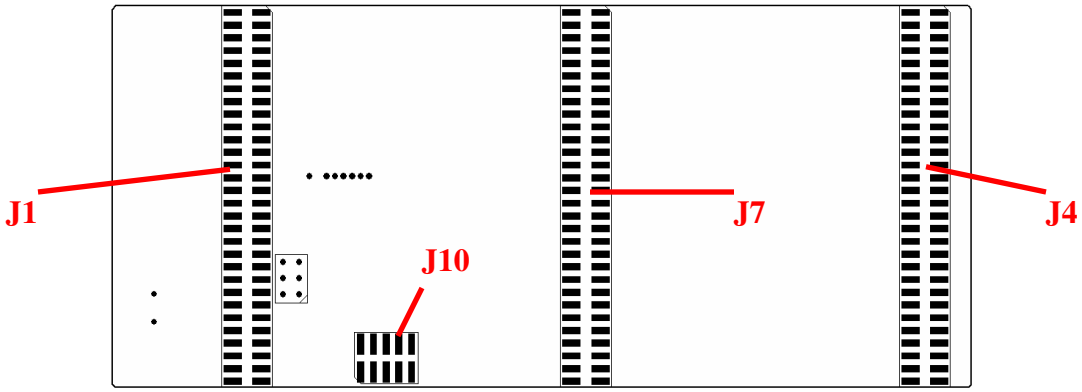
4-channel 12-bit A/D Converter
– Sampling frequency up to 1KHz
– Conversion range: 0 to 2.5V

4 Connector pinouts

Below you will find pinout information on all the onboard connectors. The downstream and upstream connectors have some common signals and some unique signals. For compability reasons with Bitfire expansion headers the signals are carefully laid out.

4.1 Downstream connectors

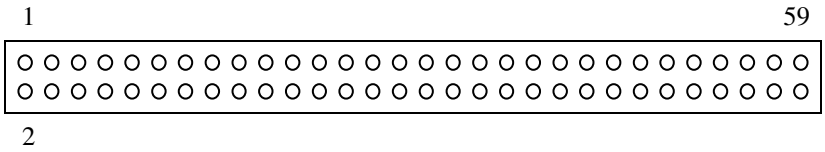
Downstream connectors are connectors mounted on the backside of Atmosfire mating to the Bitfire board.



Bottom View

4.1.1 MCU IO Downstream Connector

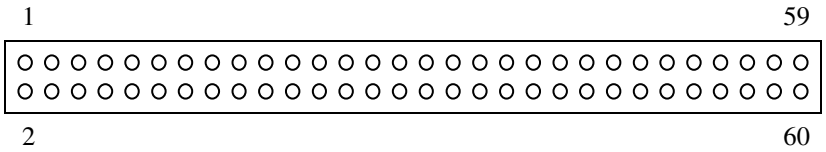
Connector type: 60 pin 1 mm dual row socket. SAMTEC SMx
Connects to: Expansion connector J10 on base board
Reference: J1



Pin	Dir	GPIO	Primary	Secondary	Bitfire Function
4	In	-	\RESET	-	Master Reset
8	Out	P2.4	A20	-	RTS0/DE0
10	In	P2.5	A21	-	CTS0
12	Out	P2.12	-	-	SPI_SEL (FPGA I/F)
13	Out	P0.12	SCCLK	-	SPI_SYNC (FPGA I/F)
14	In	P2.6	A22	-	CTS1
16	Out	P2.7	A23	-	RTS1/DE1
17	In	P0.1	MOSI0	RX3	RXD1
18	Out	P0.0	MISO0	TX3	TXD1
21	Out	P0.5	MOSI1	-	SPI_MOSI0 (FPGA I/F)
22	In	P0.4	MISO1	-	SPI_MISO1 (FPGA I/F)
24	Out	P0.6	SCK1	-	SPI_SCK0 (FPGA I/F)
25	Bi	-	-	-	I2C SDA (to Config MCU)
26	Bi	-	-	-	I2C SCL (to Config MCU)
27	In	P0.13	OCA2	RX2	RXD0
28	Out	P0.14	ICA2	TX2	TXD0
35	Out	P1.12	CANTX	-	CANTX0
36	In	P1.11	CANRX	-	CANRX0
38	Out	-	-	-	CANTX1 (Passtrough)
40	In	-	-	-	CANRX1 (Passtrough)
30,31,32,34		-	-	-	Analog In (to GND)
44,46,48,50		-	-	-	+3V3
52,54,56,58,60			-	-	+1V8
43,45,47,49,51,53,55,57,59			-	-	GND
1,2,3,6,7,5,9,11,15,19,23,29,33,37,20,39,42,41					Not used on Atmosfire, pulled low.

4.1.2 FPGA I/O Downstream Expansion Connector #1

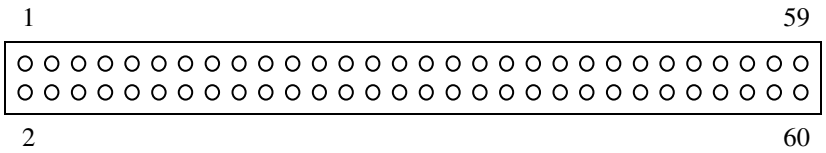
Connector type: 60 pin 1 mm dual row socket. SAMTEC SMx
Connects to: Expansion connector J11 on base board
Reference: J4



All pins are passed trough pin-to-pin to upstream connector J5 to allow FPGA I/O access even if the Atmosfire is fitted. Pin 45 is the 16MHz master clock, this signal is tapped by the Atmosfire and used for distribution and buffered trough the CPLD to Config MCU and ARM MCU. Ground pins are used and 1V5 voltage domain is extra decoupled with 10uF ceramic capacitors.

4.1.3 FPGA I/O Downstream Expansion Connector #2

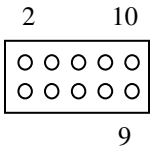
Connector type: 60 pin 1 mm dual row socket. SAMTEC SMx
Connects to: Expansion connector J12 on base board
Reference: J7



All pins are passed trough pin-to-pin to upstream connector J6 to allow FPGA I/O access even if the Atmosfire is fitted. Ground pins are used and 1V5 voltage domain is extra decoupled with 10uF ceramic capacitors.

4.1.4 Stackup JTAG Connector

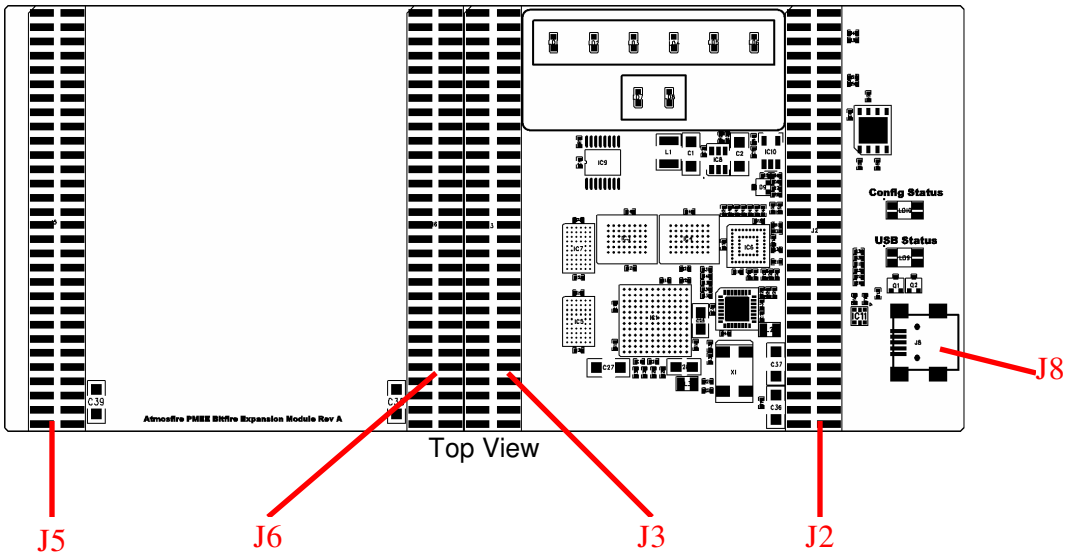
Connector type: 60 pin 1 mm dual pin-header. SAMTEC TMx
Connects to: Expansion connector J6 on base board
Reference: J10



Pin	Dir	Signal
1	In	\TRST
2	In	TDI
3	-	+3V3
4	In	TMS
5	In	\Reset
6	In	TCK
7	-	GND
8	Out	TDO
9	-	GND
10	In	DBGRQS

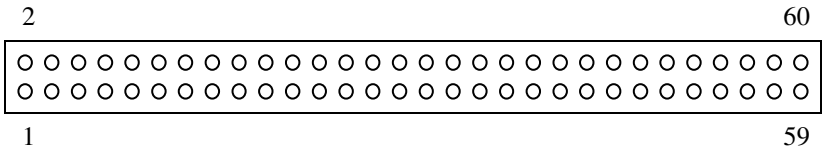
4.2 Upstream connectors

Upstream connectors are connectors facing upward mating to application boards fitted on the module stack.



4.2.1 MCU IO Upstream Connector

Connector type: 60 pin 1 mm dual row pin-header. SAMTEC TMx
Connects to: Expansion card and/or user application
Reference: J2



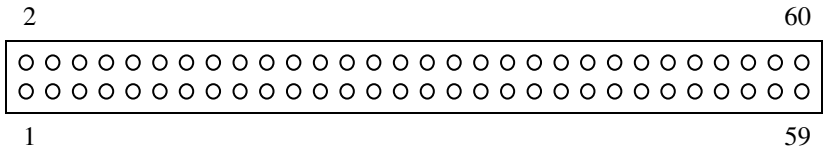
Pin	Dir	GPIO	Primary	Secondary	Planned Upstream Function
1	***Bi***	***P0.0***	***MISO0***	***TX3***	***IO/ MISO (Used for DS_TXD1)***
2	***Bi***	***P0.1***	***MOSI0***	***RX3***	***IO/ MOSI (Used for DS_RXD1)***
3	Bi	P0.3	SDA1	\SS0	IO/ \SSEL
4	Out	-	\CPURESET	-	Master from Atmosfire
5	Bi	P2.10	INT4	-	IO
6	Bi	P0.2	SCK0	SCL1	IO/ SCK
7	Bi	P1.4	ICA1	T1CK	IO/ CMP
8	***Bi***	***P2.4***	***A20***	***-***	***IO/ RTS0/DE0***
9	Bi	P2.11	INT5	-	IO
10	***In***	***P2.5***	***A21***	***-***	***IO/ CTS0***
11	***Bi***	***P2.12***	***-***	***-***	***IO/ (SPI_SEL FPGAI/F)***
12	Bi	P0.7	\SS1	-	IO
13	***Bi***	***P0.12***	***SCCLK***	***-***	***IO/ SPI_SYNC***
14	***Bi***	***P2.6***	***A22***	***-***	***IO/ CTS1***
15	Bi	P2.13	-	-	IO
16	***Bi***	***P2.7***	***A23***	***-***	***IO/ RTS1/DE1***
17	Bi	P0.10	RX1	TX1	IO/ RXD1
18	Bi	P0.11	TX1	BT1	IO/ TXD1
19	Bi	P1.10	USBCK	-	IO
20	Bi	P2.8	INT2	-	IO/ EINT0
21	***Bi***	***P0.5***	***MOSI1***	***-***	***IO/ SPI_MOSI (FPGA I/F)***
22	***Bi***	***P0.4***	***MISO1***	***-***	***IO/ SPI_MISO (FPGA I/F)***
23	Bi	P1.14	HRX	SDA0	IO
24	***Bi***	***P0.6***	***SCK1***	***-***	***IO/ SPI_SCK (FPGA I/F)***
25	***Bi***	***-***	***-***	***-***	***I2C SDA (to Config MCU)***
26	***Bi***	***-***	***-***	***-***	***I2C SCL (to Config MCU)***
27	Bi	P0.8	RX0	TX0	IO/ RXD0
28	Bi	P0.9	TX0	BT0	IO/ TXD0
29	Bi	P1.15	HTX	-	IO
30	Bi	P1.3	ICB3	AN3	Analog 3
31	Bi	P1.2	OCA3	AN2	Analog 2

32	Bi	P1.1	ICA3	AN1	Analog 1
33	Bi	P1.5	ICB1	-	IO
34	Bi	P1.0	OCB3	AN0	Analog 0
35	***Out***	***P1.12***	***CANTX***	***-***	***CANTX0***
36	***In***	***P1.11***	***CANRX***	***-***	***CANRX0***
37	Bi	P1.8	-	-	IO (Can be mapped SPI Flash \SEL)
38	***Out***	***-***	***-***	***-***	***CANTX1 (Passtrough)***
39	Bi	P2.9	INT3	-	IO/ EINT1
40	***In***	***-***	***-***	***-***	***CANRX1 (Passtrough)***
41	Bi	P1.6	OCA1	-	IO/ PWM1
42	Bi	P1.7	OCB1	-	IO/ PWM0

Note: Italic and bolded rows in list are pass-trough signals to Bitfire, these has shared functionality in some sense, please refer to the schematics for more details.

4.2.2 FPGA I/O Upstream Expansion Connector #1

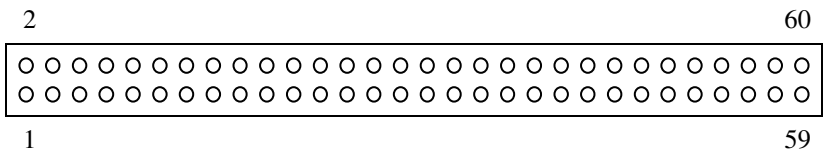
Connector type: 60 pin 1 mm dual row pin-header. SAMTEC TMx
Connects to: Expansion card and/or user application
Reference: J5



All pins are passed trough pin-to-pin to downstream connector J4 to allow FPGA I/O access even if the Atmosfire is fitted. Pin 45 is the 16MHz master clock, this signal is tapped by the Atmosfire and used for distribution and buffered trough the CPLD to Config MCU and ARM MCU. Ground pins are used and 1V5 voltage domain is extra decoupled with 10uF ceramic capacitors.

4.2.3 FPGA I/O Upstream Expansion Connector #2

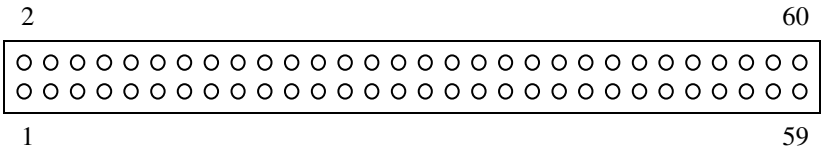
Connector type: 60 pin 1 mm dual row pin-header. SAMTEC TMx
Connects to: Expansion card and/or user application
Reference: J6



All pins are passed trough pin-to-pin to downstream connector J7 to allow FPGA I/O access even if the Atmosfire is fitted. Ground pins are used and 1V5 voltage domain is extra decoupled with 10uF ceramic capacitors.

4.2.4 MCU External Bus Interface Expansion Connector

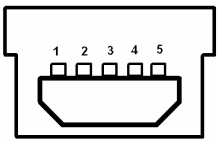
Connector type: 60 pin 1 mm dual row pin-header. SAMTEC TMx
Connects to: Expansion card and/or user application
Reference: J3



Pin	Dir	Signal	Function
1-16	Bi	D0-15	16-bit bidirectional databus
17-36	Out	A0-19	20-bit static address bus
38	Out	\WE	Write Enable
39	Out	\OE	Output Enable
40	Out	\UBYTE	Upper Byte Select
41	Out	\LBYTE	Lower Byte Select
42	Out	CS0	Chip Select 0
43	Out	CS1	Chip Select 1
44	Out	CS2	Chip Select 2
45	Out	CS3	Chip Select 3
54,56,58,60	-		GND
55,57,59	-		+3V3

4.3 USB Connector

Connector type: USB mini-B connector SMD
Connects to: USB HOST system such as PC or similar
Reference: J8



Pin	Dir	Signal	Function
1	In	VCC	HOST Bus power supply
2	Bi	D-	Bidir differential data negative
3	Bi	D+	Bidir differential data positive
4	-	NC	No Connect
5	-	GND	Signal Ground

5 Configuration trough MagicConfig

This section describes the configuration options and commands trough MagicConfig available on the Atmosfire. For more information on details of the configuration utility MCF and firmware upload etc please refer to the *'MagicConfig Handbook'*.

Use 'MCF -?' and 'MCF -?:atmosfire' to get a flying start.

5.1 Implementation

The configuration MCU on Atmosfire is based on MagicConfig codebase, this is a common shell and utility for configuration of the board functionality without the need of using jumpers. The MCF utility itself has built-in documentation for all available settings. It connects to I2C configuration port and are accessed trough its carriers (e.g Bitfire) configuration bridge.

5.2 Configuration word

An internal 16-bit configuration word controls the basic settings of the Atmosfire behaviour, below each of these settings are described. The MCF utility abstraction of these settings is done with keywords for each setting.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FR	WU	B1	B0	STB	LE	SE	WE	OE	CKE	HE	HS	CK1	CK0	CS	CE

FR - Flash reset control
0 = Reset pin forced low (flash disabled)
1 = Reset driven low under reset conditions otherwise released.

WU - Wakeup pin (P0.15) drive enable
0 = Wakeup pin floating
1 = Wakeup pin pulled trough 2k2 responding to 'ping' commands.

B1,0 - Boot memory mapping select

B1	B0	Configuration
0	0	Internal flash mapped at 0x00000000
0	1	Unused
1	0	Internal SRAM mapped at 0x00000000
1	1	External memory on CS0 mapped at 0x00000000

STB - Standby pin drive active low
Writing this bit:
0 = Standby pin driven low
1 = Standby pin released (pulled up by 10K if not in standby)
Reading this bit:
Gives the logic level of nSTB (see refmanual on STR710 for more info)

LE - Logo Enable
0 = The cool flashing Arrow/ST logo is turned off
1 = The cool flashing Arrow/ST logo is turned on

SE - Serial flash \S-pin mapping enable
0 = Pin unmapped (pulled high)
1 = Mapped to P1.8 on the MCU

WE - Serial flash \W signal mapping enable
0 = Pin unmapped (pulled high)
1 = Mapped to P2.13 on the MCU

OE - External bus buffer enable
0 = External bus A and D signals on connector J3 is disabled
1 = External bus A and D signals on connector J3 is enabled

CKE - CK main clock input driver enable
0 = CK pin is floating (external drive possible)
1 = CK pin is driven from CK-generator in CPLD

HE - HCLK clock input driver enable
0 = HCLK pin is floating (external drive possible)
1 = HCLK pin is driven from HCLK-generator (4MHz) in CPLD

HS - HCLK stop select
0 = HCLK running 4MHz
1 = HCLK stopped

CK1,0 - CK main clock frequency setting

CK1	CK0	Clock setting
0	0	Tied to GND 0Hz
0	1	4MHz (/4)
1	0	8MHz (/2)
1	1	16MHz (/1)

CS,CE External SRAM chip select configuration

CS	CE	Configuration
x	0	External SRAM memory disabled
0	1	Chip select CS1 mapped for external SRAM
1	1	Chip select CS0 mapped for external SRAM

5.3 Application Commands

There are a few unique commands used for writing settings and controlling the behaviour of the Atmosfire. This section describes the native commands trough the communication tunnel. MCF utility gives an abstraction of these and is easier to use.

5.3.1 RESET

Usage: reset
Result: ok
Resets the MCU and serial flash on the Atmosfire.

5.3.2 SETCFG

Usage: setcfg HHHH
Result: ok
Set bits according to given 16-bit hexmask in the configuration word

5.3.3 CLRCFG

Usage: clrcfg HHHH
Result: ok
Clear bits according to given 16-bit hexmask in the configuration word

5.3.4 GETCFG

Usage: getcfg
Result: HHHH
Reads the configuration word

5.3.5 PING

Usage: ping
Result: ok
Pulses the WAKEUP pin if driving of this signal is enabled.

5.3.6 PINGTIME

Usage: pingtime HHHH
Result: ok
Sets a periodic WAKEUP ping signal, writing 0000 will disable this feature. If ping command is called the timer for this function is reset for a new period (sync). Resolution is 5.12ms, range is therefore 5.12ms – 335.54s (~6 min)

5.4 Atmosfire Specifics

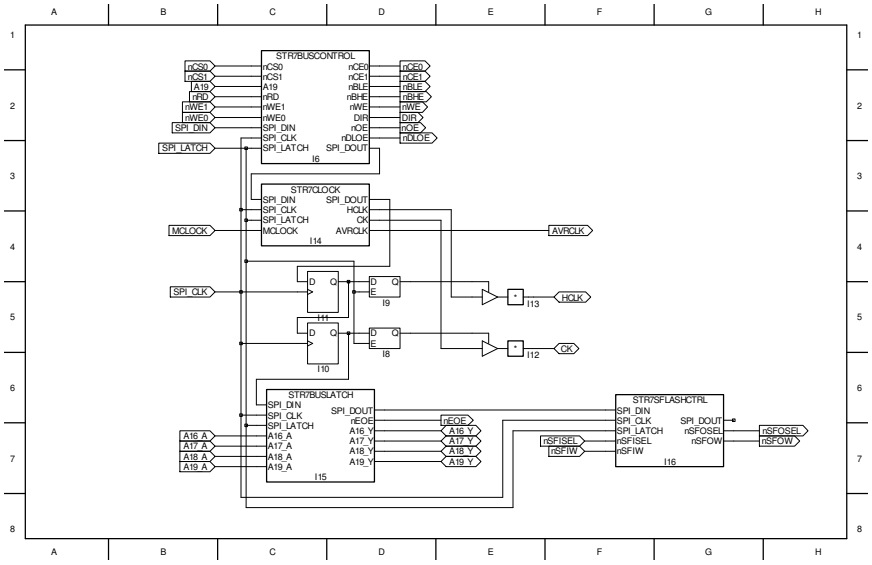
The Equipment ID for Atmosfire Rev.A is 0x02. The hardware condition to force boot monitor lock is holding both I2C signals low during power up.

Design Reference

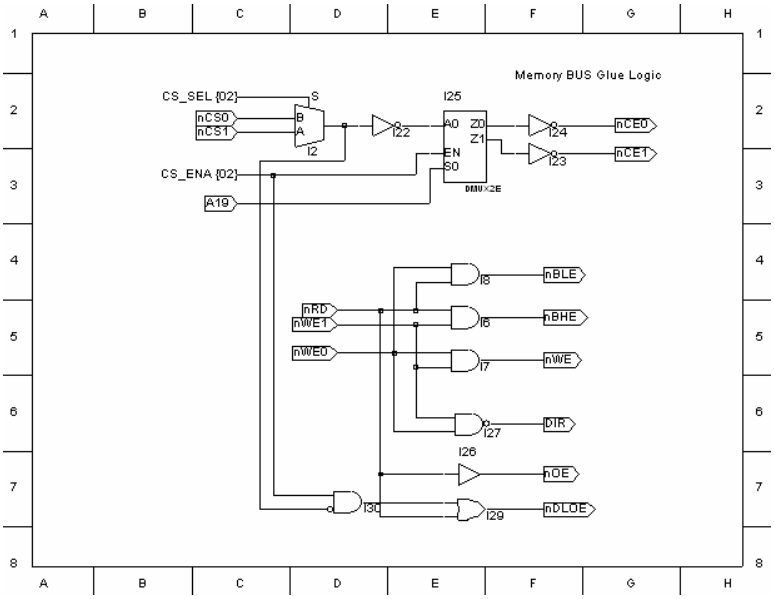
Hardware schematics and layout are available in a separate pdf document see *'Atmosfire Design'* for further details.

6.1 CPLD Design

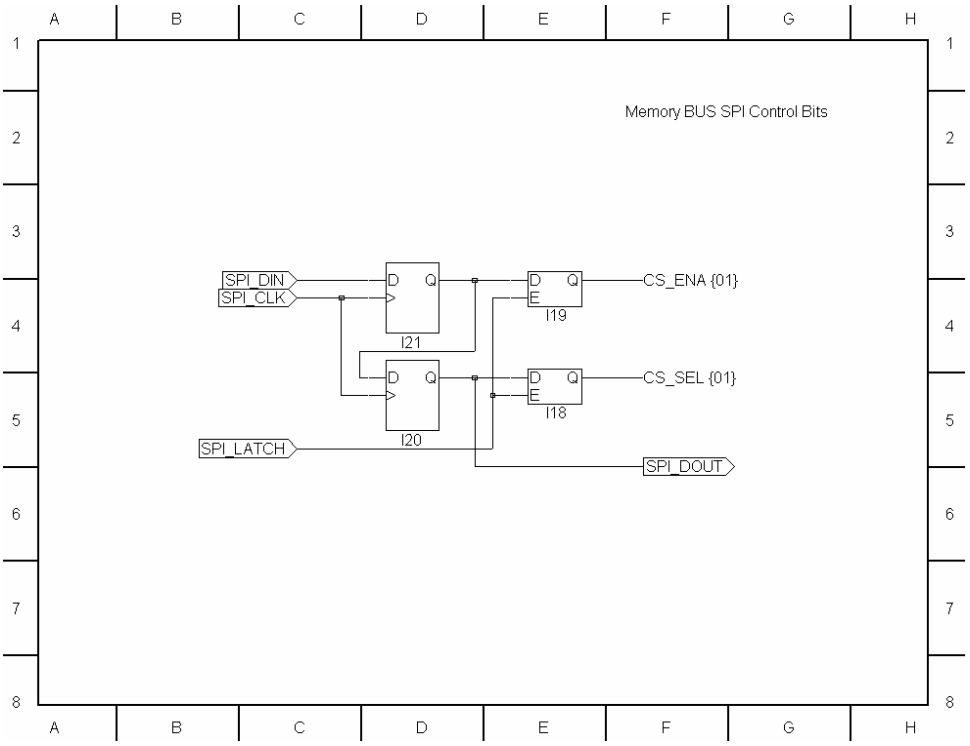
The full CPLD design can be found on the content CD, it's implemented by schematic capture and below you find the schematics.



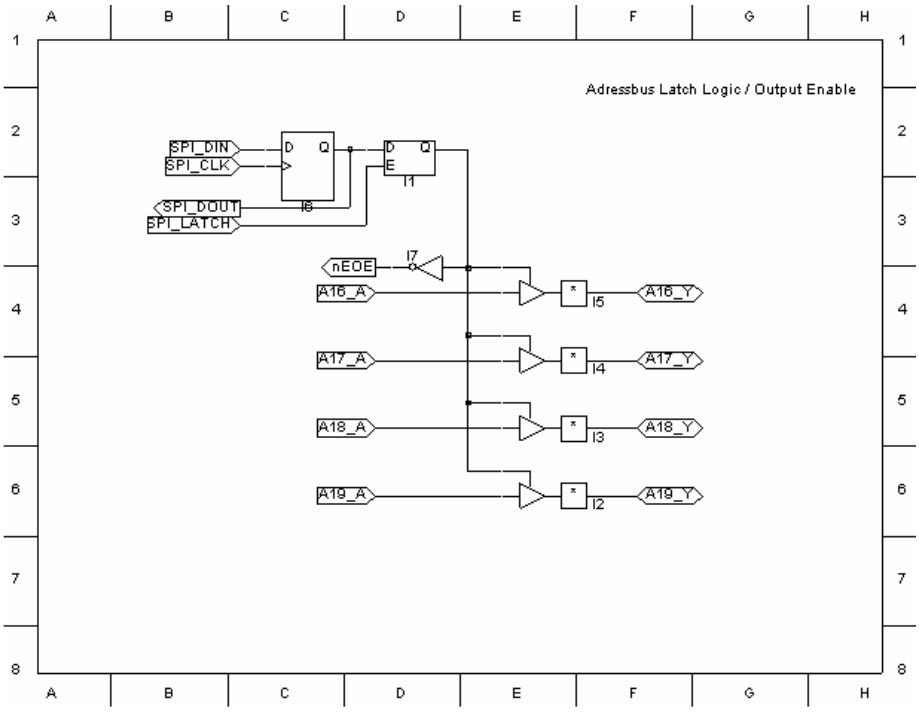
Top Level



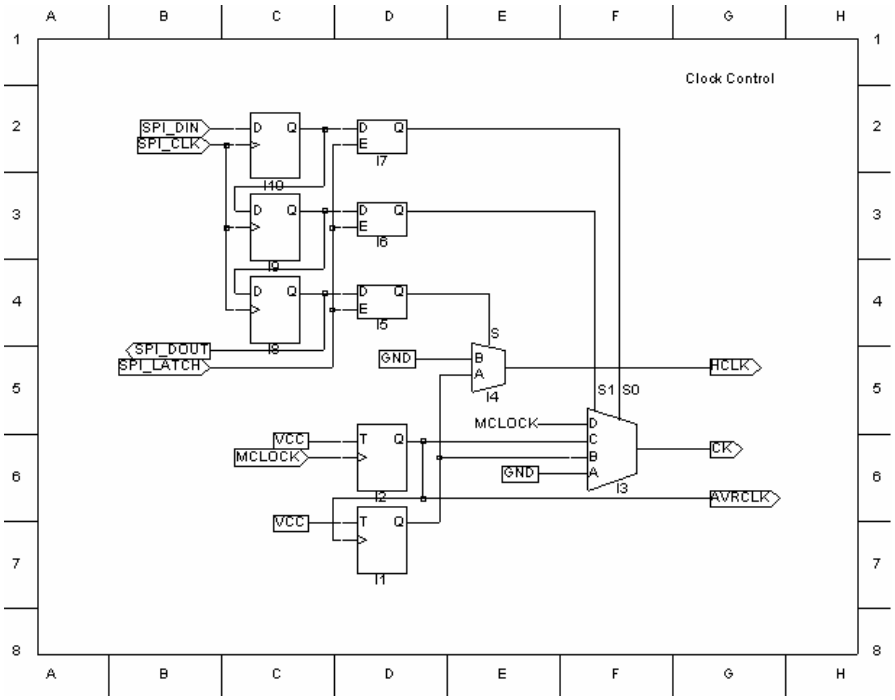
Bus Glue Logic



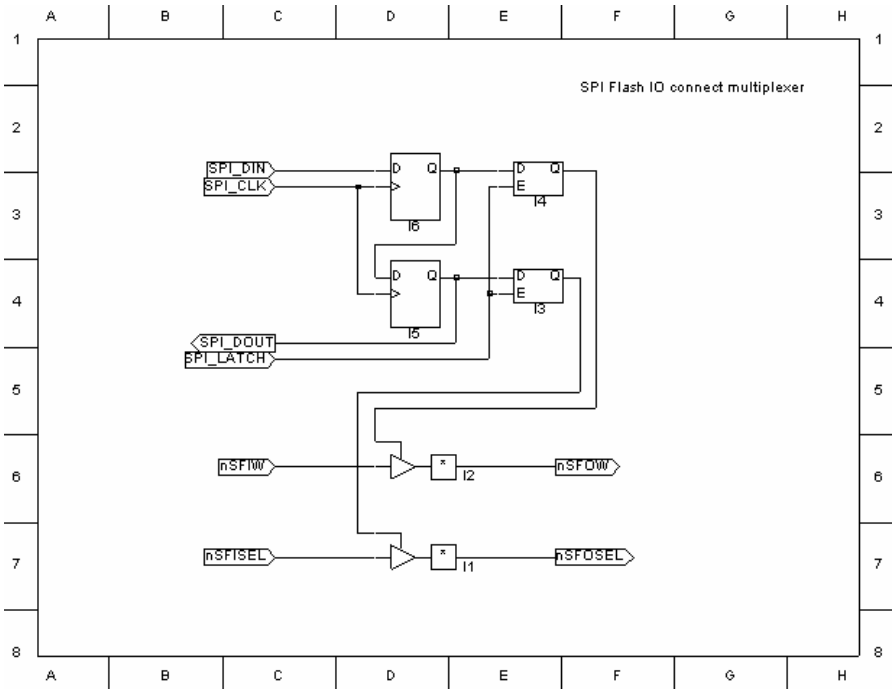
Bus Glue Logic (SPI Config)



Bus Latch



Clock Control



Serial Flash Control

This page is intentionally left blank.

Notes: