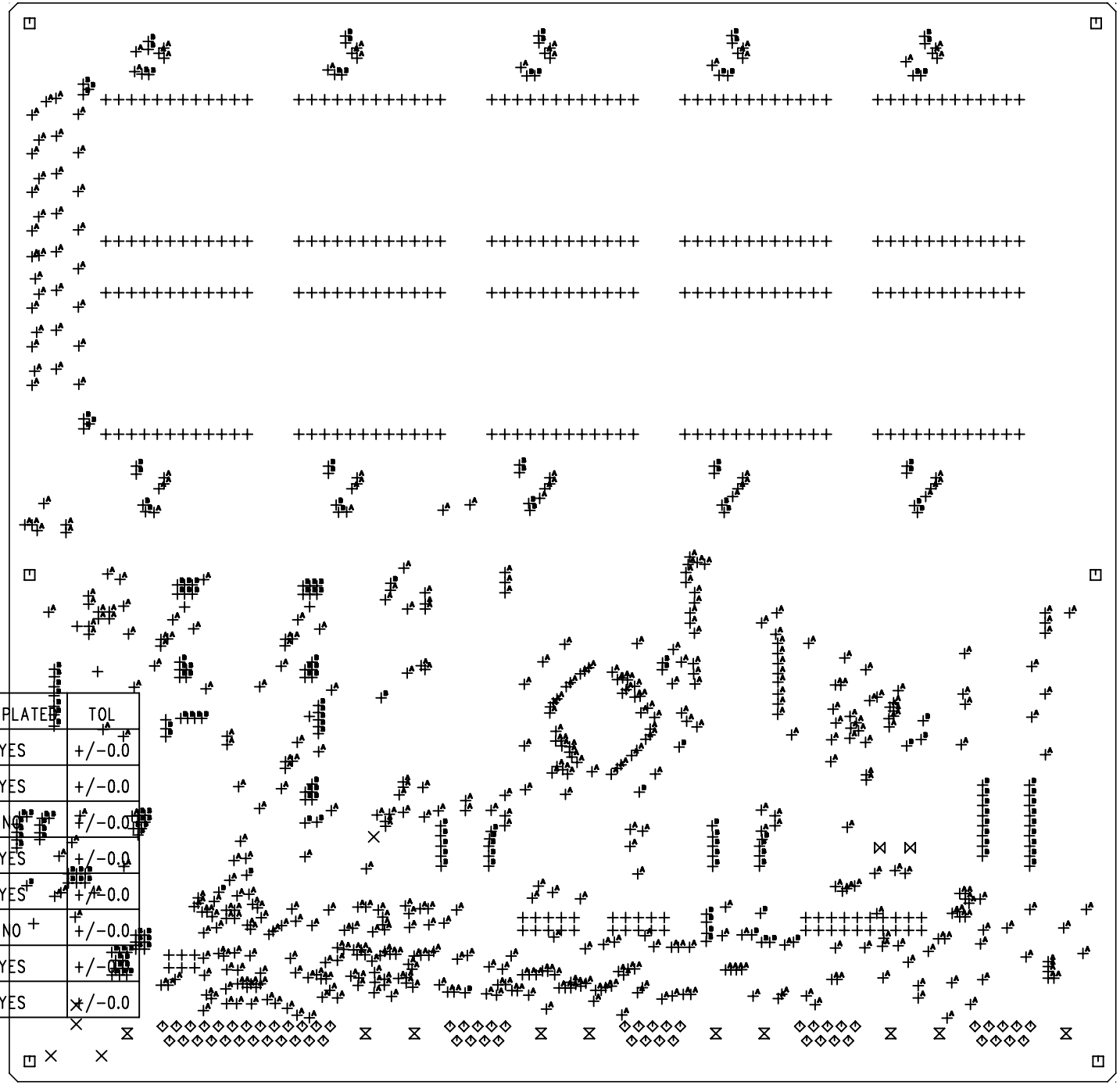
Bitfire Development Kit
Bitfire Layout
Version 1.12

ARROW ENGINEERING SWEDEN

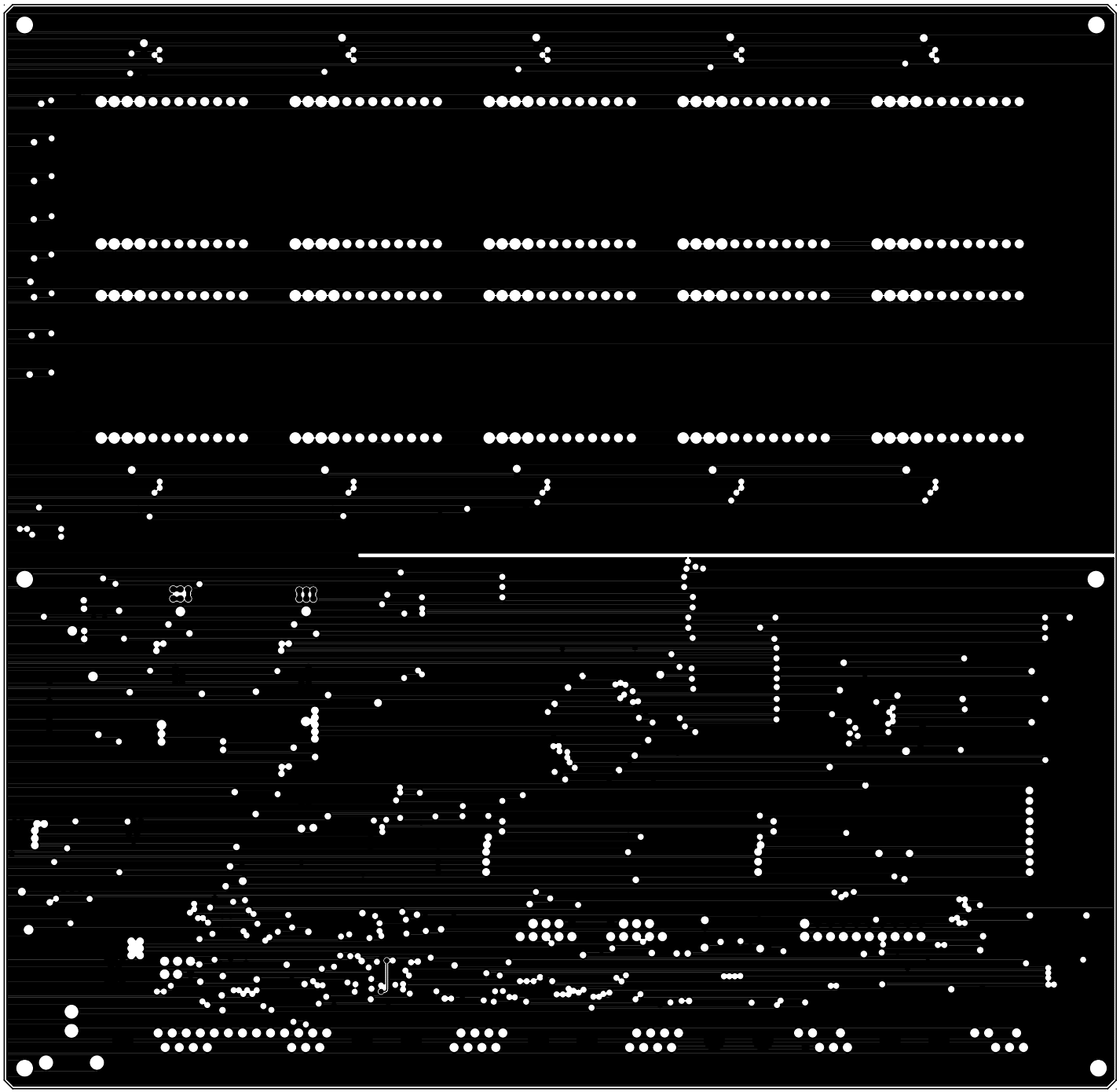
Revision History		
Version	**Date**	**Updates**
1.10	050430	Final design, ARM School edition
1.11	050707	Second spin edition; • Replaced PIC18 against the more capable ATMega48. • Added UART override support for debug controller. • Added I2C configuration support for debug controller. • Added LED traffic indicators on all UART & CAN channels with delayed flash. • Changed logos • Changed and added more origin points • Spread all DSUB's (had connector fitting issue) • Removed patch for pullup on SSEL. • Added 8MHz oscillator output with buffering. • … and some cleaning.
1.12	061011	Third spin: • Changed the whole power supply to National Semi. • Improved OCD user interface. • Corrected HW-handshaking bug • Added upstream JTAG port for addon boards • And some smaller adjustments

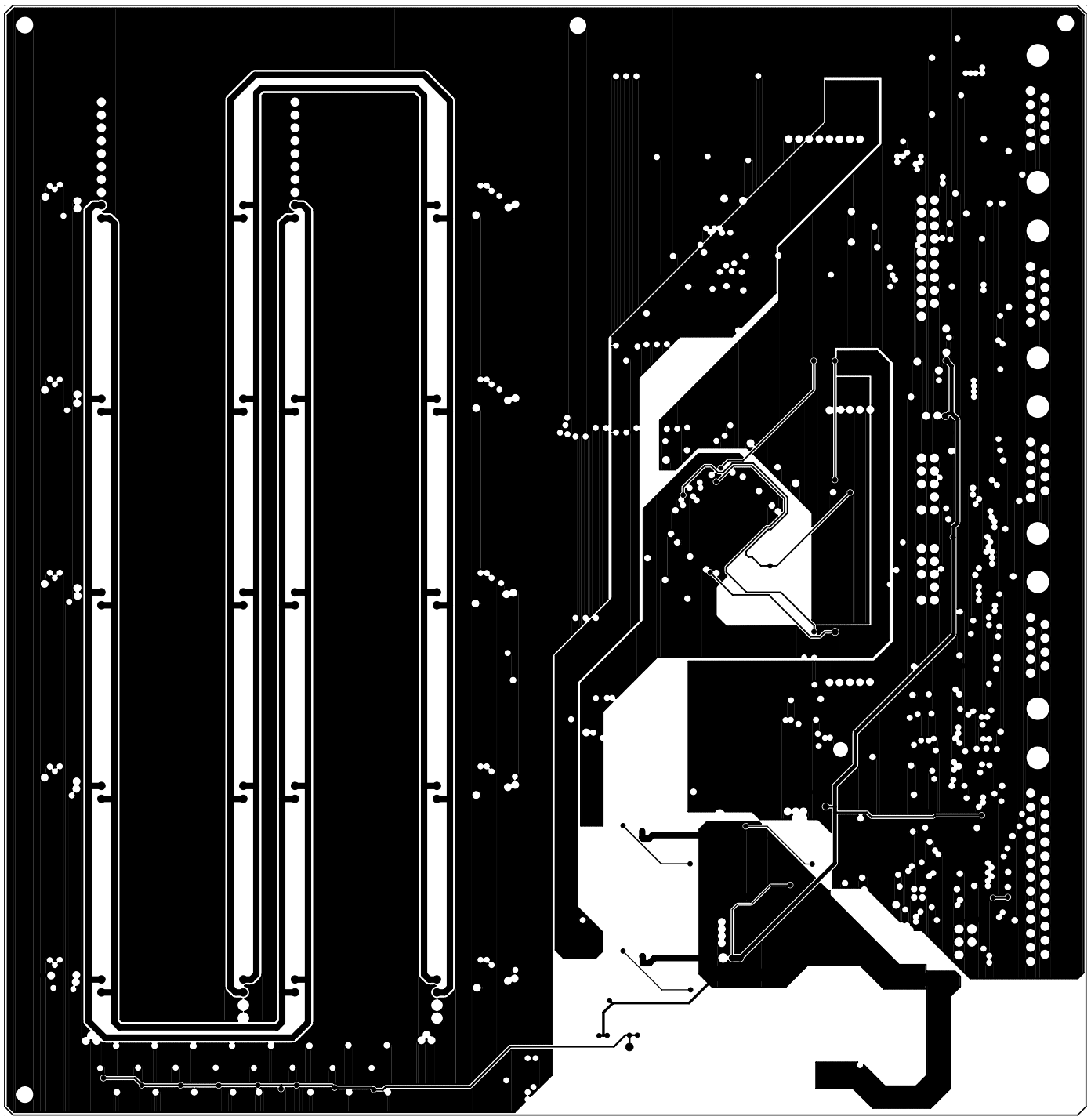
Arrow Engineering Sweden, Timmernabben, Sweden

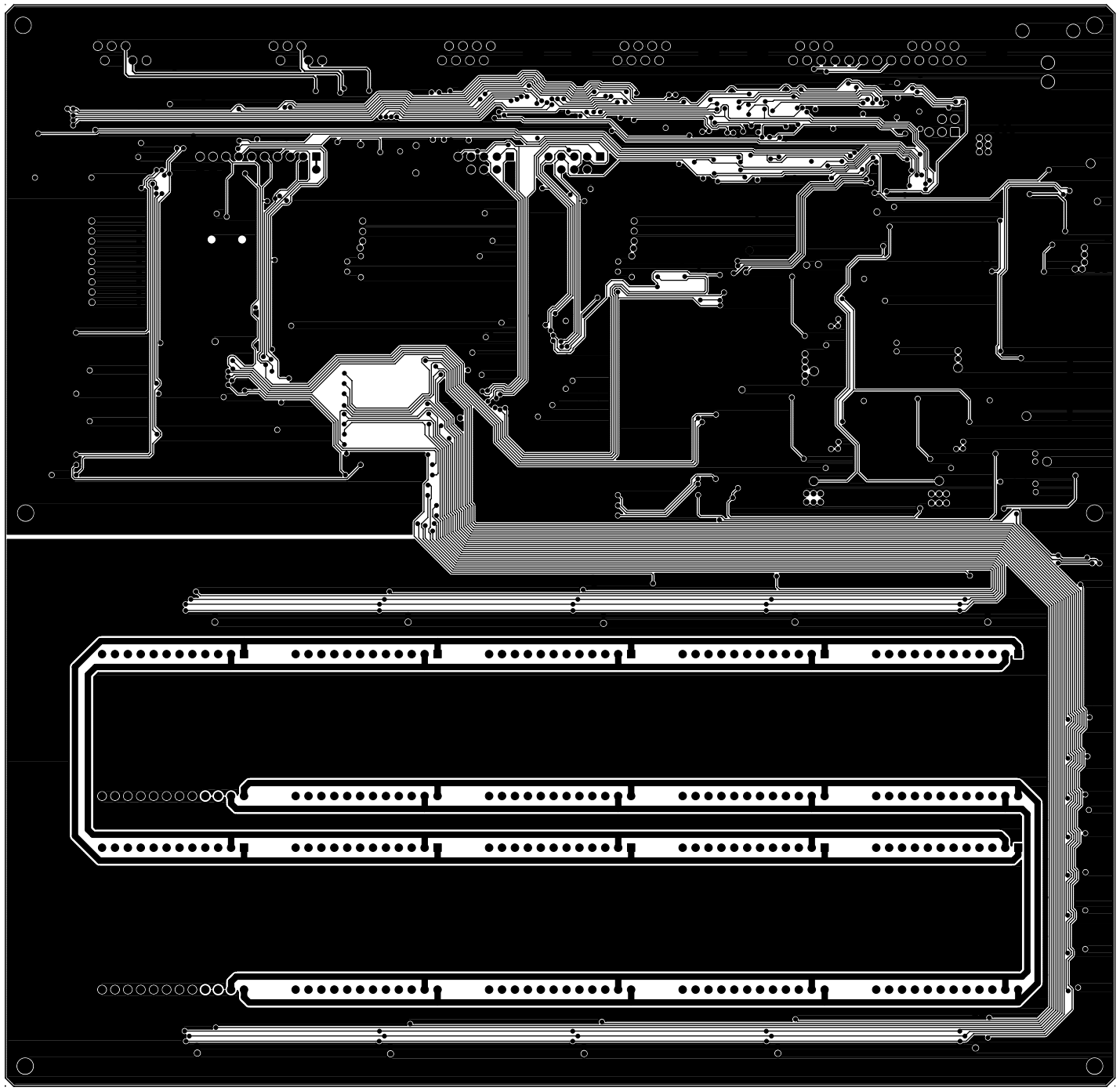


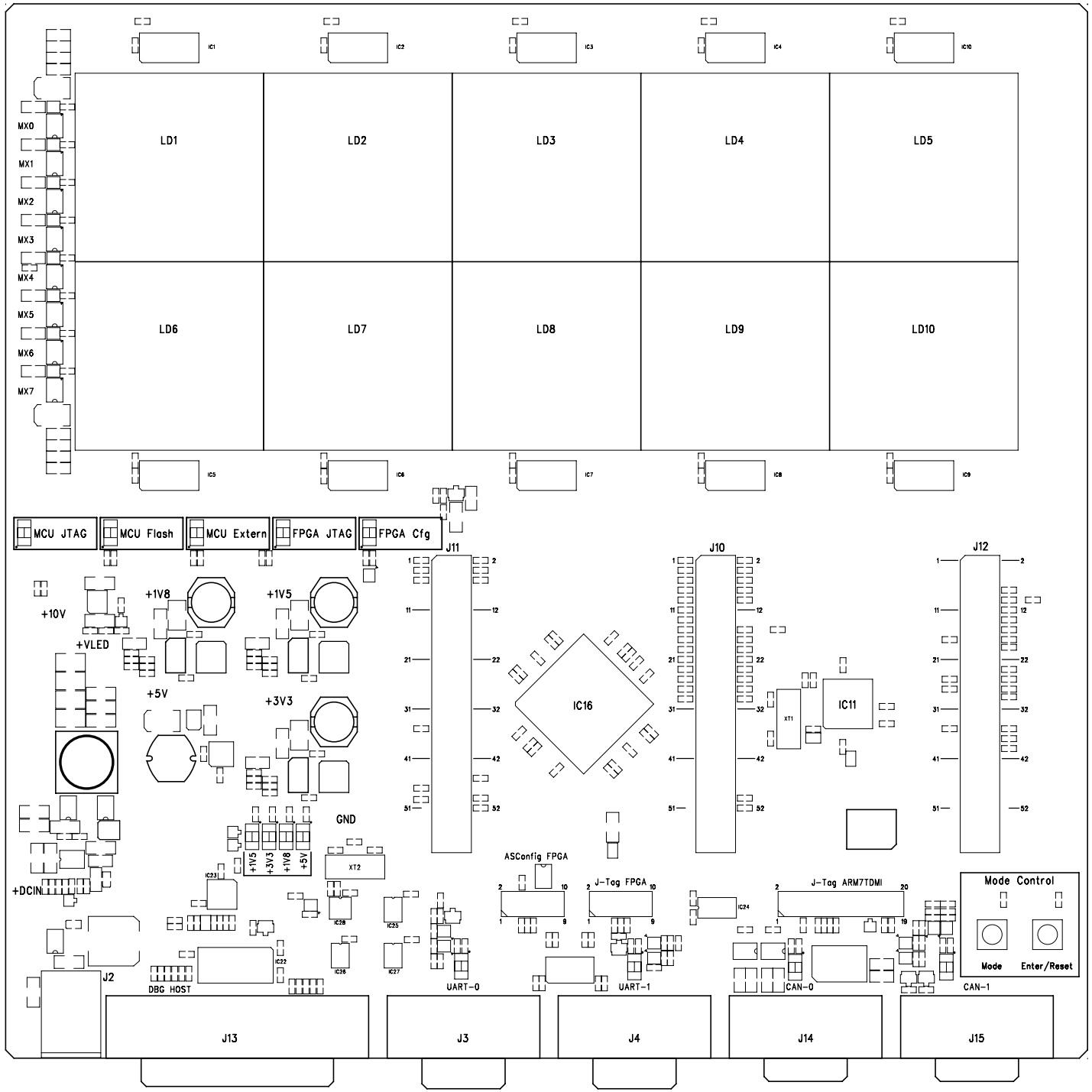
SIZE	QTY	SYM	PLATED	TOL
37	293	+	YES	+/-0.0
59	5	X	YES	+/-0.0
118	6	□	NO	+/-0.0
39	61	◇	YES	+/-0.0
122	10	⧖	YES	+/-0.0
46.85	2	⋈	NO	+/-0.0
16	533	+A	YES	+/-0.0
20	191	+B	YES	+/-0.0

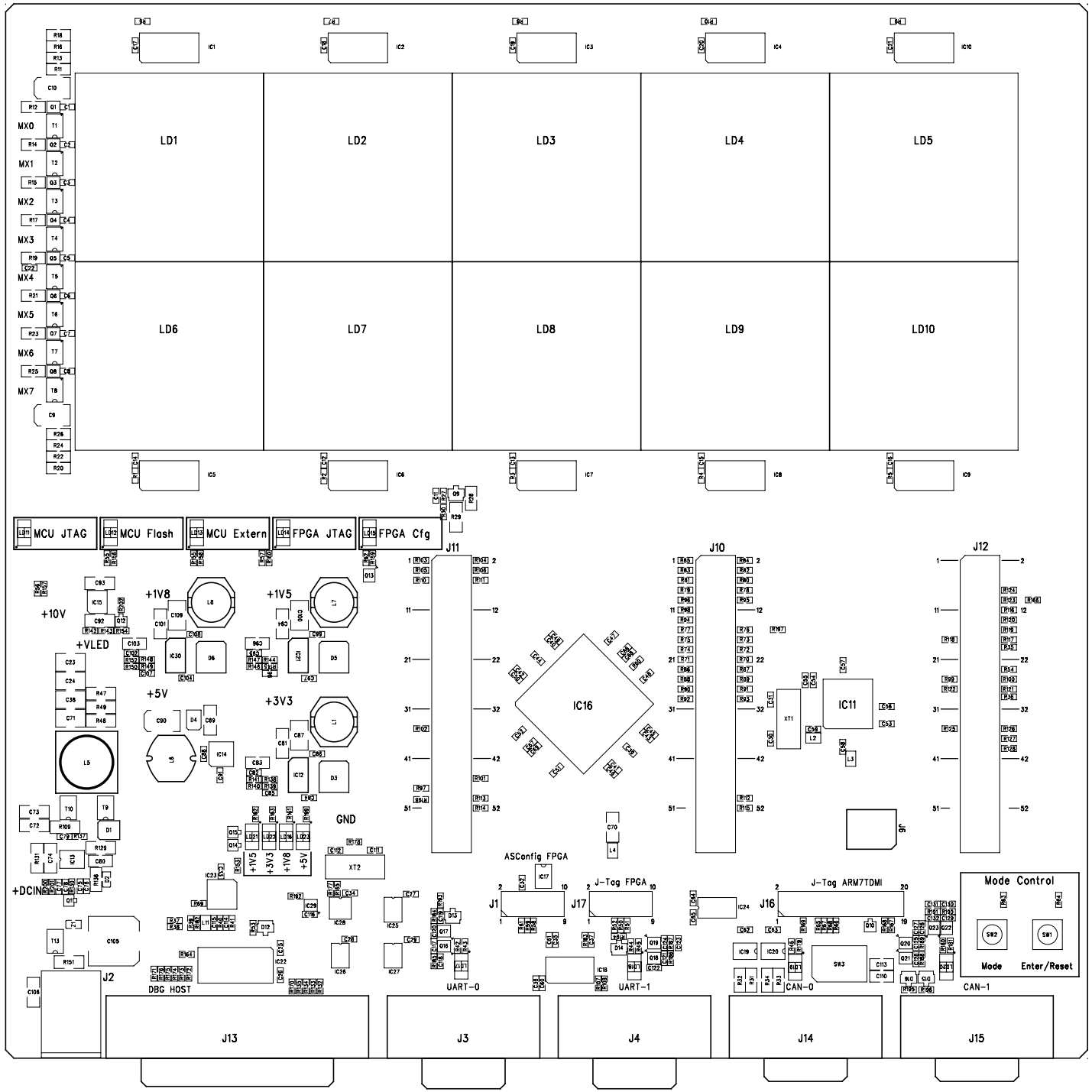
Bitfire – V1.12
Arrow Development Kit
http://www.bitfire.se
(Designed by DN & MT)
Elektronik Partner AB
ARM7 Powered By
PHILIPS
PCB supplied by
Designed By
ARROW
ARROW ENGINEERING
LCD Matrix Powered by
TOSHIBA
National Semiconductor








LD1
LD2
LD3
LD4
LD5
LD6
LD7
LD8
LD9
LD10
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
IC1
IC2
IC3
IC4
IC10
IC5
IC6
IC7
IC8
IC9
MCU JTAG
MCU Flash
MCU Extern
FPGA JTAG
FPGA Cfg
J11
J10
J12
+10V
+VLED
+1V8
+1V5
+5V
+3V3
IC16
IC11
XT1
GND
+1V5
+3V3
+1V8
+5V
XT2
IC23
IC28
IC25
IC22
IC26
IC27
+DCIN
J2
DBG HOST
UART-0
ASConfig FPGA
J-Tag FPGA
UART-1
IC24
J-Tag ARM7TDMI
CAN-0
CAN-1
Mode Control
Mode
Enter/Reset
J13
J3
J4
J14
J15


LD1
LD2
LD3
LD4
LD5
LD6
LD7
LD8
LD9
LD10
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J12
J16
J17
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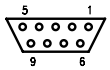
J2
J3
J4
J13
J14
J15
J6
ASConfig FPGA
J-Tag FPGA
J-Tag ARM7TDMI
Mode Control
Mode
Enter/Reset
UART-0
UART-1
CAN-0
CAN-1
DBG HOST

ARROW ENGINEERING

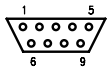
J3 & J4 (UART0 & 1)

1 – NC
2 – RXD/[B]TX/Out
3 – TXD/[B]RX/In
4 – NC
5 – GND
6 – NC
7 – RTS/[A]TX/Out
8 – CTS/[A]RX/In
9 – NC



J14 & J15 (CAN0 & 1)

1 – NC
2 – CANL
3 – GND
4 – NC
5 – GND
6 – GND
7 – CANH
8 – NC
9 – NC



J11 (FPGA Expansion #1)

*1 – P109.R0.B2/LVDS34n	*2 – P110.R0.B2/LVDS34p
*3 – P111.R0.B2/LVDS32n	*4 – P112.R0.B2/LVDS32p
*5 – P113.R0.B2/LVDS31n	*6 – P114.R0.B2/LVDS31p
7 – P119.R0.B2/DPCLK3	8 – P120/VREF0B2
9 – P121.R0.B2	10 – P122.R1.B2/LVDS27n
11 – P123.R1.B2/LVDS25n	12 – P124.R1.B2/LVDS25P
13 – P125/VREF1B2	14 – P128.R1.B2/LVDS24n
15 – P129.R1.B2/LVDS24p	16 – P130.R2.B2/LVDS23n
17 – P131.R2.B2/LVDS23p	18 – P132.R2.B2/LVDS19p
19 – P133/VREF2B2	20 – P134.R2.B2/DPCLK2
21 – P139.R2.B2/LVDS18n	22 – P140.R2.B2/LVDS18p
23 – P141.R2.B2/LVDS17n	24 – P142.R2.B2/LVDS17p
25 – P143.R2.B2/LVDS15n	26 – P144.R2.B2/LVDS15p
27 – P1.R0.B1/LVDS14p	28 – P2.R0.B1/LVDS14n
29 – P3.R0.B1/LVDS13p	30 – P4.R0.B1/LVDS13n
31 – P5/VREF0B1	32 – P6.R0.B1
33 – P7.R0.B1/LVDS12p	34 – P10.R0.B1/DPCLK1
*35 – P11/VREF1B1	36 – P26.R1.B1/PLL1_OUTp
37 – P27.R1.B1/PLL1_OUTn	38 – P28.R2.B1/DPCLK0
39 – P31/VREF2B1	40 – P32.R2.B1
41 – P33.R2.B1/LVDS1p	42 – P34.R2.B1/LVDS1n
43 – P35.R2.B1/LVDS0p	44 – P36.R2.B1/LVDS0n
*45 – CLK0.R1.B1/LVDSCK0p	*46 – CLK1.R1.B1/LVDSCLK0n
*47 – CLK2.R1.B3/LVDSCK2p	48 – CLK3.R1.B3/LVDSCLK2n
49 – GND	50 – VCCIOB3 (std +3V3)
51 – GND	52 – VCCIOB2 (std +3V3)
53 – GND	54 – +1V5
55 – GND	56 – +1V5
57 – GND	58 – +1V5
59 – GND	60 – +1V5

J10 (FPGA Expansion #2)

*1 – P108.R0.B3/LVDS35p	*2 – P107.R0.B3/LVDS35n
*3 – P106.R0.B3/LVDS36p	*4 – P105.R0.B3/LVDS36n
*5 – P104/VREF0B3	*6 – P103.R0.B3
*7 – P100.R0.B3/DPCLK4	*8 – P99.R0.B3/LVDS38p
*9 – P98.R0.B3/LVDS38n	*10 – P97.R0.B3/LVDS39p
*11 – P96/VREF1B3	*12 – P85.R2.B3/LVDS47n
*13 – P84.R2.B3/LVDS48p	14 – P83.R2.B3/LVDS48n
*15 – P82.R2.B3/DPCLK5	*16 – P79/VREF2B3
*17 – P78.R2.B3/LVDS49p	*18 – P77.R2.B3/LVDS49n
*19 – P76.R2.B3/LVDS50p	*20 – P75.R2.B3/LVDS50n
*21 – P74.R2.B3/LVDS51p	*22 – P73.R2.B3/LVDS51n
*23 – P72.R0.B4/LVDS52n	*24 – P71.R0.B4/LVDS52p
*25 – P70.R0.B4/LVDS54n	*26 – P69.R0.B4/LVDS54p
*27 – P68.R0.B4/LVDS55n	*28 – P67.R0.B4/LVDS55p
*29 – P62.R0.B4/DPCLK6	30 – P61/VREF0B4
31 – P60.R0.B4	32 – P59.R1.B4/LVDS59n
33 – P58.R1.B4/LVDS61n	34 – P57.R1.B4/LVDS61p
35 – P56/VREF1B4	36 – P53.R1.B4/LVDS62n
37 – P52.R1.B4/LVDS62p	38 – P51.R2.B4/LVDS63n
39 – P50.R2.B4/LVDS63p	40 – P49.R2.B4/LVDS67p
41 – P48/VREF2B4	42 – P47.R2.B4/DPCLK7
43 – P42.R2.B4/LVDS68n	44 – P41.R2.B4/LVDS68p
45 – P40.R2.B4/LVDS69n	46 – P39.R2.B4/LVDS69p
47 – P38.R2.B4/LVDS71n	48 – P37.R2.B4/LVDS71p
49 – GND	50 – VCCIOB4 (std +3V3)
51 – GND	52 – VCCIOB1 (std +3V3)
53 – GND	54 – +1V5
55 – GND	56 – +1V5
57 – GND	58 – +1V5
59 – GND	60 – +1V5

J12 (ARM7 Expansion)

1 – P0.18/CAP1.3/MISO1/MAT1.3	2 – P0.19/MAT1.2/MOSI1/CAP1.2
3 – P0.20/MAT1.3/SSEL1/EINT3	*4 – MCU RESET
5 – P1.20/TRACESYNC	6 – P0.17/CAP1.2/SCK1/MAT1.2
7 – P0.16/EINT0/MAT0.2/CAP0.2	*8 – P0.15/RI1/EINT2
9 – P1.21/PIPESTAT0	*10 – P0.14/DCD1/EINT1
11 – P1.22/PIPESTAT1	*12 – P0.13/DTR1/MAT1.1
*13 – P0.12/DSR1/MAT1.0	*14 – P0.11/CTS1/CAP1.1
15 – P1.23/PIPESTAT2	*16 – P0.10/RTS1/CAP1.0
*17 – P0.9/RXD1/PWM6/EINT3	*18 – P0.8/TXD1/PWM4
19 – P1.24/TRACECLK	20 – P0.7/SSEL0/PWM2/EINT2
*21 – P0.6/MOSI0/CAP0.2	*22 – P0.5/MISO0/MAT0.1
23 – P1.25/EXTIN0	*24 – P0.4/SCK0/CAP0.1
*25 – P0.3/SDA/MAT0.0/EINT1	*26 – P0.2/SCL/CAP0.0
*27 – P0.1/RXD0/PWM3/EINT0	*28 – P0.0/TXD0/PWM1
29 – P1.16/TRACEPKT0	30 – P0.30/AIN3/EINT3/CAP0.0
31 – P0.29/AIN2/CAP0.3/MAT0.3	32 – P0.28/AIN1/CAP0.2/MAT0.2
33 – P1.17/TRACEPKT1	34 – P0.27/AIN0/CAP0.1/MAT0.1
*35 – TD1	*36 – P0.25/RD1
37 – P1.18/TRACEPKT2	*38 – P0.24/TD2
39 – P1.19/TRACEPKT3	*40 – P0.23/RD2
41 – P0.22/CAP0.0/MAT0.0	42 – P0.21/PWM5/CAP1.3
43 – GND	44 – +3V3
45 – GND	46 – +3V3
47 – GND	48 – +3V3
49 – GND	50 – +3V3
51 – GND	52 – +1V8
53 – GND	54 – +1V8
55 – GND	56 – +1V8
57 – GND	58 – +1V8
59 – GND	60 – +1V8

* = Signal used for onboard function, caution when used externally.
(Most signals can be deattached by removing resistor – see docs)

Wiggler

J16 (ARM J-TAG)

1 – VCC	2 – VCC
3 – TRST	4 – GND
5 – TDI	6 – GND
7 – TMS	8 – GND
9 – TCK	10 – GND
11 – RTCK	12 – GND
13 – TDO	14 – GND
15 – RESET	16 – GND
17 – PULLD	18 – GND
19 – PULLD	20 – GND

ByteBlaster – II

J1 (FPGA Config)

1 – DCLK	2 – GND
3 – CONF_DONE	4 – VCC
5 – NCONFIG	6 – NCE
7 – DATAOUT	8 – DCLK
9 – ASDI	10 – GND

J17 (FPGA J-TAG)

1 – TCK	2 – GND
3 – TDO	4 – VCC
5 – TMS	6 – NC
7 – NC	8 – NC
9 – TDI	10 – GND

ISP Connector

Input Power
10–23VDC
Max 50W