LPC2129 ARM7TDMI-S

Philips Implementation

ARMSchool 2005 Bitfire Workshop, Gothenburg

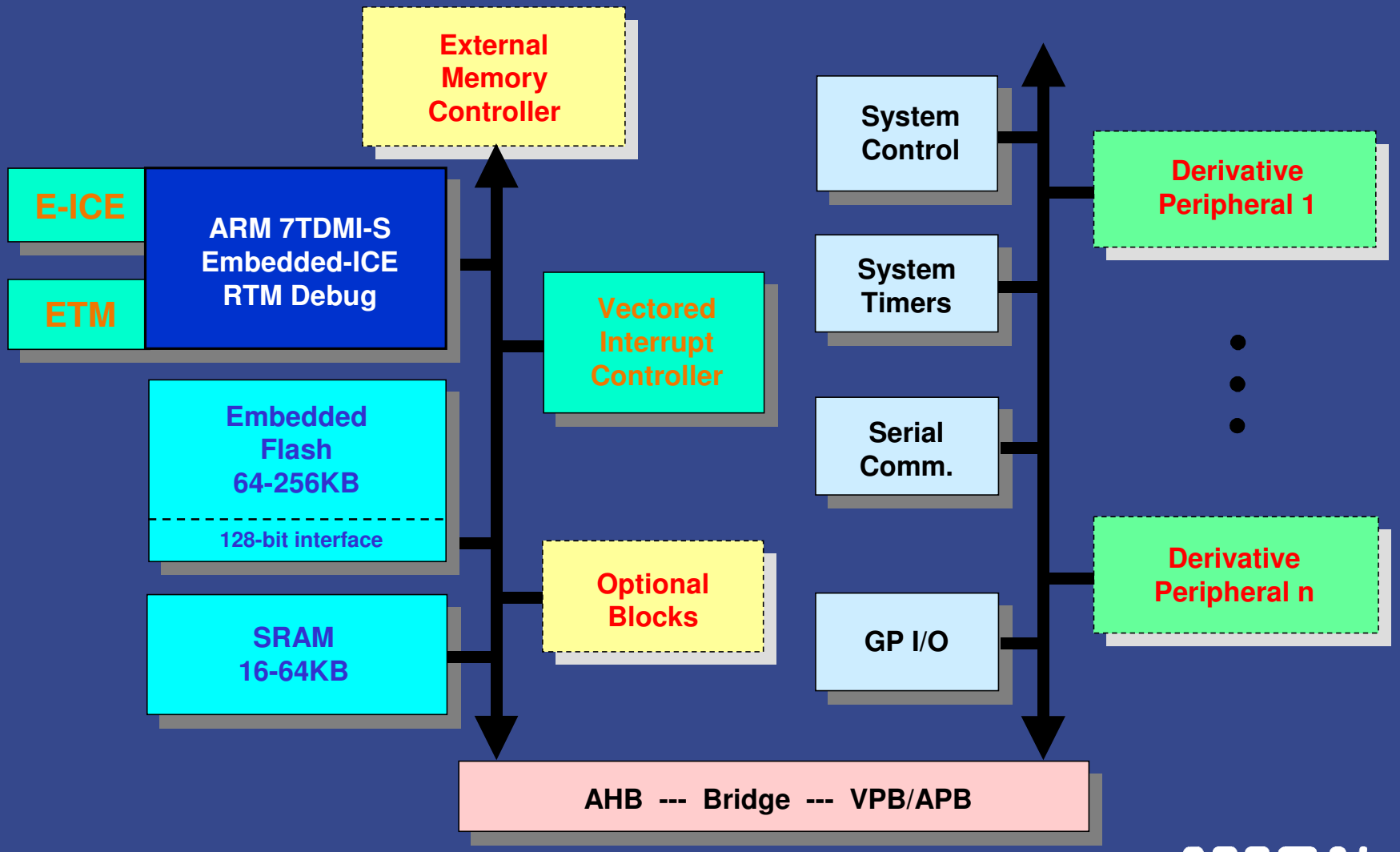
2005-10-25

Powering the Supply Chain.SM

Philips LPC2xxx family

- Shared system architecture
  - 32-bit ARM7TDMI-S core
  - E-ICE RTM™ to support real-time debugging
  - ETM™ to perform real-time tracing of the code being executed
  - Vectored Interrupt Controller (ARM Prime Cell™)
- All derivatives share
  - high-bandwidth 128-bit Flash and on-chip programming interface
  - memory map and interrupt structure
  - ARM PrimeCell™ and Philips peripheral IP
  - low-cost, high-volume production packages

Philips LPC2xxx family

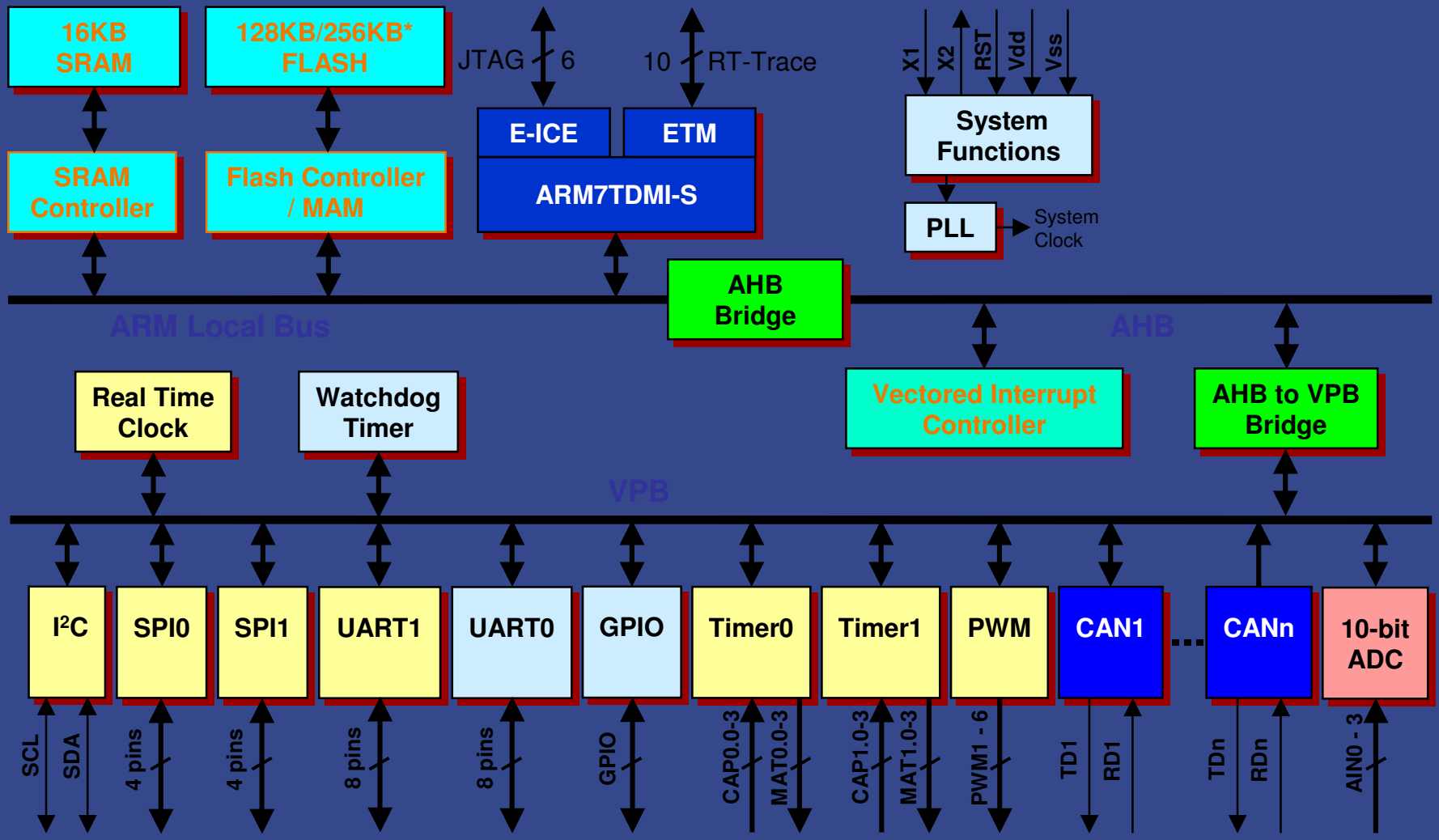


Philips LPC2xxx family

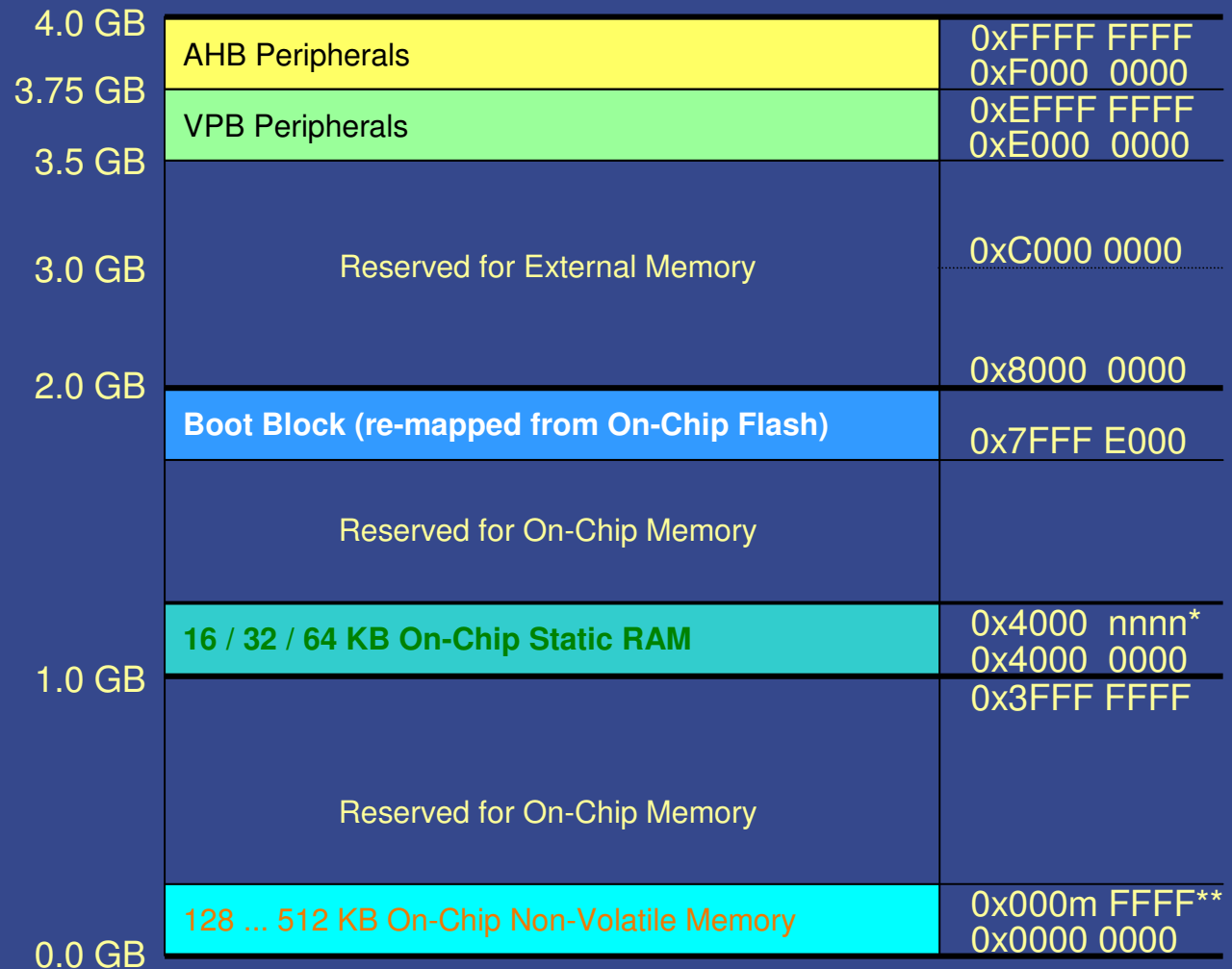
- Some common features
  - ARM7TDMI-S core with E-ICE RTM™ / ETM™
  - Operation up to 60MHz
  - 32-bit timers
    - 2 (4 capture and 4 compare channels each)
    - PWM (6 outputs)
    - RTC
    - Watchdog
  - 2 UARTs (16C550)
  - I²C (400kb/s)

*Flash size:	LPC2119	128KB
	LPC2129	256KB
	LPC2194	256KB

LPC2119, LPC2129, LPC2194



Memory Map



Memory blocks not drawn to scale!

*: nnnn	RAM
FFFF	64KB
7FFF	32KB
3FFF	16KB

**: m	Flash
1	128KB
3	256KB
7	512KB

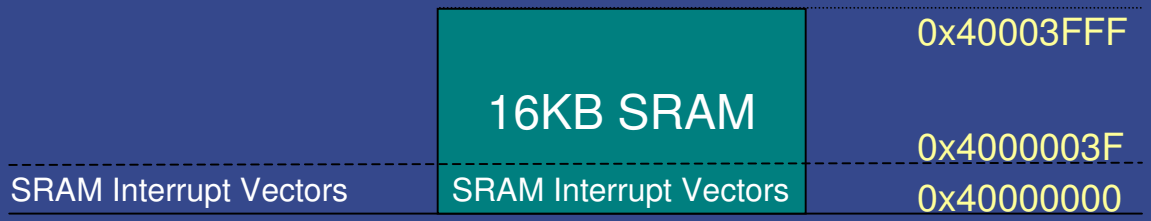
Flash


128KB
8K Boot Block
0x1FFFF
Sector 14 8K
Sector 13 8K
Sector 12 8K
Sector 11 8K
Sector 10 8K
Sector 9 8K
Sector 8 8K
Sector 7 8K
Sector 6 8K
Sector 5 8K
Sector 4 8K
Sector 3 8K
Sector 2 8K
Sector 1 8K
Sector 0 8K
0x0
Active Exception Vectors
0x3F
0x00
256KB
8K Boot Block
0x3FFFF
Sector 16 8K
Sector 15 8K
Sector 14 8K
Sector 13 8K
Sector 12 8K
Sector 11 8K
Sector 10 8K
Sector 9 64K
Sector 8 64K
Sector 7 8K
Sector 6 8K
Sector 5 8K
Sector 4 8K
Sector 3 8K
Sector 2 8K
Sector 1 8K
Sector 0 8K
0x0

SRAM

LPC2119

LPC2129



System Control

- Includes a number of important system features
  - Power Control
  - Memory mapping configuration
  - Oscillator
  - PLL
  - VPB divider
  - Reset (active low)
  - Wakeup Timer
  - External Interrupts

Boot Block

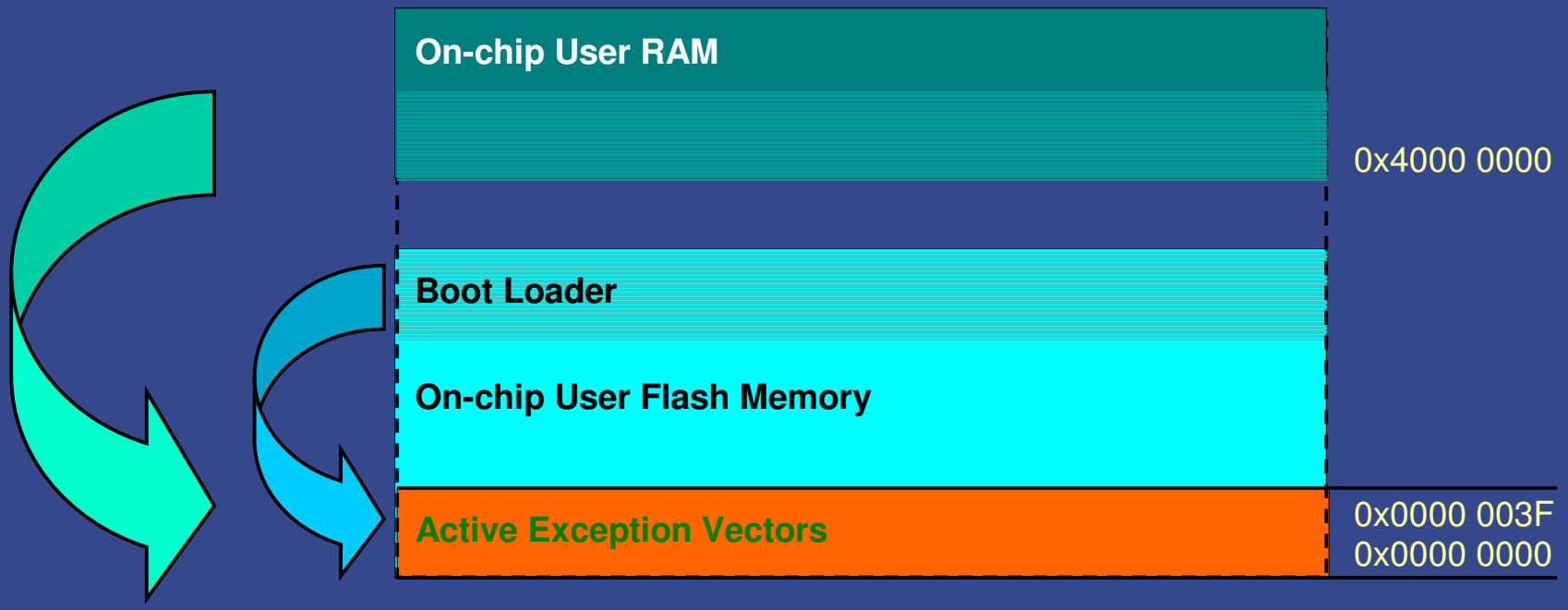
- The uppermost Flash sector contains the Boot Loader
  - controls physical interface for programming and erasing the Flash
  - supports ISP mode for initial programming of customer code
  - supports In-Application Programming in a running system under the control of customer software
  - buffers an entire Flash line (512 bytes) at once to keep programming time to a minimum
- The Boot Loader is automatically run following reset
  - checks for a “Valid User Program” key to prevent running code on incorrectly programmed devices

Memory Mapping Control

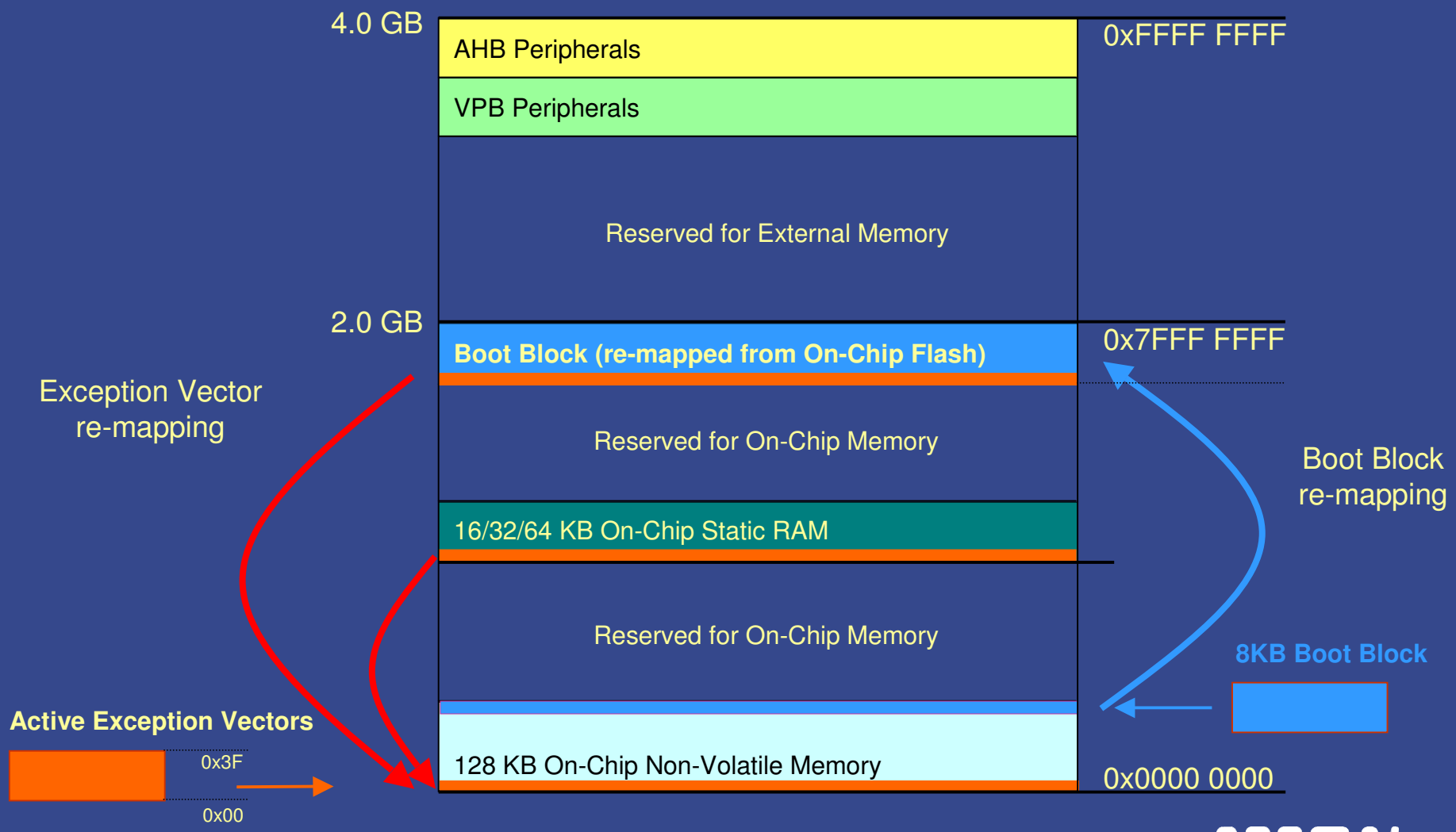
- Re-mapping of **Exception Vectors**
  - always appear to begin at 0x0000 0000
  - but can be mapped from different sources

Memory Mapping Control

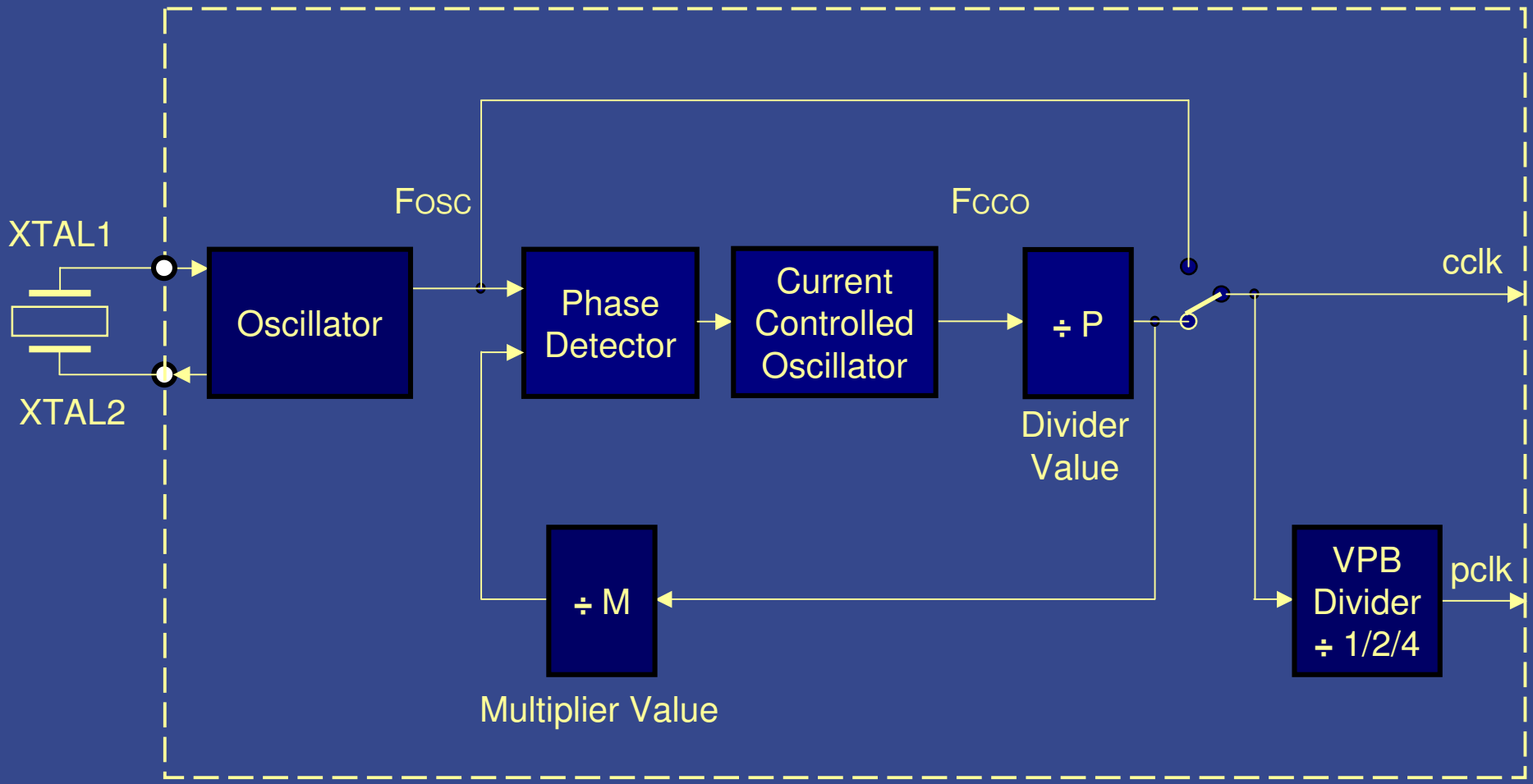
- Boot Loader Always executed after reset. **Exception Vectors** re-mapped from Boot Block



Memory Mapping Overview



Phase Locked Loop



VPB Divider Register

- VPB Divider Register [VPBDIV – 0xE01FC100] R/W

VPBDIV 1:0	VPBDIV	cclk / pclk ratio 00: 4 01: 1 10: 2

On-chip Memory with 0-wait States

- ARM7TDMI-S is a 1-clock core
  - CPI of ~1.9, but many instructions execute in 1 cycle
  - CPU requires one instruction per clock cycle

For highest performance:

32 bits needed with every clock

- Memory access time < 17ns @ 60MHz

General Purpose I/O

- Pins available for GPIO:
  - 48-pin devices: 32
  - 64-pin devices: 46
  - 144 pin devices: 76 (with external memory)
    112 (w/o external memory)
- Shared with
  - Alternate functions of all peripherals
  - Data/address bus and strobe signals for external memories

General Purpose I/O

- Direction control of individual bits
- Separate set and clear registers
- Pin value and output register can be read separately
- Slew rate controlled outputs (10 ns)
- 5 registers used to control I/Os

General Purpose I/O

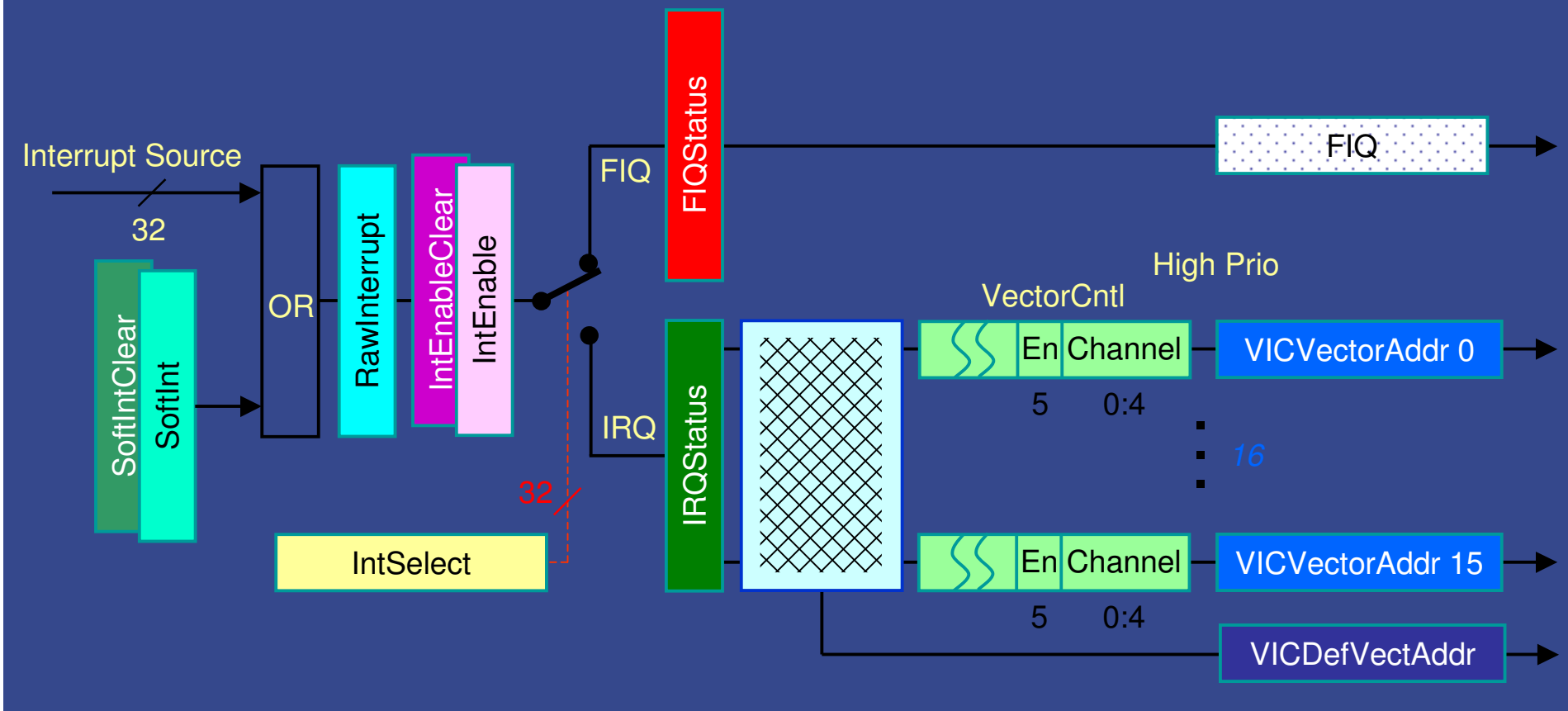
Register

IOPIN	IOSET	IOCLR	IODIR	PINSEL

Vectored Interrupt Controller

- ARM PrimeCell™
- 32 interrupt request inputs
- 16 IRQ interrupts can be auto-vectored
  - Single instruction vectoring to ISR
  - Dynamic software priority assignment
- 16 non-vectored interrupts
- Software interrupts

Vectored Interrupt Controller



Interrupt Latency

- FIQ: 200ns @ 60MHz (worst case 12 cycles)
- IRQ: 416ns @ 60MHz (worst case 25 cycles)

A/D Converter

- Features
  - 10 bit successive approximation analog to digital converter
  - Multiplexed inputs
    - 4 pins (64-pin devices)
    - 8 pins (144-pin devices)
  - Power down mode
  - Measurement range 0V ... 3V
  - Minimum 10 bit conversion time: 2.44 µS
  - Burst conversion mode for single or multiple inputs
  - Optional conversion on transition on input pin or Timer Match signal
  - Programmable divider to generate required 4.5MHz from VPB clock

UARTs

- UART 0, UART 1
  - 16 byte Receive and Transmit FIFOs
  - PC UART 16C550 “look-alike”
  - Built-in baud rate generator
  - Supports 6 modem control signals
    - CTS, RTS, DCD, DSR, DTR and RI functions are selectable
    - Note:

      UART 0 has Tx and Rx pins only

I²C Bus

- Fast-I²C compliant bus interface
  - Configurable as Master, Slave, or both
  - Multi-master bus
  - Bi-directional data transfer between masters and slaves
  - Up to 400kb/s
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Programmable clock rate

SPI Bus

- Compliant with Serial Peripheral Interface (SPI) specification
- Combined SPI master and slave function
- Maximum data bit rate of 1/8 of the peripheral clock rate
- Programmable clock polarity and phase for data transmit/receive operations
- No. of SPI channels:
  - 1 (48-pin devices)
  - 2 (64/144-pin devices)

CAN Bus

- CAN **(Controller Area Network)** features
  - Serial communications protocol
  - Efficiently supports distributed real-time control
  - Very high level of security
  - Application domain: high speed networks to low cost multiplex wiring
- LPC2xxx with CAN have 2 or 4 CAN channels
  - Can be used as gateway, switch or router among CAN buses
  - Industrial or automotive applications

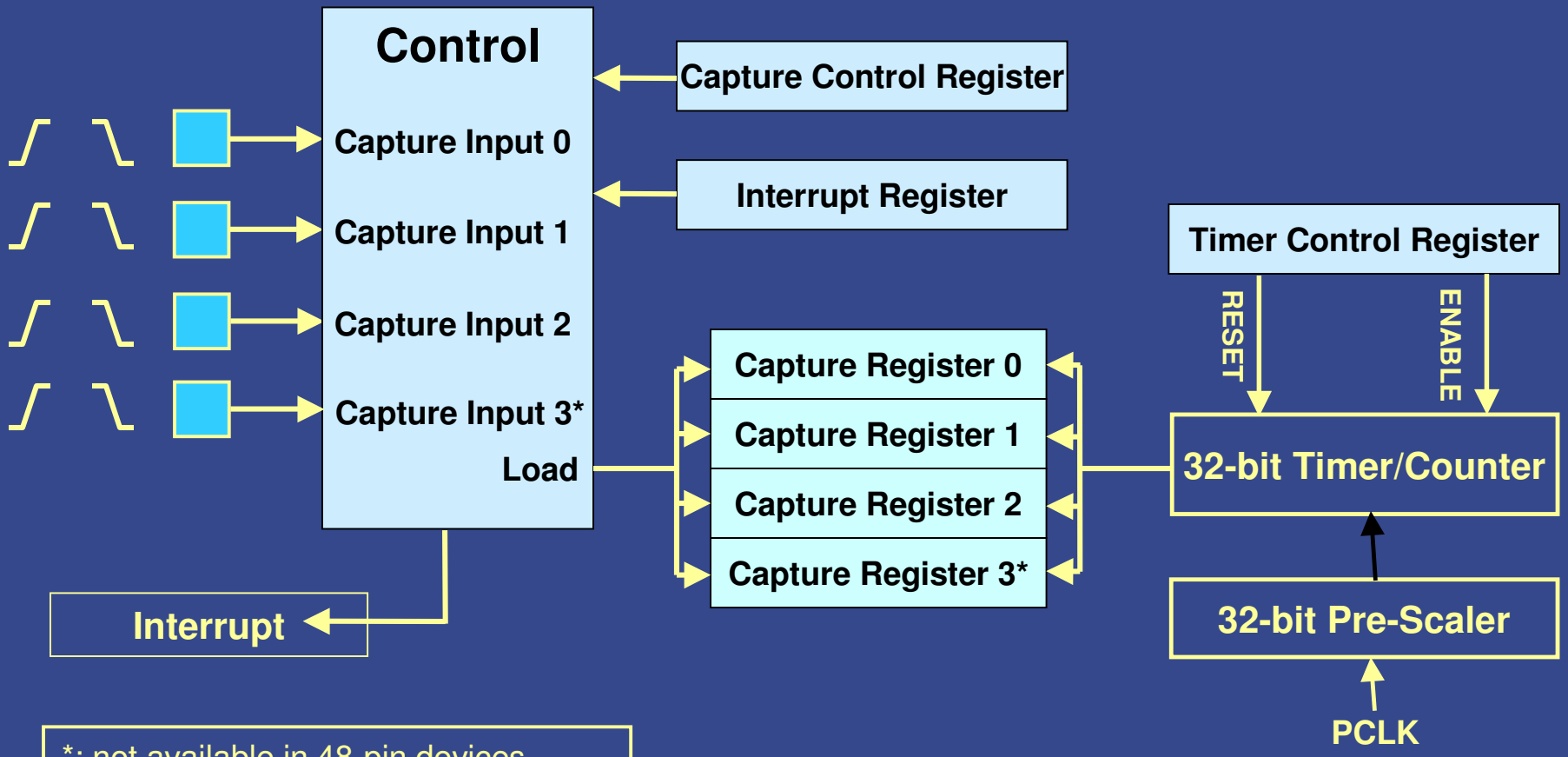
CAN Bus

- Data rates to 1 Mbit/s on each bus
- 32-bit register and RAM access
- Compatible with CAN specification 2.0B, ISO 11898-1
- Global Acceptance Filter recognizes 11- and 29-bit Rx Identifiers for all CAN buses
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers
- No. of CAN channels
  - 2 on LPC2119, LPC2129, LPC2290, LPC2292
  - 4 on LPC2194, LPC2294

Timer 0 and 1

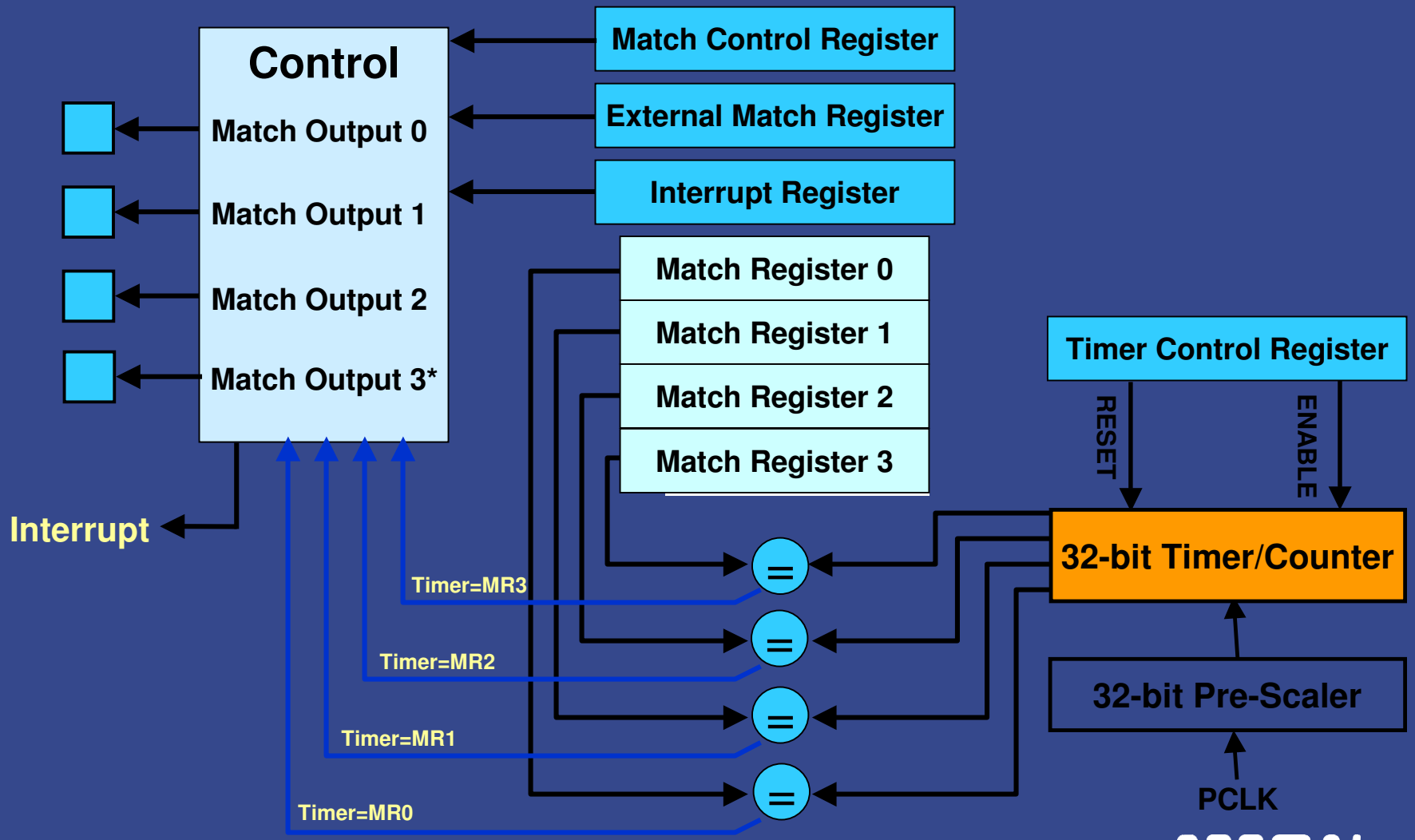
- 32-bit Timer
- 32-bit Capture Registers and Capture Pins
  - Four on each timer (48-pin devices three on Timer 0 and four on Timer 1)
  - Capture event can optionally trigger an interrupt
- 32-bit Match Registers and Match Pins
  - Four on each timer (48-pin devices three on Timer 0 and four on Timer 1)
  - Interrupt, timer reset or timer halt on match
  - Match output can toggle, go high, go low or do nothing

Timer Capture



*: not available in 48-pin devices

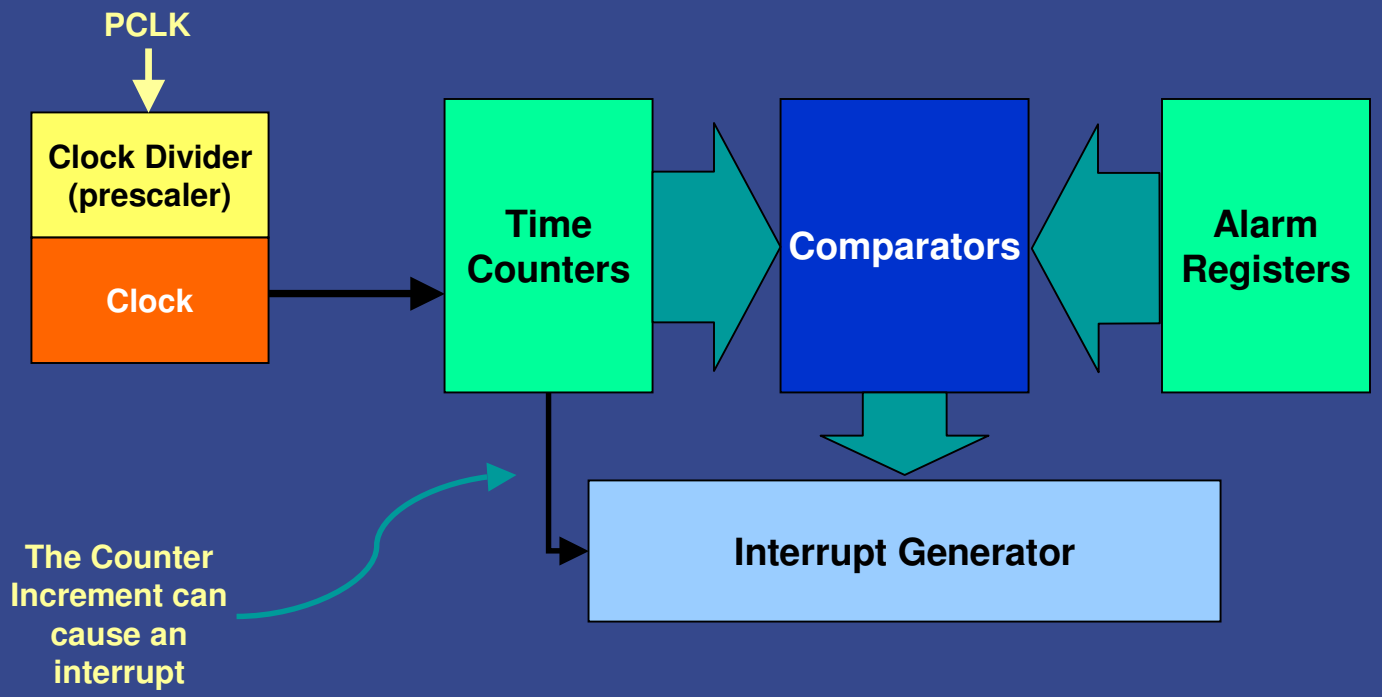
Timer Compare



Real Time Clock

- Full Clock/Calendar function with alarms
  - Generates its own 32.768 kHz reference clock from any crystal frequency
  - Counts seconds, minutes, hours, day of month, month, year, day of week and day of year
  - Can generate an interrupt or set an alarm flag for any combination of the counters

Real Time Clock



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