

Course: CSC258F

Professor: Steve Engels

Experimenter: Yuhao Yang

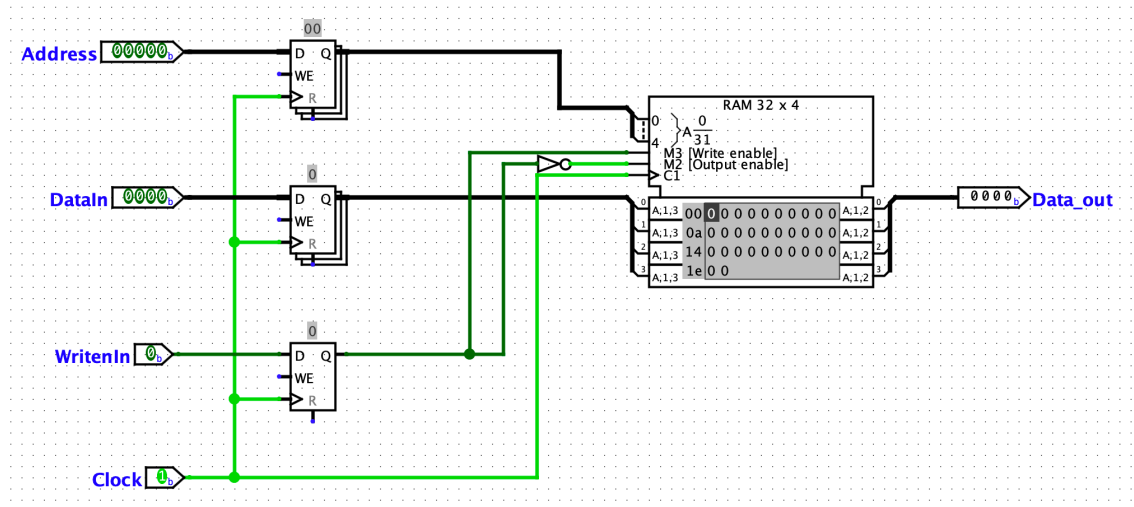
Student ID: 1005808057

Lab7

Pre-Lab Report

Part1:

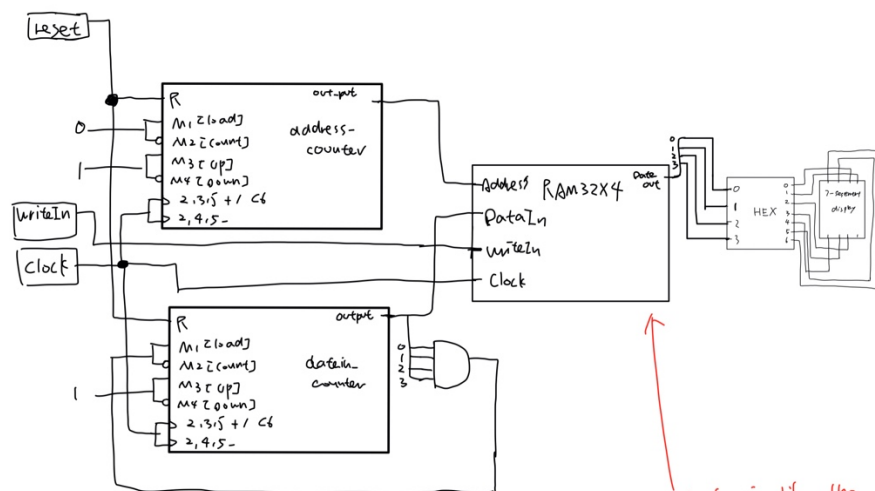
1. Create a 32 * 4 RAM module in Logisim.



2. What happens if both signals are off when the clock goes high? What happens when both signals are on?

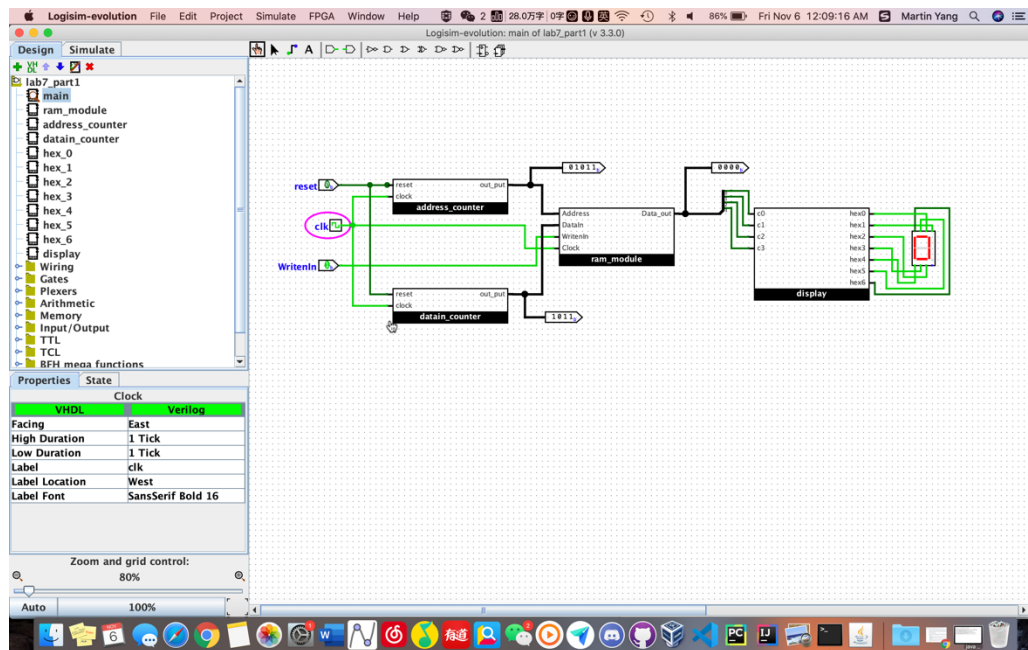
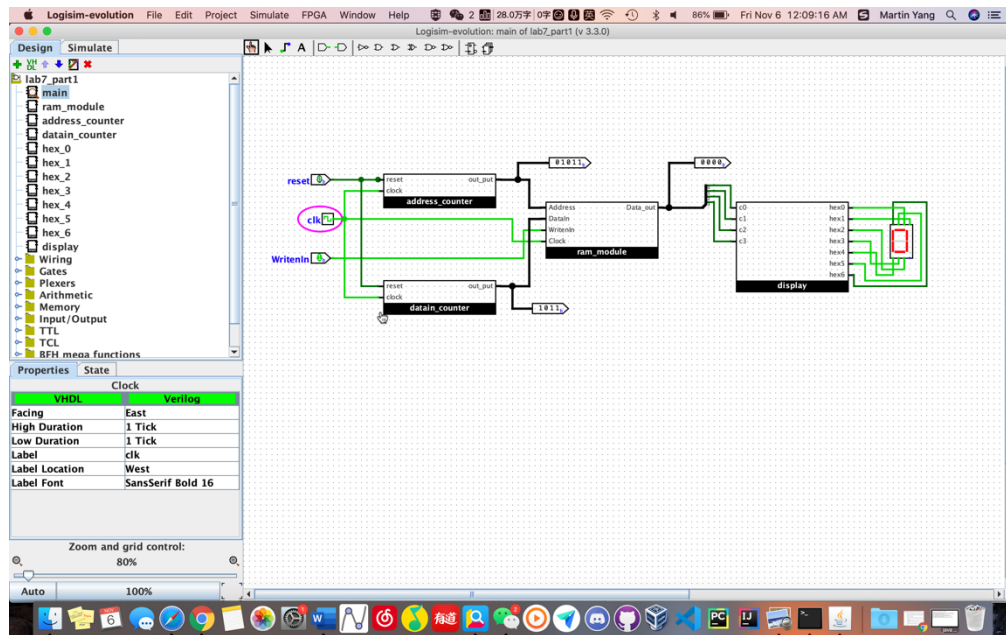
If both signals are off when the clock goes high, and then there is nothing will happen. In another case, if both signals are on when the clock goes high, then the DataIn will be written into RAM at the correct address and the output will be displayed as well.

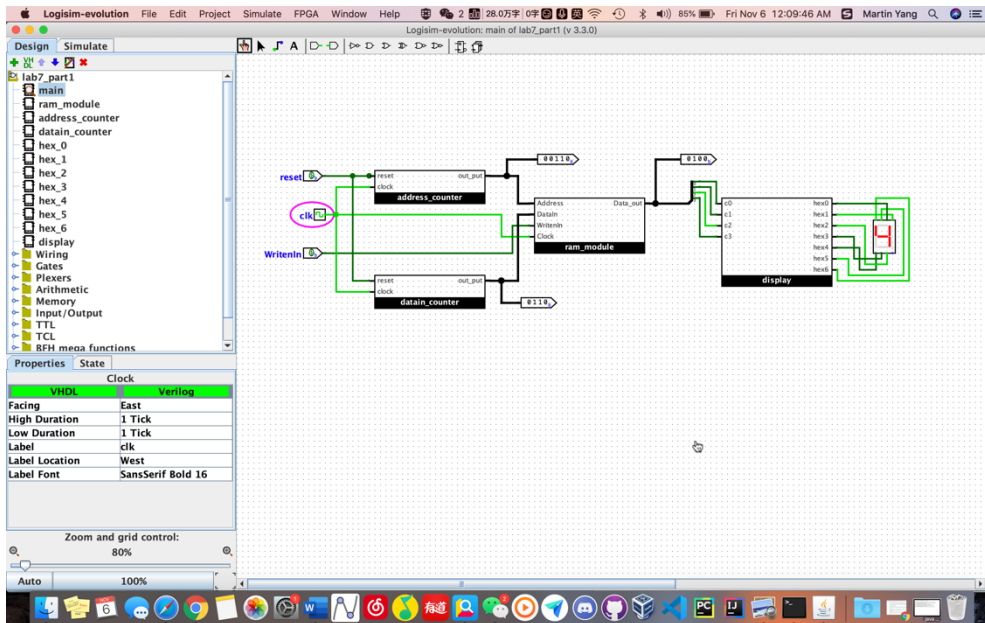
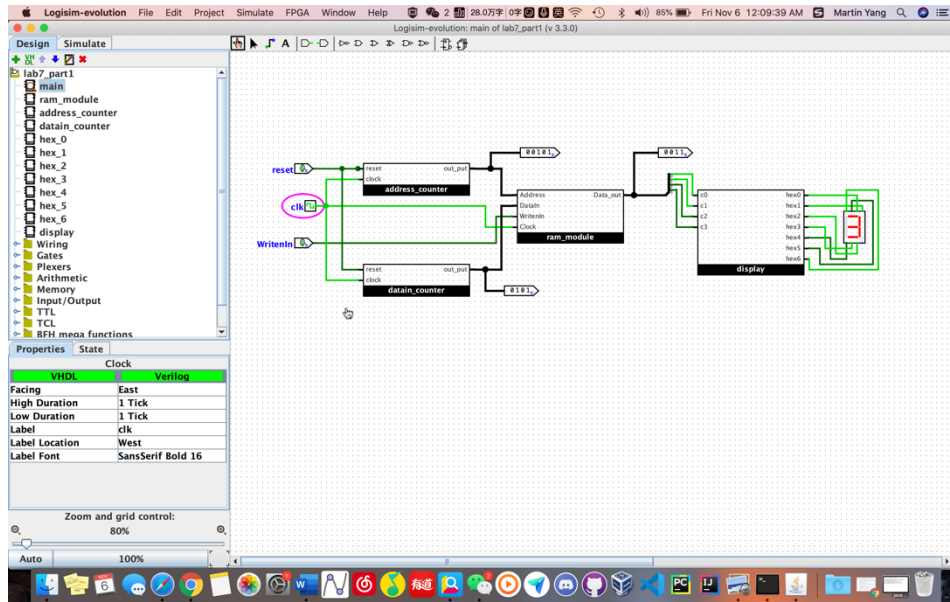
3. Draw a schematic.



we just simplify the whole design in here, since it is so complicated to draw by hand, please, understand!

4. Test the circuit.





Part2:

1. What happens if you don't turn Enable off before updating X and Y?

Some extra pixel will be drawn on the RGB board.

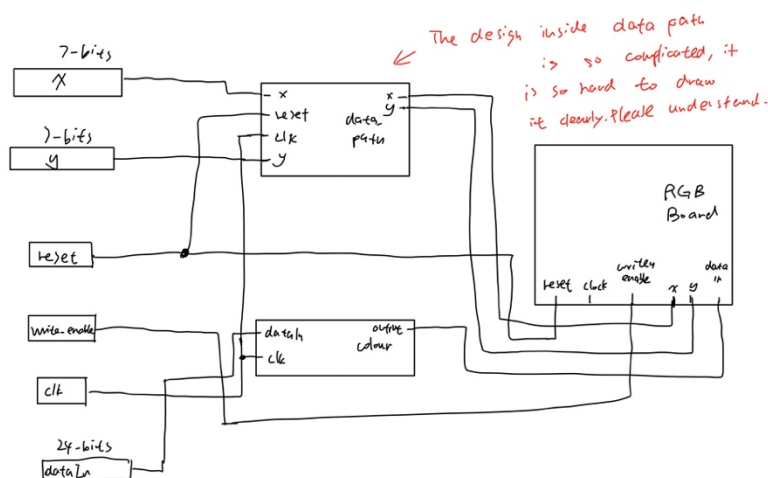
2. What happens if you turn Enable off before 256 clock cycles have passed?

The square you want to draw will not be complete, which means the rest of pixels will not be drawn on your RGB board.

3. What happens if you turn Reset on while Enable is on?

All pixels are you have drawn will be erased

4. Draw the schematic.



All other parts will be demonstrated in meeting. The circuit is like the blow.

