Course: CSC258F

Professor: Steve Engels

Experimenter: Yuhao Yang

Student ID: 1005808057

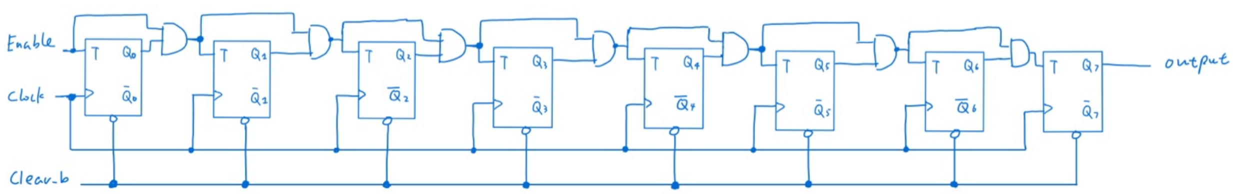
Lab5

Pre-Lab Report

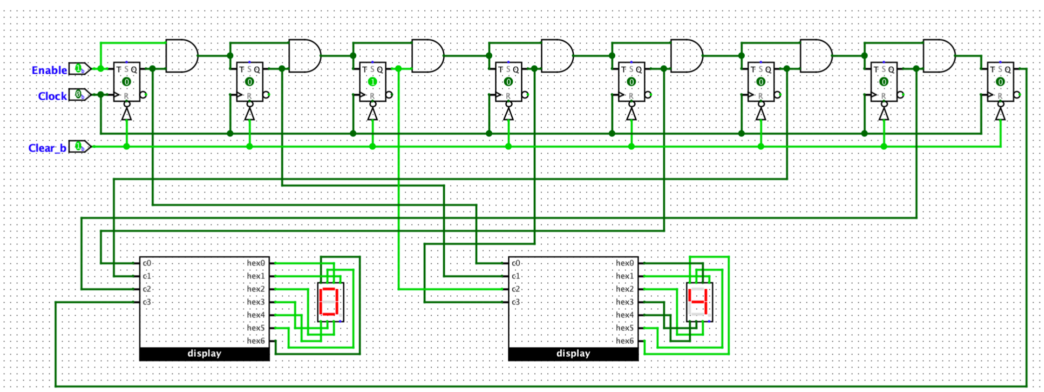
Part1:

1 & 2. Draw the schematic for an-8-bit counter.

8 - bit counter

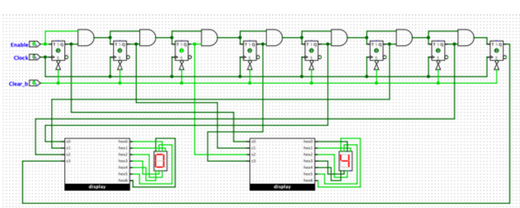


3 & 4. Build the circuit on Logisim.

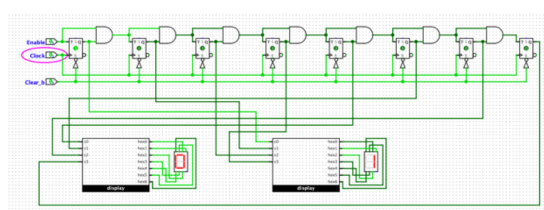


5. Show some poke results.

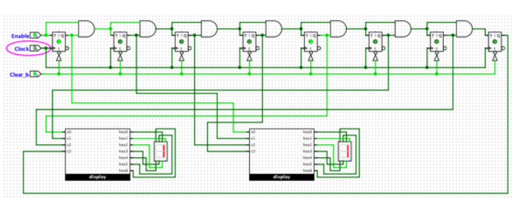
Poke show 01:



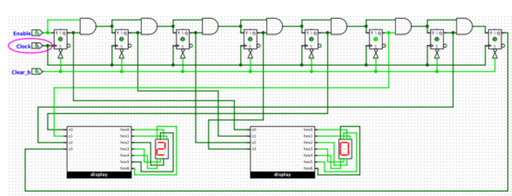
Poke show 04:



Poke show 11:



Poke show 20:



Part2:

1. Why the maximum for the example is not necessary?

Because we have a and gate in the example, when the counter's value reaches 1111(15), then the and gate, M1 and M2 will be activated and then counter will restore to zero. Therefore, we do not need to care about the maximum, since the value range of this counter is from zero to fifteen.

2. How to adjust the circuit if you want to build a 4-bit counter to counter from 0 – 9?

We can just simply add a not gate(negate) for the middle two inputs of the and gate then when the counter reaches 1001(9) then the counter will restore to one since the and gate, M1 and M2 are activated.

3. In Properties there is a setting called Action On Overflow. Explain how each value for this setting responds to overflow by experimenting with this setting and describing the results.

Wrap around: When the counter reaches maximum 1111, then the next value will be zero, which means the counter will restore to zero after that.

Stay at value: When the counter reaches maximum 1111, then the counter's value will remain at the maximum, which means the counter will remain at 1111 after that.

Counite counting: When the counter reaches maximum 1111, the counter continues incrementing, keeping the number of bits as

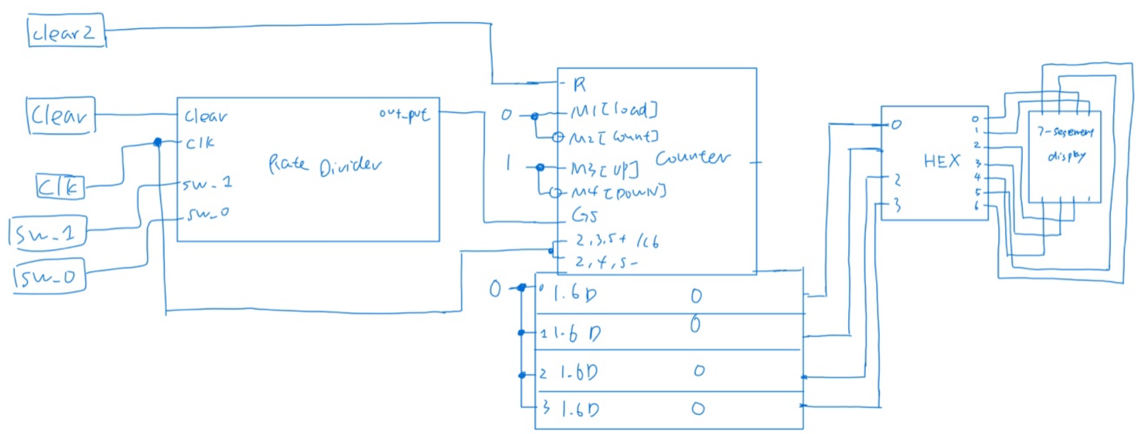
provided by the Data Bits attribute, so that the counter will show 0000, since 1111 is the maximum for that counter.

Load next value: When the counter reaches maximum 1111, The next value is loaded from the D input, which means the counter will go to 0000 by we set.

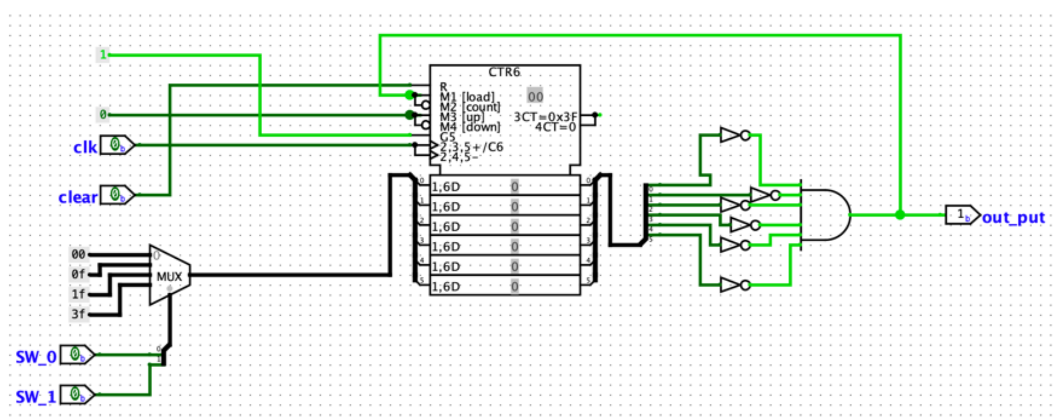
4. Calculate how large a counter would be required to count 50 million clock cycle?

The counter needs log2 50 Million = 26 bits.

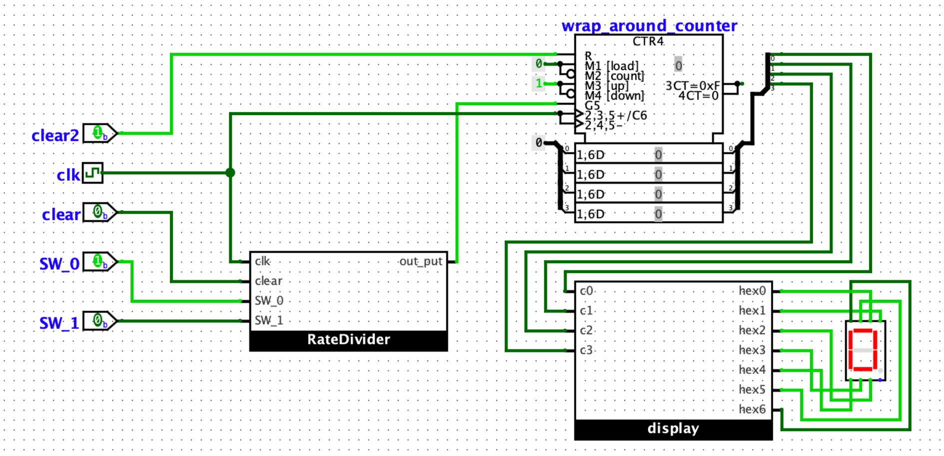
1. Draw the schematic.



The graph of the rate divider.

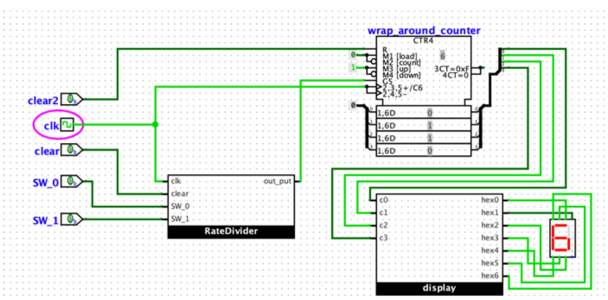


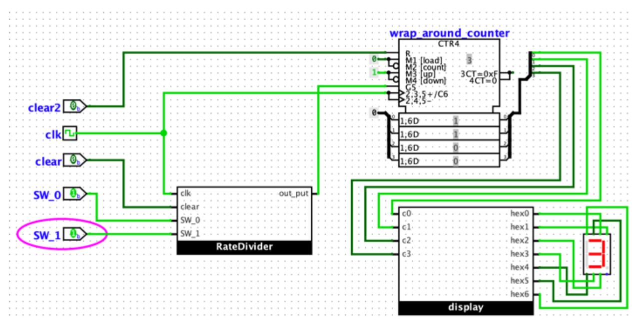
2. Build the circuit on Logisim

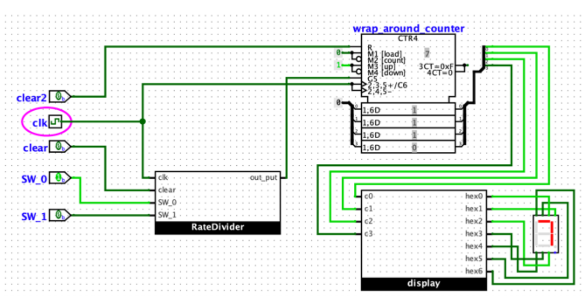


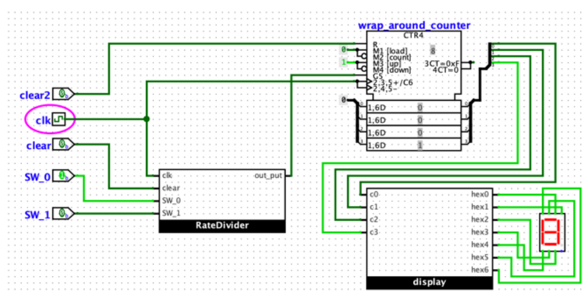
3. Simulate the circuit.

Some poke results.









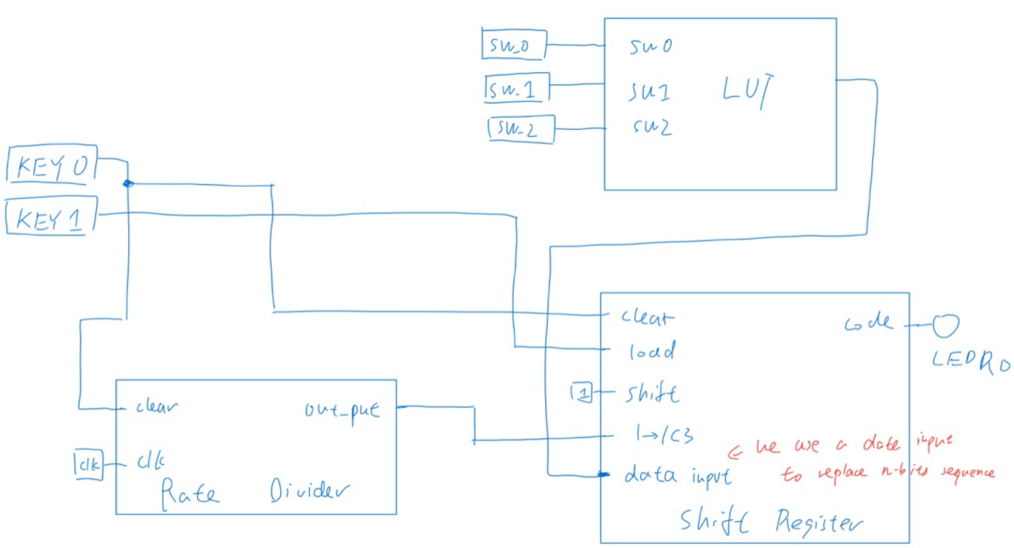
Part3:

Morse Pattern Representation Table:

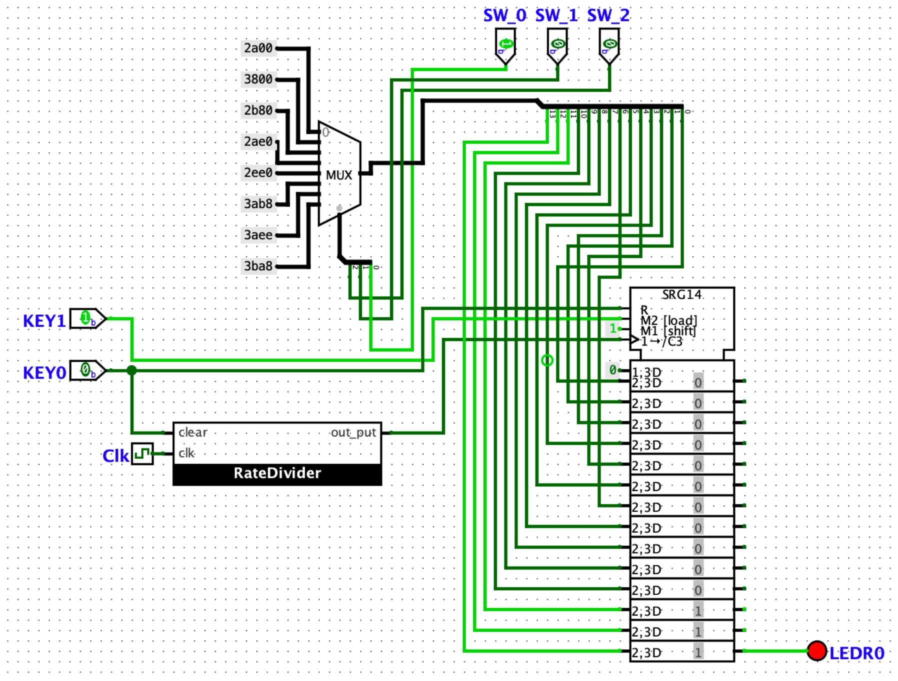
Letter	Morse Code	Pattern Representation (sequen length is 14 bits)
S	• • •	10101000000000
T	—	11100000000000
U	• • —	1010111000000
V	• • • —	10101011100000
W	• — —	10111011100000
X	— • • —	11101010111000
Y	— • — —	11101011101110
Z	— — • •	11101110101000

The length of binary representation needs 14 bits, since Y (- - · -) takes 13 bits which means binary representation needs at least 13 bits to work, and I choose 14 bits.

2. Draw the schematic.



3. Design circuit in Logisim.



4. Since I did not create a single module for LUT, I used poke method to check whether all data in my LUT is correct, and I poke SW0 – SW2 from 000 to 111 and all outputs are correct.