Course: CSC258F

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Lab1

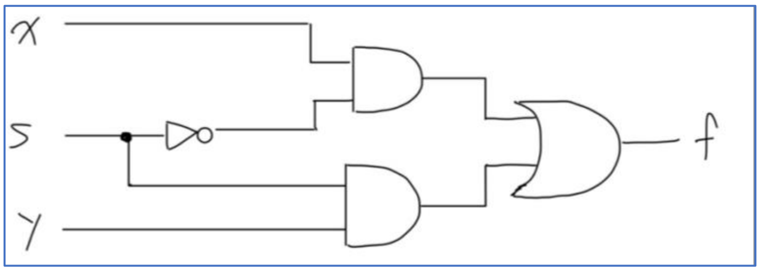
Pre-Lab Report

Part1:

Restate question:

There is a device called multiplexer that puts multiple inputs and get one output value out. The logical expression f = xs’ + ys (s’ means inverted s or not s’) is a 2-to-1 multiplexer, which means when s equals 1 then the output will be y, conversely when f is o, then the output will be x. Show the diagram by using just AND, OR and NOT gates and truth table of this logical expression f = xs’ + ys.

1. The diagram:



2. The truth table:

s	s'	x	y	f
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1

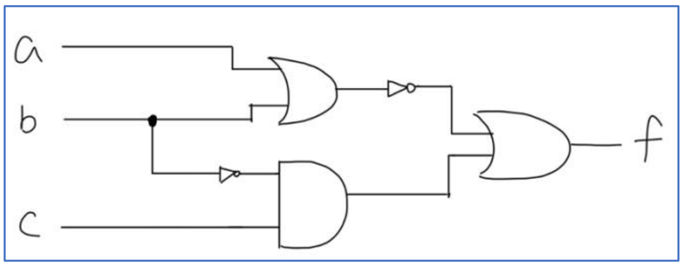
Illusion:

The diagram and truth table both show that when s = 0, as long as x = 1then the output will be 1. Instead, when s =1, as long as y = 1 then the output will be 1. It perfectly satisfies the question’s requirements.

Part2:

Restate question: Show the diagram of the logical expression f = (a + b)’ + cb’ by using only AND, OR and NOT gates, then write down the truth table of the expression. Is there any cheaper implementation for this design, if yes, show the solution how to simplify by rewriting the Boolean function.

1. the diagram:



2. The truth table:

a	b	c	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Illustration: This question has three inputs which are a, b and c, the a, b and c will get one output f after a series of logical implementation. The diagram and truth table perfectly show how logical expression f = (a + b)’ + cb’ works. We also can invert (a + b)’ to a’b’ by De Morgan’s Law to do further simplification for this this expression.

3. Yes, it has chapter implementation for this design, we can just use De Morgan's law to simplify this Boolean expression like shown below:

$$f = (a + b)' + cb'$$

$$= a'b' + cb' \text{ --- De Morgan's Law}$$

$$= b' (a' + c) \text{ --- Distribution Law}$$

We used five chips in the original Boolean function but now we only used 4 chips.