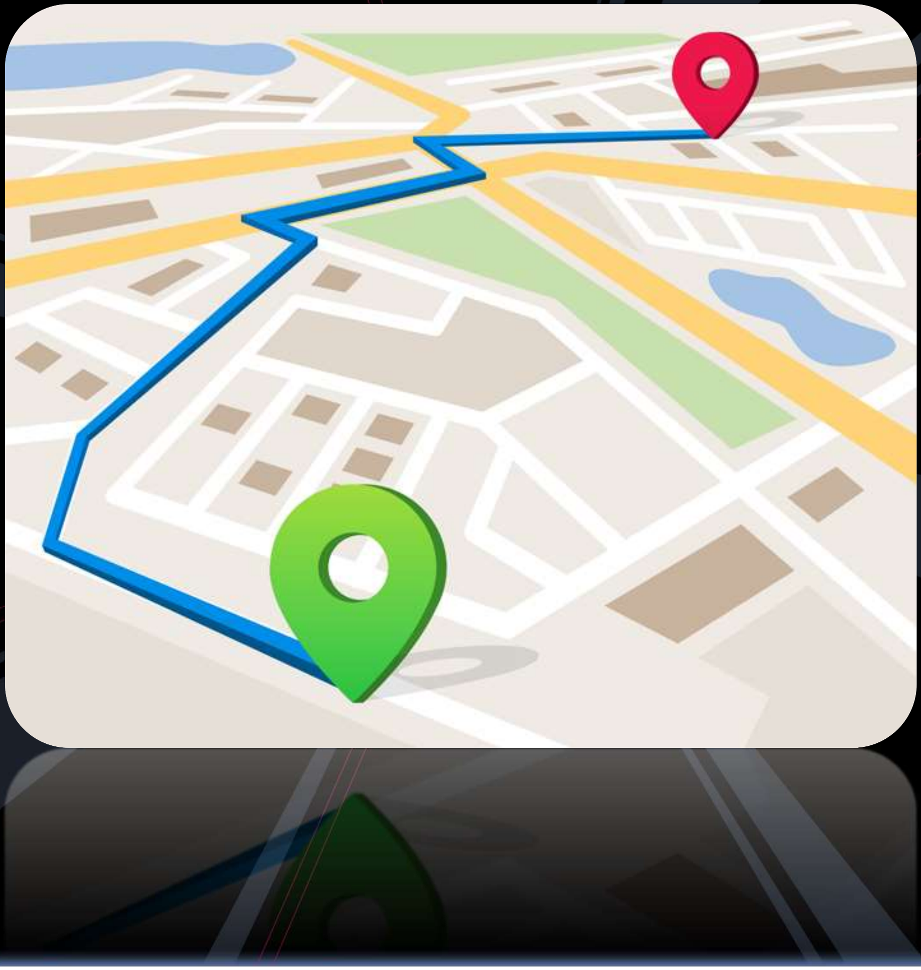
Lab 1 – Preparation

Today's Tutorial

- Learning objectives for Lab 1
- Lab 1 parts
  - Warm-up exercise
  - What to hand in
- Intro to Logisim

Learning objectives



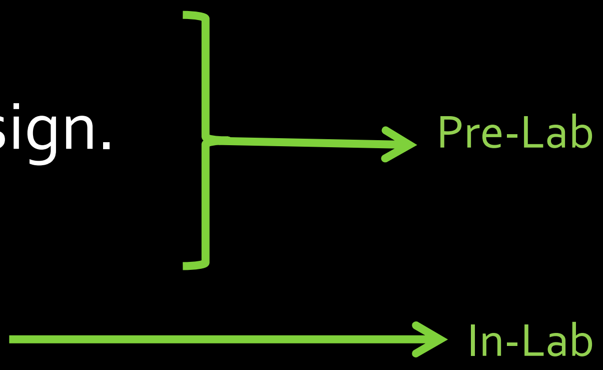
Lab 1 Learning Objectives

- What are the labs about?
  - Creating demo-worthy designs.

- What is Lab 1 about?
  - Learn how to build logic circuits by using logic gates.
  - Produce truth tables for a given design (starting either from a given logic function or from a description of the design’s behaviour).
  - Demonstrate familiarity with the graphic tool Logisim.

Approach to Lab 1

- Experience is the best teacher.
  - Prepare a design.
  - Implement your design.
  - Debug the circuit.
  - Demo your design

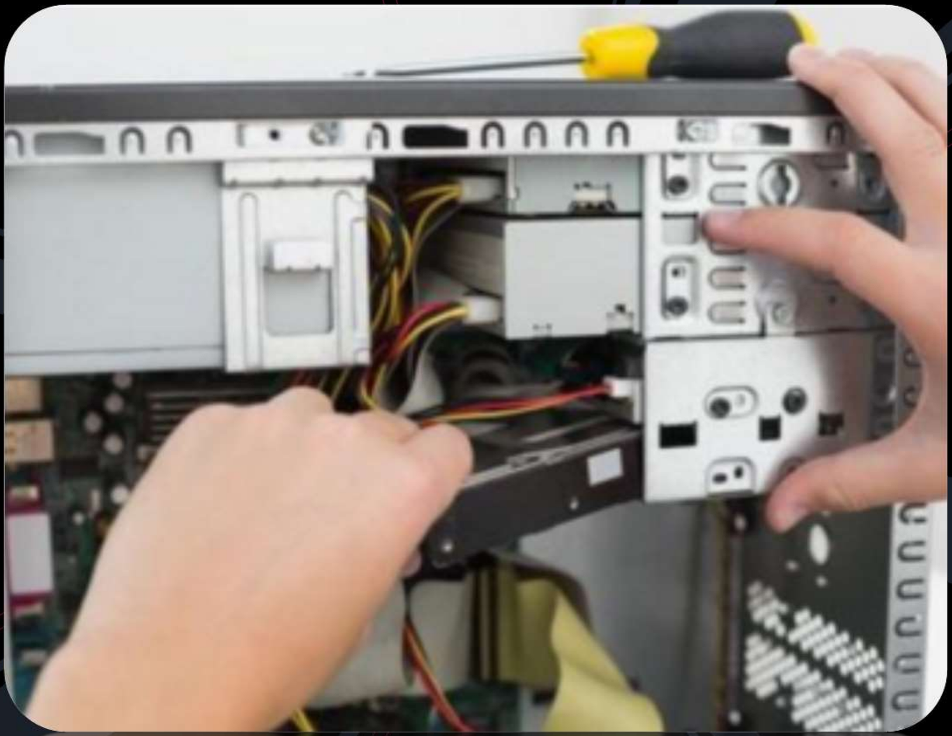


Pre-Lab

In-Lab

- Try to think of your prelabs as "an assignment due before the beginning of the lab".

Lab Breakdown

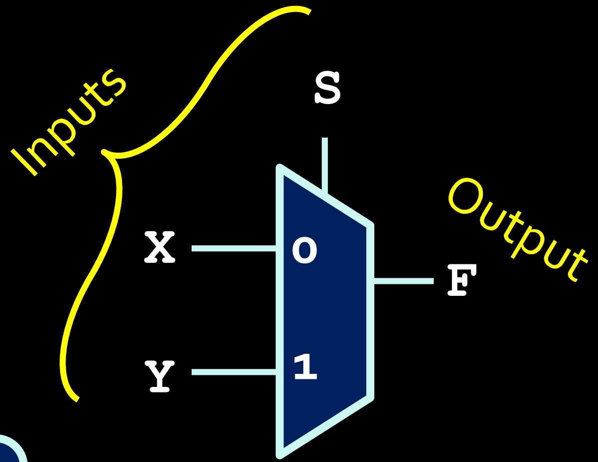


Lab 1 breakdown

- Mark breakdown:

Pre-lab:	2 marks
Part I:	2 marks
Part II:	2 marks
Part III:	2 marks

- Part I:
  - Design circuit for multiplexer:



$$F = X\overline{S} + YS$$

Lab 1 breakdown

- Part I (cont'd):
  - Note that the following are all different ways of expressing the same thing:
    - $F = X\overline{S} + YS$
    - $F = X*S' + Y*S$
    - F = (X and (not S)) or (Y and S)
  - Need to represent this logical expression in gates.
  - Need to show the truth table for the three inputs X, Y & S and the output F.
- Part I doesn't involve Logisim yet ☺

Lab 1 breakdown

- Part II:
  - Given the function:

$$f = (a+b)' + cb'$$

  - How would you implement this in gates?
  - What is the minimal number of gates you need?
- Part III:
  - Implement these circuits in Logisim.
  - Test your designs (using Poke tool and test files)

Warm Up Example

- Design a circuit that implements the following logic function, using only 2-input AND and 2-input OR gates.

```
f = a*b + (c + b)
```

- Write down the truth table for this design.
  - Note: This expression is common shorthand for:

```
f = a AND b OR (c OR b)
```

Warm Up Example cont’d

- Is there a cheaper implementation (i.e., with fewer gates)?
  - f = a*b + (c + b)

What to hand in

Prelab vs Lab Demo

- Prelab exercises are due before 6pm on lab days.
  - Written/hand-drawn elements in PDF files.
  - Logisim circuits as `*.circ` files.
  - Logisim tests as `*.txt` files.
- TAs will definitely ask to look at your Logisim designs, so be ready to share your screen with them.
  - Also be ready to share the hand-written elements in case a question arises about your design process.

Pre-lab reports

- The hand-written report should include the following:
  - Lab number and title
  - Student info (last name, first name, student #)
  - Exercise parts
    - Each in its own clearly-labeled section.
    - Restate the question (summarized).
    - Provide the calculations (if applicable).
    - Illustrate the solution (including pin labels).
  - PLEASE BE NEAT.
- The Logisim files should be named to reflect the lab number and part number.
  - e.g. `lab1_part2.circ`

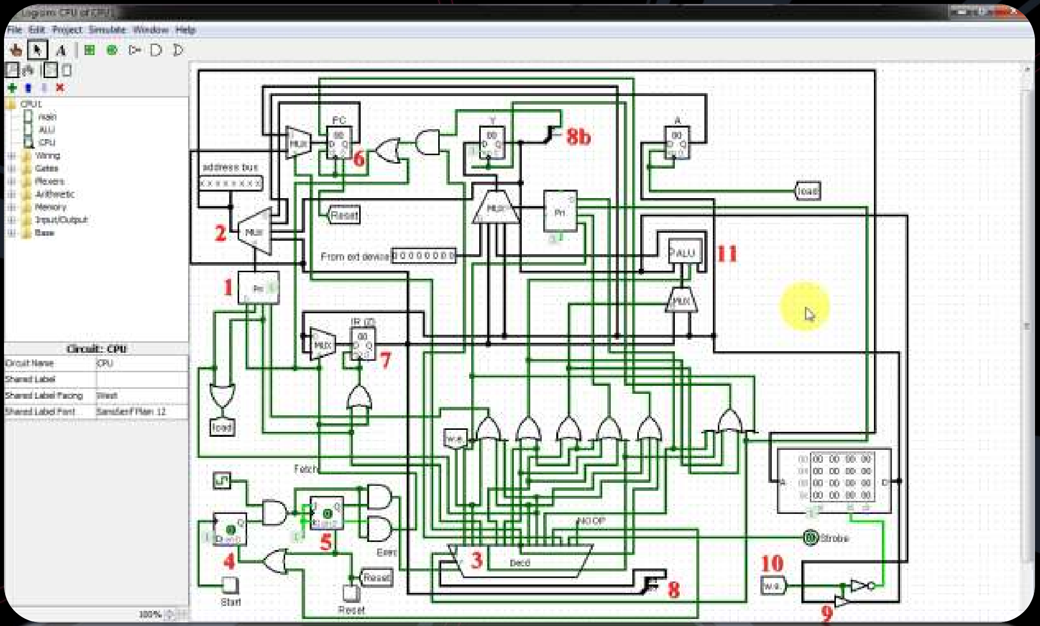
Things to note

- This will be the easiest lab you do in the course.

- Whenever possible, use the tools and submit a printed pre-lab report.

- Try to come up with the smallest circuits possible.
  - How do you reduce a complex circuit?
  - For now, think back to boolean algebra axioms!
  - Simple reasoning helps as well ☺

Intro to Logisim

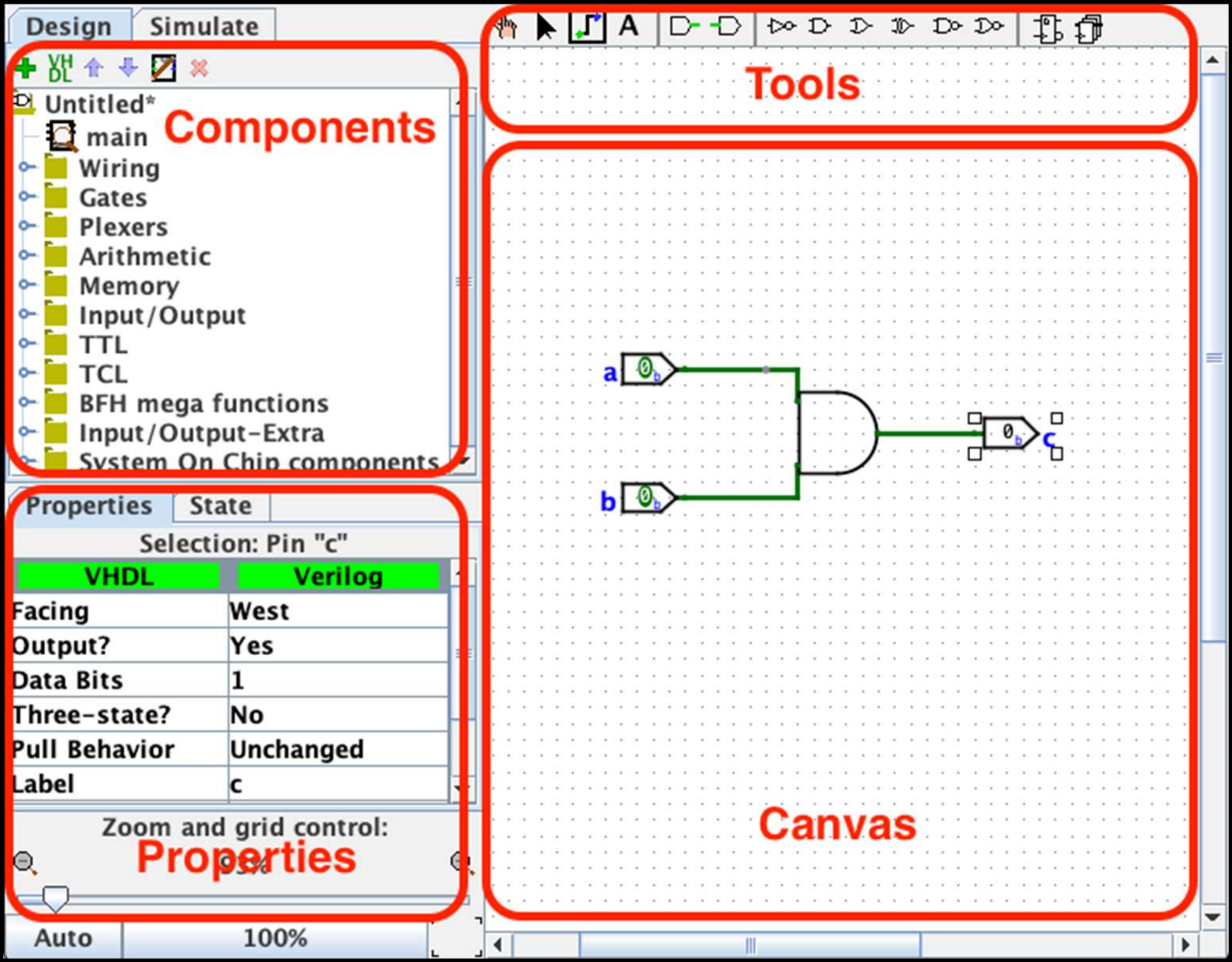


Circuit: CPU	
Circuit Name	CPU
Shared Label	
Shared Label Facing	West
Shared Label Font	SansSerif Plain 12

Logisim installation

- Logisim is a powerful logic circuit simulation environment.
  - In this course, we will be using version 3.3.0
    - https://github.com/reds-heig/logisim-evolution/releases/tag/v3.3.0
    - Just the `jar` file is needed.
- Note:
  - Make sure to use Logisim-Evolution downloaded at the above link. Do NOT use the original Logisim or any other variations or versions of it.
  - You will need Java 13 installed to launch this.

Logisim walkthrough



Components

Tools

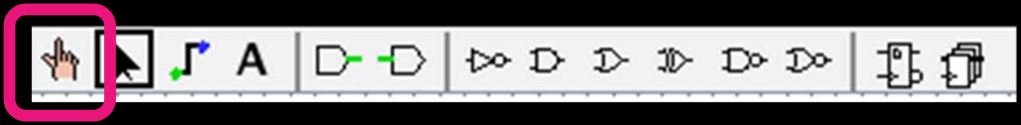
Canvas

Properties

Selection: Pin "c"

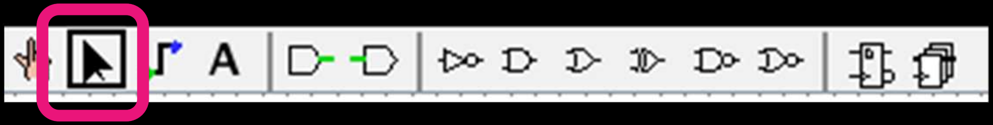
VHDL	Verilog
Facing	West
Output?	Yes
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	c

Tools/Views



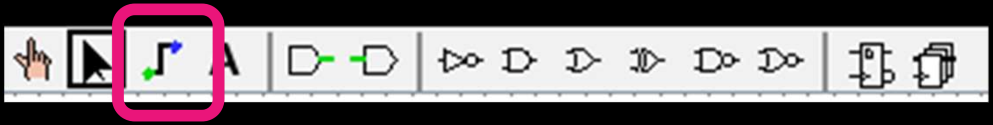
Poke: Click on wires to inspect their state, click on most components to change their state.

Tools/Views



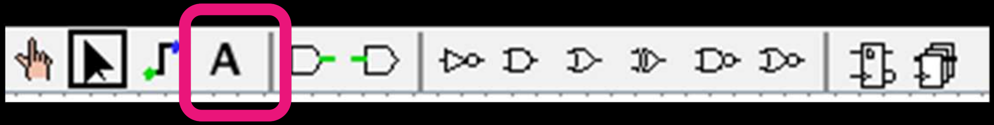
Select: Selects and moves things in the canvas, and manipulates wires/buses. Click and drag from inputs/outputs to create wires/buses.

Tools/Views



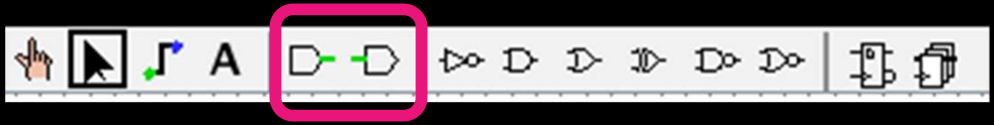
Wire: Creates wires on the canvas.

Tools/Views



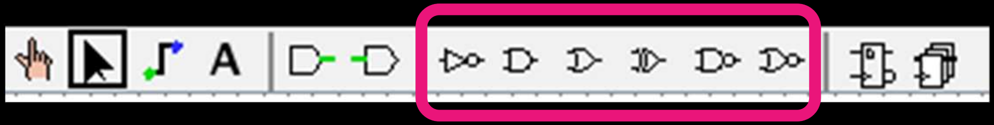
Text: Add text on the Canvas.

Tools/Views



Default Input/Output: default type of input and output for the circuits. You will be using them a lot throughout the course.

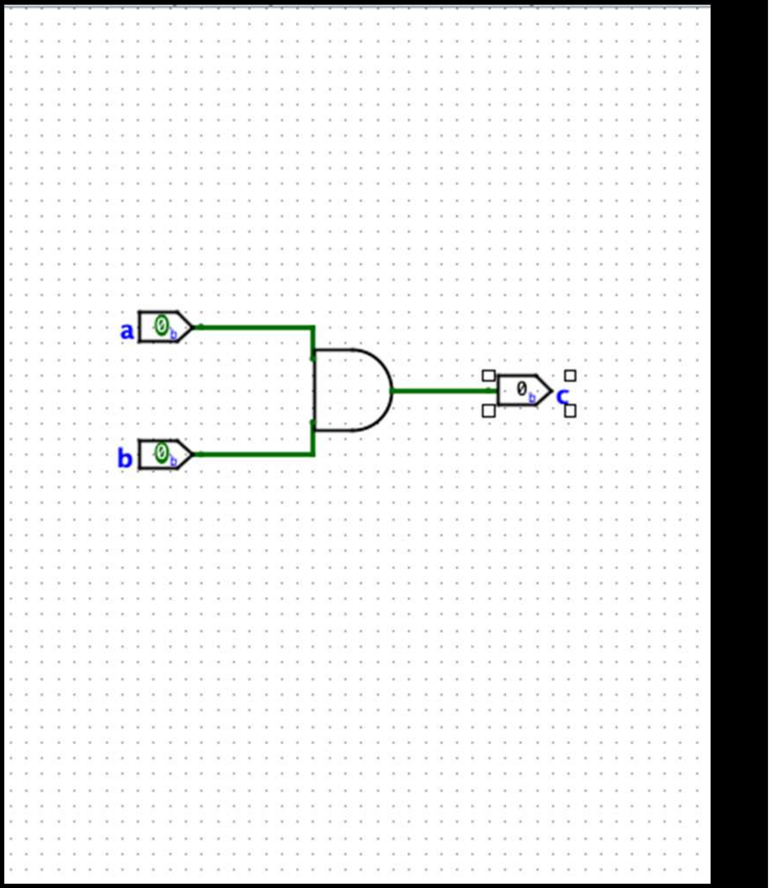
Tools/Views



Logic gates: some commonly used logic gates that you can click and drop on the canvas to build your circuits.

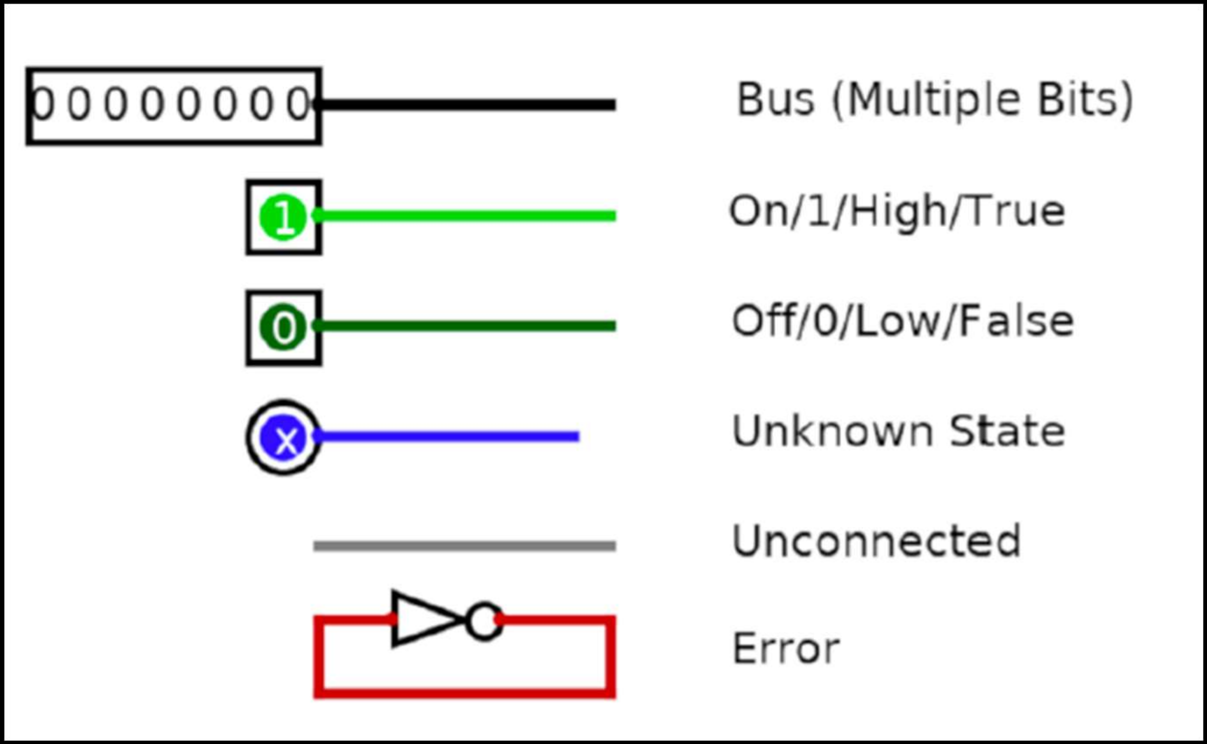
Canvas

- Canvas is where you will be building your circuits by dropping components on the canvas and then connect them with wires.



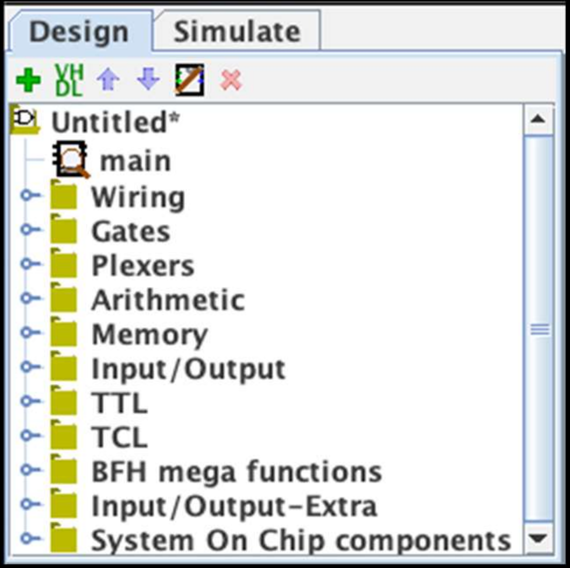
Wires

- Wires and buses can have many states. You can inspect the state of a wire/bus using **poke** in the toolbar.



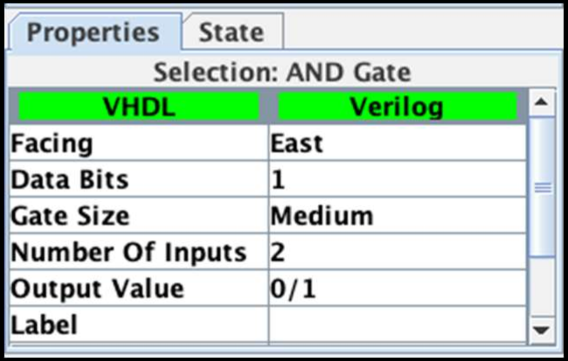
Components

- This contains all the circuits in this le as well as all the built-in components.
- Double-click on each circuit to view it. To place a component from this list, select it, and then click somewhere in the canvas.
- You can add/delete a circuit using the green + sign and the red x sign on the top.



Properties

- If you click on a component on the canvas, you would be able to view and edit its properties.
- For example, this is the properties for an AND gate. You can change the number of input bits and number of inputs here. This will be useful in the future.

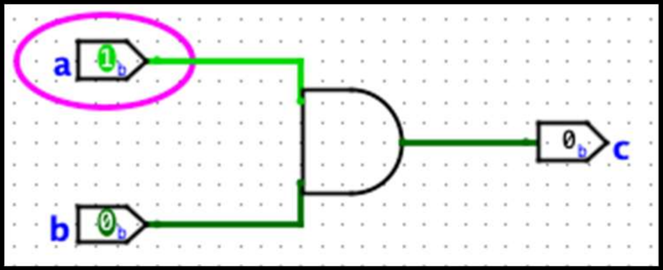


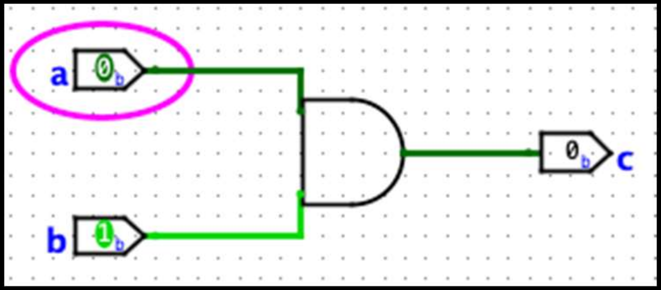
Selection: AND Gate

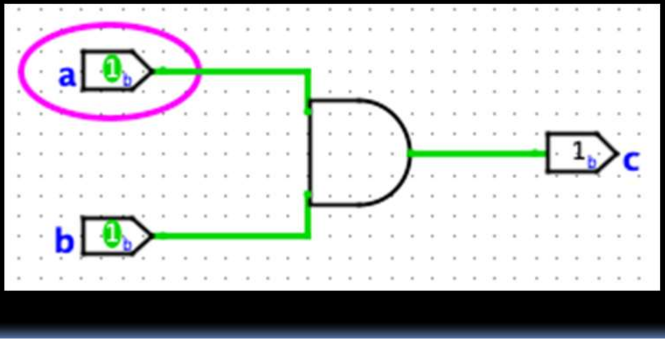
VHDL	Verilog
Facing	East
Data Bits	1
Gate Size	Medium
Number Of Inputs	2
Output Value	0/1
Label	

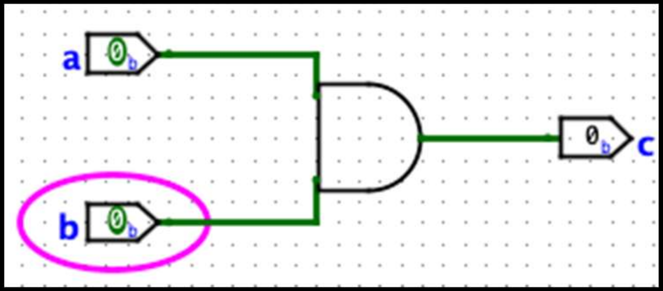
Testing in Logisim

- The easiest and most visual way of testing is using the Poke in the tool bar and click on the components to change the state. This will be very useful throughout the course so make sure you try this out.









Testing in Logisim

- Another way is through test vector files. (details can be found in the lab handout)
- Steps involved:
  1. list the truth table for your circuit, the values for the inputs and the expected values for the outputs
  2. Logisim will be able to run the tests according to your truth table to test the functionality of your circuit.