

Course: CSC258F

Professor: Steve Engels

Experimenter: Yuhao Yang

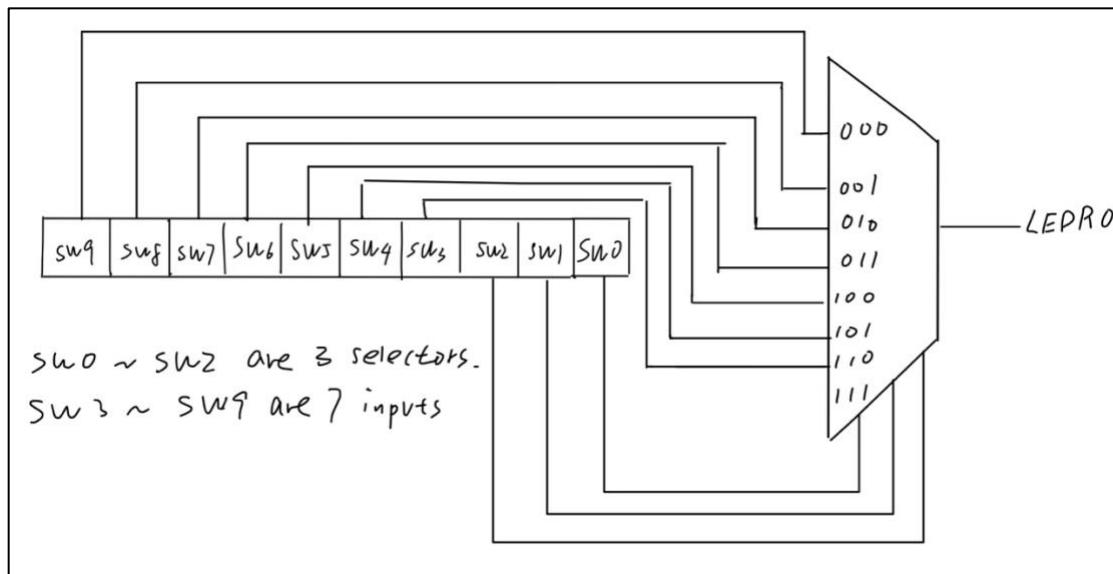
Student ID: 1005808057

Lab3

Pre-Lab Report

Part1:

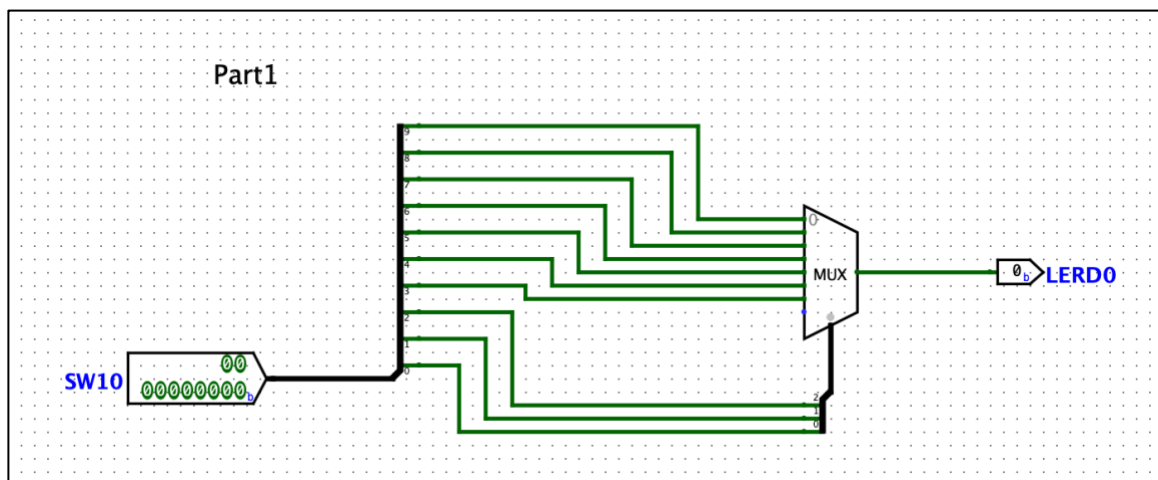
1. Draw the 7-to-1 multiplexer and label properly of all inputs, outputs and wires between modules.



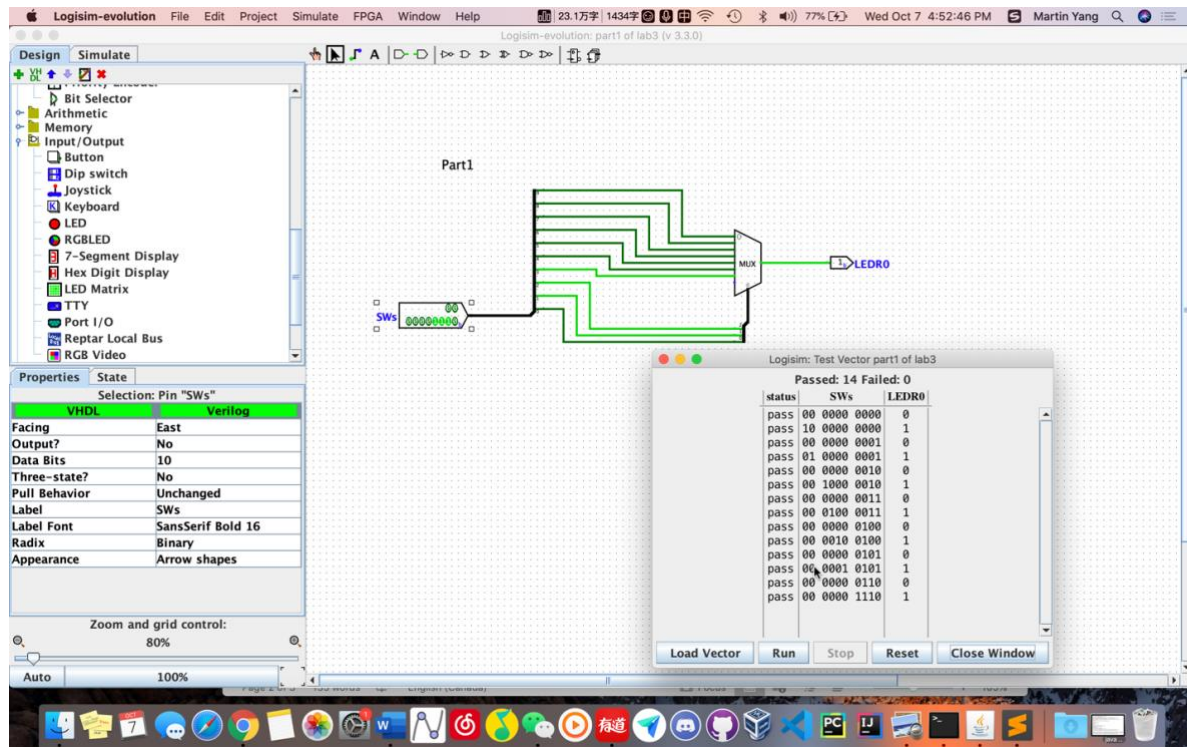
1_b) How big does the multiplexer bit input need to be able to provide all the inputs to the 7-to-1 multiplexer?

I think the multiplexer needs to have 10 bits to be able to provide all the inputs to the 7-to-1 multiplexer, since there are 3 bits selector from SW0 to SW2 and 7 bits inputs from SW3 to SW9. (Although selector on Logisim only has one port but we consider the port contains 3 bits selector.)

2. Building the circuit in Logisim by using a 7-to-1 multiplexer and the splitter.

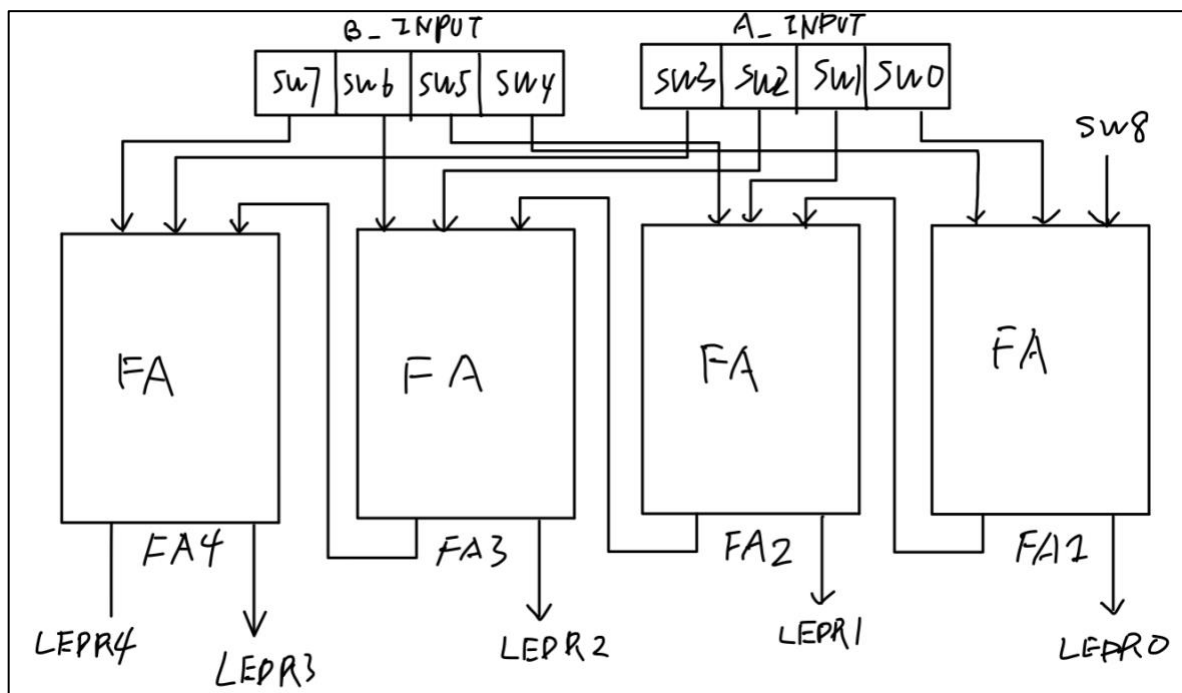


3. Test the by using proper test vector and show the screenshot.



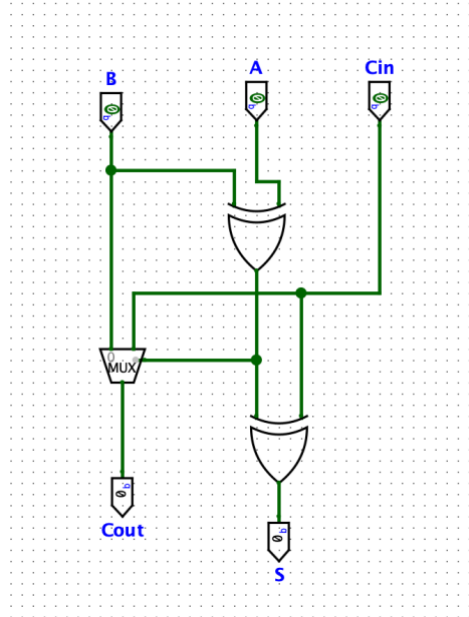
Part2:

1. Draw the schematic of the structure with all wires, inputs and outputs labeled.

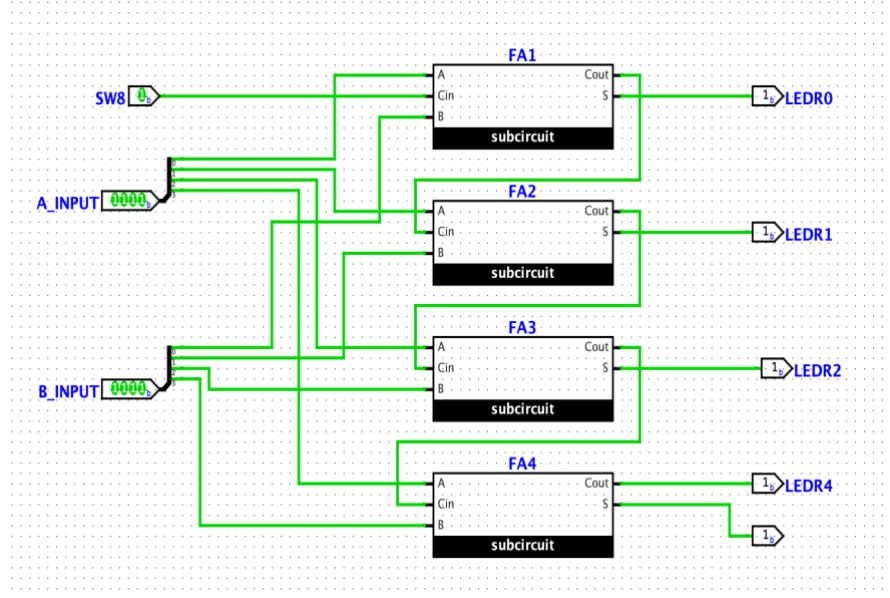


2. Build the module for the full adder in Logisim by using the heretical strategy.

This is circuit of each adder.



This is the circuit of four adder together.



3. Using test vector to show that the circuit is working correctly.

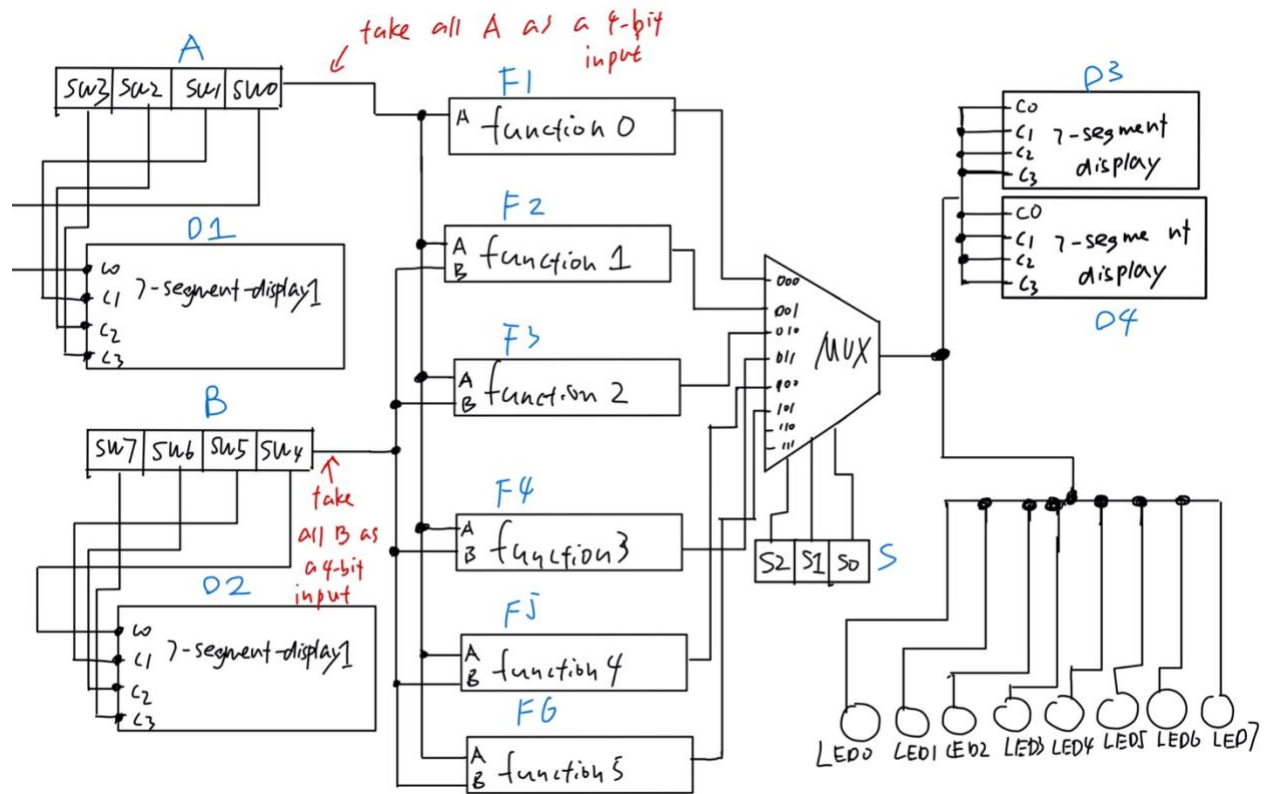
The screenshot shows the Logisim-Evolution interface. The main window displays the circuit diagram of four full adders. The left sidebar shows the 'Design' and 'Simulate' tabs. The 'Properties' panel on the left shows the circuit name 'main' and the Verilog language selected. The 'Test Vector' window is open, showing a table of test cases and their results.

status	A_INPUT	B_INPUT	SW8	LEDR0	LEDR1	LEDR2	LEDR3	LEDR4
pass	0000	0000	0	0	0	0	0	0
pass	1100	0011	0	1	1	1	1	0
pass	0001	0001	0	0	1	0	0	0
pass	0010	0010	0	0	0	1	0	0
pass	0100	0100	0	0	0	0	1	0
pass	1000	1000	0	0	0	0	0	1
pass	1111	1111	0	0	1	1	1	1
pass	0000	0000	1	1	0	0	0	0
pass	0001	0001	1	1	1	0	0	0
pass	1111	1111	1	1	1	1	1	1

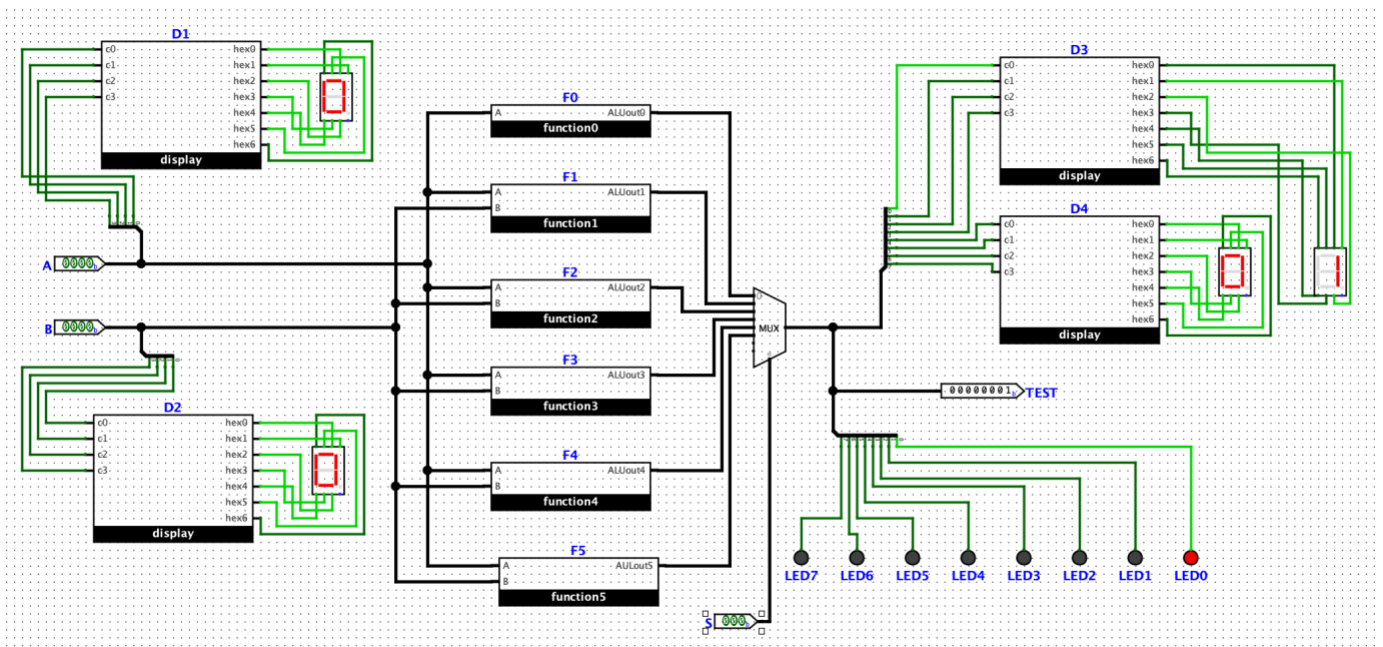
The 'Test Vector' window also includes buttons for 'Load Vector', 'Run', 'Stop', 'Reset', and 'Close Window'.

Part3:

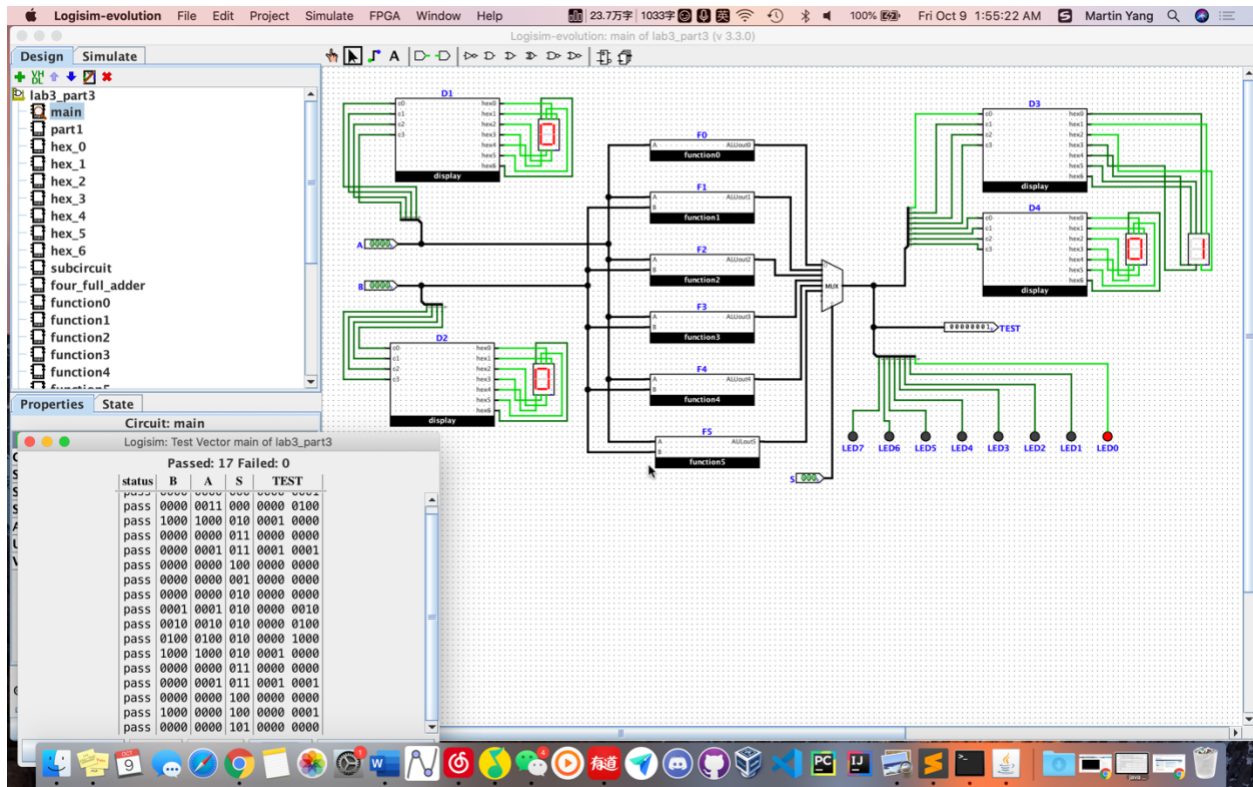
1. Draw the schematic of the structure with all wires, inputs and outputs labeled.



2. Build the Logisim module for the ALU including all high-level inputs and outputs



3. Using test vector to show that the circuit is working correctly.



Because there are too many situations for the circuit, I just randomly wrote down some of test vectors, but the test vectors include all six-functions in circuit.