Course: CSC258F

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Lab4

Pre-Lab Report

Part1:

1. Build the D latch and master slave flip-flop in Logisim in different modules.

***D latch circuit***

Diagram, schematic

Description automatically generated

***master slave flip-flop***

Diagram

Description automatically generated

2. Show the circuit is correct by using Poke.

***Showed on Logisim.***

3. For the D latch and the flip flop, are there any input combinations of Clk and D that should NOT be the first you test?

***From my perspective, all combinations for the D latch should not be the first test, because no matter Clk takes value of zero of one for the first test, one of the D latches will have zero as input of Clk since invertor. As we know, when Clk is zero, then the D latch will keep the previous state, but there is no previous state for both D latches when I first test, then it will raise an error. Same to flip flop, one of D latch will have zero of Clk, but there is no previous state for that D latch, so the flip flop will raise an error for all combinations of Clk and D.***

Part2:

1. Build the circuit in Logisim.

Diagram

Description automatically generated

2. Answer the question

2.

a) What would happen if we remove register in the circuit?

***By observing the circuit, we know that if we remove the register, then the function 1 to function 7 will not have input signal B, and it will cause errors if we select function 1 to 7 in MUX.***

b) How many bits we need to store the result if we multiple two n-bit binary number?

***If we multiple two n-bit binary number, then we need 2n bits to store the result.***

3. Answer the questions below.

***a) Let data to be zero than we set clk to be one, then set clk to be zero and change s to be 001 from 000 which means we changed to the next function and set clk to be one again, we just need to follow this process and we can get a correct and net sequence.***

***Table

Description automatically generated***

***b) Use test vector to show new operations are correct.***

***Function5***

***A picture containing graphical user interface

Description automatically generated***

***A picture containing diagram

Description automatically generatedFunction6***

***Function7***

A picture containing graphical user interface

Description automatically generated

Part3:

1. What is the behaviour of the 8-bit shift register shown in Figure 5 when Load n = 1 and ShiftRight = 0?

***When Load n = 1 and ShiftRight = 0, the output will remain the previous state because load\_val cannot pass the second MUX in ShiftBit.***

A picture containing diagram

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2. Draw the schematic

4. Show the circuit in Logisim.Diagram

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