Design of Low Inductance Busbar for 500 kVA Three-Level ANPC Converter

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***Abstract*— The adoption of SiC devices in high power applications enables higher switching speed, which requires lower circuit parasitic inductance to reduce the voltage overshoot. This paper presents the design of a busbar for a 500 kVA three-level active neutral point clamped (ANPC) converter. The layout of the busbar is discussed in detail based on the analysis of the multiple commutation loops, magnetic canceling effect, and DC-link capacitor placement. The loop inductance of the busbar is verified with simulation, impedance measurements, and converter experiments. The results match with each other, and the inductances of small and large loop are 6.5 nH and 17.5 nH respectively, which is significantly lower than the busbars of NPC type converters in other references.**

I. Introduction

The three-level active neutral point clamped (3L-ANPC) converter as shown in Fig. 1 is widely implemented in high power medium voltage applications because of its lower device voltage rating requirement, higher efficiency, lower EMI noise generation, higher power quality, and flexible power flow control capability [1], [2].

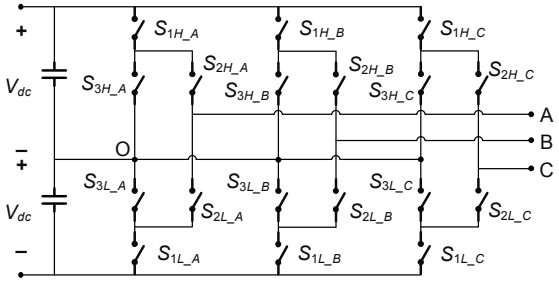


Fig. 1. Topology of 3L-ANPC converter.

In high power converters, busbars are the main connectors between power modules, capacitors and filters, and they not only bear high voltage and deliver high current at steady state, but also transmit high frequency voltage and current during switching transitions. The resonance between the loop inductance of the busbar and the parasitic capacitance of power semiconductor devices can result in voltage and current overshoot. A poor design of the busbar with high parasitic inductance produces higher harmonics, and the overshoot can damage the power devices. As shown in Fig. 2, the peak of the drain-source voltage during a switching transient is three times higher than its steady state value. This issue becomes even more severe and complicated in multi-level topologies since they have multiple commutation loops. In 3L-ANPC converters, two commutation loops exist during the switching transient [3]-[7].

Moreover, the introduction of silicon carbide (SiC) MOSFETs enables higher switching speed compared to Si IGBTs, which helps reduce the switching loss and increase the switching frequency. However, parasitics show higher impact as the *dv*/*dt* and *di*/*dt* during a switching transition increase. Therefore, a proper design of the busbar with low loop inductance is essential for fully utilizing the switching capability of SiC power devices.

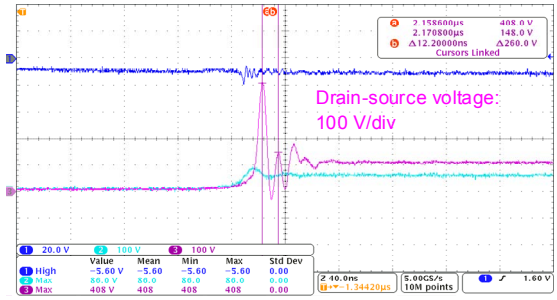


Fig. 2. Severe voltage overshoot caused by poor loop inductance.

Extensive work has been conducted to analyze and optimize busbar design [8]-[13]. However, most previous work focused on two-level converters and did not consider the multi-loop issue in multi-level converters. In [14]-[18],

busbars are designed specifically for three-level NPC type converters. However, the loop inductances in sub-1MW converters are normally higher than 100 nH, which still limits the switching speed of SiC MOSFETs due to introduced voltage overshoot. Thus, it is desirable to design a busbar with lower loop inductance for 3L-ANPC converter.

This paper presents the design of a busbar that considers the multi-loop influence, which can significantly reduce the parasitic inductances of the commutation loops in 3L-ANPC converter.

II. Evaluation of Commutation Loops and Parasitic Inductance

A. Commutation Loops in 3L-ANPC Converter

The equivalent circuit of a single phase in the 3L-ANPC converter is illustrated in Fig. 3. Different busbar parts, parasitic inductances, and commutation loops are highlighted. One example of the modulation scheme [3] is plotted in Fig. 4, and it is divided into four states during one line cycle as listed in Table I. S_{1H}, S_{3H}, S_{1L} and S_{3L} operate at high switching frequency while S_{2H} and S_{2L} operate at line switching frequency.

During the half line cycle with negative output voltage, the operation state changes between N and O$^-$, which means that S_{1L} and S_{3L} operates at high frequency while S_{2L} and S_{3H} keep in on state, and S_{2H} and S_{1H} are off.

As shown in Fig. 3, there are two commutation loops. One goes through S_{1L} and S_{3L}, and it is marked in pink color. This loop is similar to a conventional loop in two-level phase legs. The parasitic inductance resonates with the output capacitance of S_{1L} or S_{3L} depending on which one is the synchronous switch.

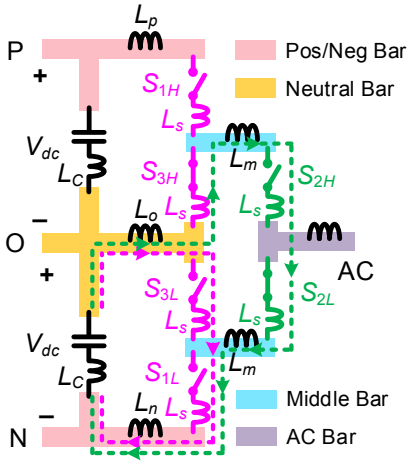


Fig. 3. Circuit of single phase 3L-ANPC converter considering parasitic inductance.

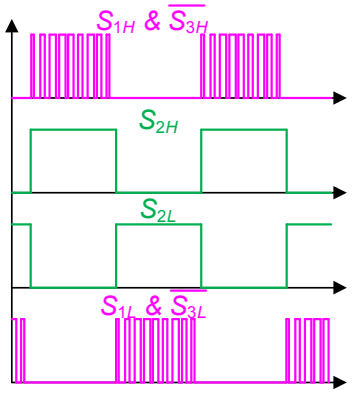


Fig. 4. Modulation scheme of single phase 3L-ANPC converter.

Table I. Operation states of single phase 3L-ANPC converter.

State	S_{1H}	S_{3H}	S_{2H}	S_{2L}	S_{3L}	S_{1L}
P	On	Off	On	Off	On	Off
O$^+$	Off	On	On	Off	On	Off
O$^-$	Off	On	Off	On	On	Off
N	Off	On	Off	On	Off	On

The other commutation loop is shown in green line. Since S_{2L} and S_{3H} are in on state, S_{2H} is equivalently paralleled with S_{3L}. As a result, when S_{3L} is commutating with S_{1L}, the drain-source voltage of S_{2H} follows the drain-source voltage of S_{3L} even though S_{2H} is a non-active switch during the half line cycle. The parasitic inductance resonates with the output capacitance of S_{2H}.

B. Parasitic Inductance Distribution

Assuming each busbar part is independent and is not coupled with other busbar parts, the total parasitic inductance of the two loops can be evaluated as follows.

For the pink commutation loop, it includes the decoupling capacitors, neutral busbar, negative busbar, and two power switches S_{1L} and S_{3L}. Thus, the total parasitic inductance L_1 of the pink loop is

$$L_1 = L_C + L_o + L_n + 2L_s \quad (1)$$

where L_C is the ESL of decoupling capacitors, L_o and L_n is the inductance of the neutral and negative busbars, L_s is the inductance of each power switch.

In terms of the green commutation loop, it consists of the decoupling capacitors, neutral busbar, two parts of middle busbar, negative busbar, and four power switches S_{1L}, S_{3H}, S_{2H} and S_{2L}. The total parasitic inductance L_2 of the green loop is

$$L_2 = L_C + L_o + L_n + 2L_m + 4L_s \quad (2)$$

where L_m is the inductance of the middle busbar.

It can be concluded that the green commutation loop has

larger parasitic inductance than the pink one does, which matches with the analytical result in [6]. Therefore, the pink loop is named as small loop while the green loop is large loop here.

III. Busbar Design

According to the analysis above, to minimize the overall parasitic inductance, the inductance of the power switches, the inductance of busbars, and the ESL of decoupling capacitors should all be taken into consideration.

A. Power Switch Selection

In high power applications, power modules are usually adopted. With the development of packaging technology, the stray inductance inside the module is progressively getting lower. Here, the HT-3000 series SiC MOSFET power modules from Wolfspeed with half bridge structure are used. Fig. 5 shows the picture of the module packaging. According to the datasheet, the stray inductance of the module can be as low as 5 nH.

Fig. 5. Adopted power module.

B. Busbar Design

Busbar is the main source of the inductance in a commutation loops and it is the key point to reduce the parasitics. For a typical busbar with two laminated plates in Fig. 6, the parasitic inductance of a plate includes two parts: self-inductance and mutual inductance.

The self-inductance L of one plate can be calculated with the equation from [8], [19]

$$L=\frac{\mu_0\mu_r l}{\pi}\left(\frac{1}{8}+\frac{2h}{h+w}\right) \qquad (d \ll h \,||\, d+h \ll w) \qquad (3)$$

where μ_0 and μ_r are the vacuum permeability and the relative permeability of the insulation material; l, w and h are the length, width and thickness of the plate; d is the distance between two adjacent plates.

The mutual inductance M between two plates is calculated as [8], [19]

$$M=\frac{\mu_0\mu_r lh}{\pi\sqrt{4(d+h)^2+kw^2}}\cos\varphi \qquad (4)$$

where k is the correction coefficient and φ is the angle between the current direction of two plates.

If the two plates have the same shape and the current directions are opposite, the magnetic fields generated by the currents on two plates have a canceling effect. In such case, the total parasitic inductance of the busbar is

$$L_{sum}=\frac{\mu_0\mu_r l}{\pi}\left(\frac{1}{4}+\frac{4h}{h+w}-\frac{2h}{\sqrt{4(d+h)^2+kw^2}}\right) \qquad (5)$$

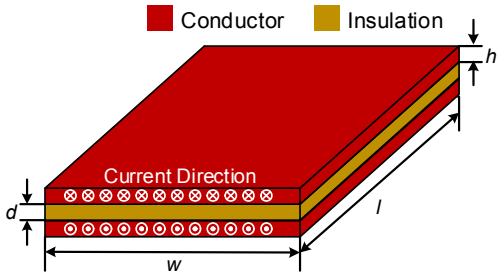


Fig. 6. Typical structure of two-layer busbar.

To minimize the parasitic inductance, it is preferred to increase the mutual inductance between two adjacent busbar layers. In other words, two busbar parts with opposite current directions in Fig. 3 should be overlapped to form the laminated architecture. To simplify the design and reduce the cost, here a two-layer laminated structure is adopted for the required busbar.

In terms of the small commutation loop, it only includes two busbar parts: the neutral busbar and the negative (or positive) busbar. So the two parts should be laminated and located in two layers.

The large commutation loop is more complicated and critical, which consists of four busbar parts: the neutral busbar, negative busbar and two middle busbars. Considering the overall system layout including the placement of SiC MOSFET power modules and the capacitors, Fig. 7 plots the conceptual 3D view of the busbar layout for the large commutation loop. The middle busbars (blue) and the negative (orange) busbar are placed in the same layer. The neutral busbar (yellow) is a whole plate and serves as the return path of the commutation loop. With such design, the busbar parts are coupled and the magnetic field can be canceled with the opposite current flowing direction, resulting in lower loop inductance.

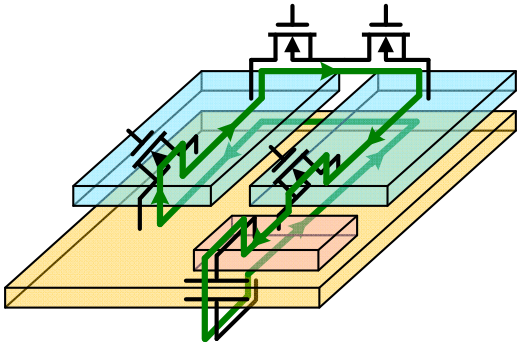


Fig. 7. 3D view of busbar layout with large commutation loop.

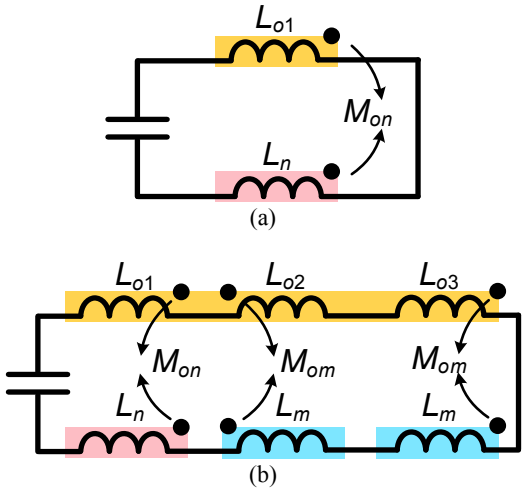


Fig. 8. Equivalent circuits of commutation loops, (a) small loop, (b) large loop.

The equivalent circuits of the commutation loops considering the busbar structure are illustrated in Fig. 8. For the small commutation loop, the negative and neutral busbar are coupled, and the mutual inductance is M_{on}. For the large loop, the negative and middle busbars are coupled with the neutral busbars. The mutual inductance between middle and neutral busbars is M_{om}. Note that the effective self-inductance of the neutral busbar in the small loop (L_{o1}) is smaller than that in the large loop (L_o=L_{o1}+ L_{o2}+ L_{o3}).

Based on Fig. 8, (1) and (2) can be modified as

$$\begin{cases} L_1 = L_C + L_{o1} + L_n - 2M_{on} + 2L_s \\ L_2 = L_C + L_o + L_n + 2L_m - 2M_{on} - 4M_{om} + 4L_s \end{cases} \quad (6)$$

In terms of the implementation, Kapton sheets and epoxy are selected as the insulation material. Kapton sheets are mainly used between two layers while the epoxy is used to seal the edge of the holes and bars. Fig. 9 shows the cross-section of the busbar structure. The distance between two layers is 0.5 mm.

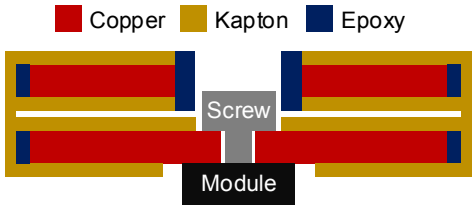


Fig. 9. Cross section of laminated busbar layers.

C. DC-Link Capacitor Selection and Placement

Film capacitors should be used for the DC-link capacitor due to their low ESL. There are two options for the capacitor selection. One is to choose a single bulky capacitor, and the other is to use multiple capacitors in parallel.

Table II shows the comparison of the examples of the two options. The required capacitance of the converter is 300 µF. To achieve 100 µF capacitance for a single-phase, ten smaller capacitors need to be paralleled. However, considering the ESL, weight and price, paralleling capacitors is a better choice. The challenge is to carefully place the capacitors to reach minimized inductance and good current balancing. Ideally, no extra decoupling capacitor is needed as the overall loop inductance is low enough.

Table II. Capacitor comparison.

	Part	Capacitance	ESL	Weight	Price	Qty
	FFVE6K0107K	100 µF	25 nH	350 g	$ 60.00	1
	MKP1848C61060JK2	10 µF	15 nH	15 g	$ 4.20	10

As recommended in [20], the adjacent two paralleled capacitors are placed oppositely. Fig. 10 sketches the top view of the placement of the capacitors on the busbar plate. The red line represents the current on the top layer (positive/negative busbar), and the yellow dotted line is the current on the bottom layer (neutral busbar), while the dark dashed line is the current inside the capacitors. For the left side capacitor, the current flows into the capacitor on the bottom layer, while the current flows out of the right side capacitor through the top layer. Therefore, current on two laminated plates is in opposite directions, which helps the magnetic field cancellation and reduces the total inductance.

Fig. 11 shows the designed busbar plate for DC-link capacitors in one phase. There are ten capacitors in two rows. The orange plate is the negative/positive busbar while the yellow one is the neutral busbar. The finalized busbar design for a single phase is shown in Fig. 12.

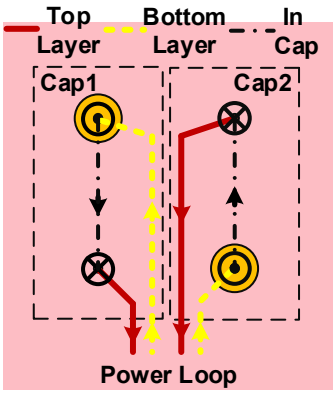


Fig. 10. Top view of busbar with capacitors placement and current flow directions.

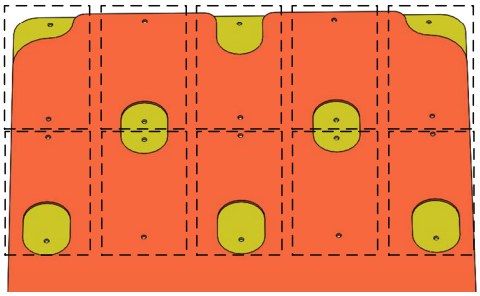


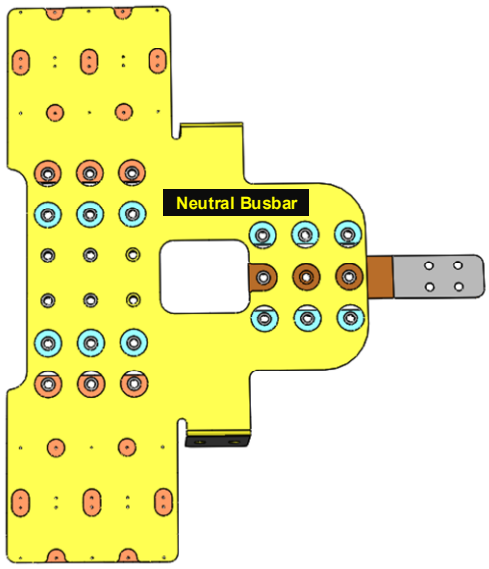
Fig. 11. Designed plate for capacitors.

IV. Simulation and Experimental Results

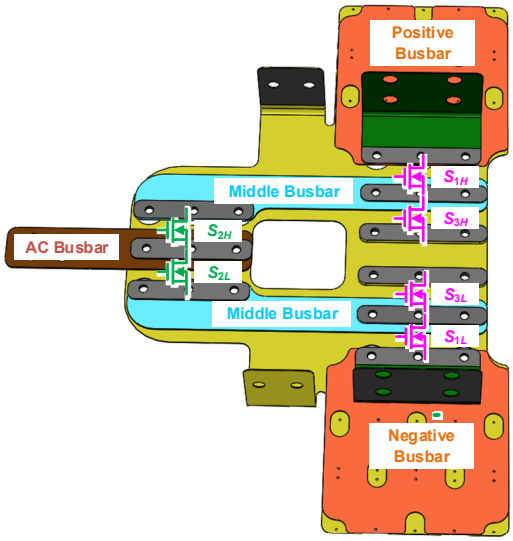
The equivalent circuit of the busbar with parasitics was extracted from Ansys Q3D and simulated in Saber along with the SiC MOSFET module model. Fig. 13 shows the turn-on switching transient of the MOSFET drain-source voltage. The ringing frequency of the small loop is 34.5 MHz while that of the large loop is 18.9 MHz. Based on the output capacitance value from the device datasheet, the parasitic inductances of the small and large loop are calculated as 6.5 nH and 17.5 nH, respectively.

Fig. 14 plots the simulated current waveforms of ten paralleled DC-link capacitors in one switching cycle. The current RMS value of each capacitor is about 8 A, and the largest RMS difference among the capacitors is 0.6 A, which indicates good current balancing in the capacitors.

Fig. 15 presents the prototype for a single-phase 3L-ANPC converter with the fabricated busbar. An impedance analyzer is used to measure the impedance of the busbar loops including the DC-link capacitors but without the power modules. From Fig. 16, the measured small and large loop inductances are 2.5 nH and 10 nH, respectively. Considering the inductance of one power switch L_s is 4 nH, the result can match with the simulation in Fig. 13.



(a) Top view



(b) Bottom view

Fig. 12. Designed laminated busbar for single phase.

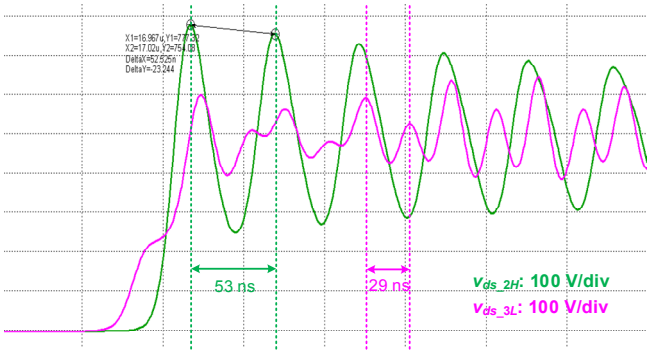


Fig. 13. Simulated switching transient with module model and extracted busbar equivalent circuit.

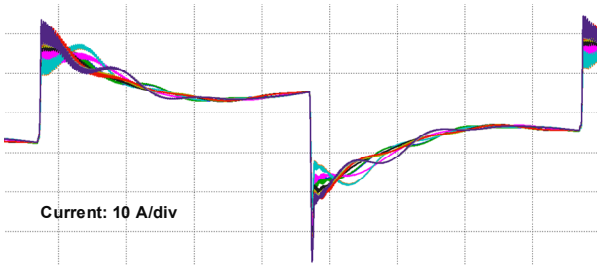


Fig. 14. Simulated current waveforms of ten paralleled DC-link capacitors during one switching cycle.

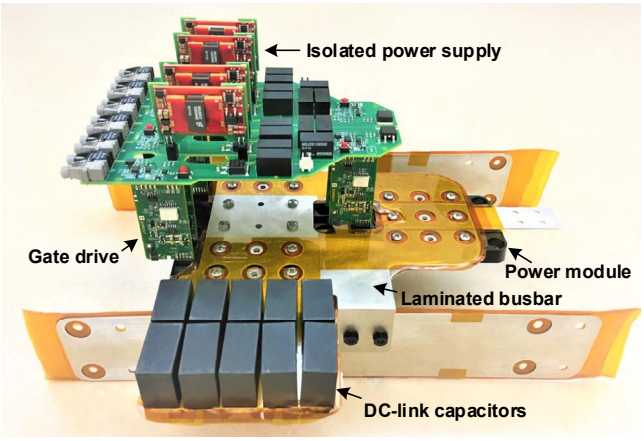


Fig. 15. Prototype of 3L-ANPC converter (single phase).

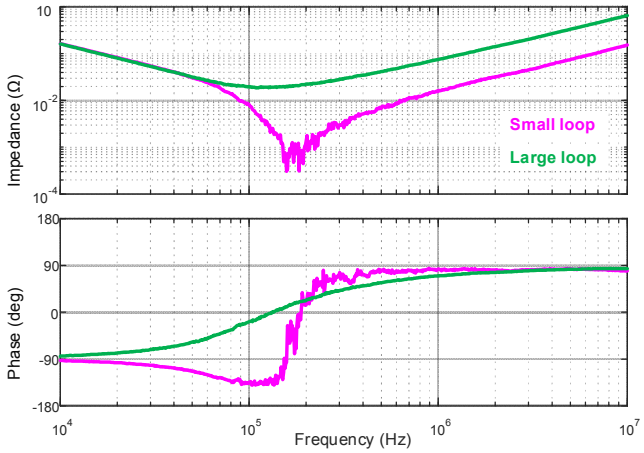


Fig. 16. Measured impedance spectra of busbar.

Fig. 17 shows the testing setup of the three-phase converter. The DC bus voltage V_{dc} is 500 V, the peak load current is 650 A, and the line-to-line output voltage RMS value is 600 V, which corresponds to 500 kVA output power. The switching frequency of the SiC MOSFETs is 60 kHz, and the output line frequency is 3 kHz.

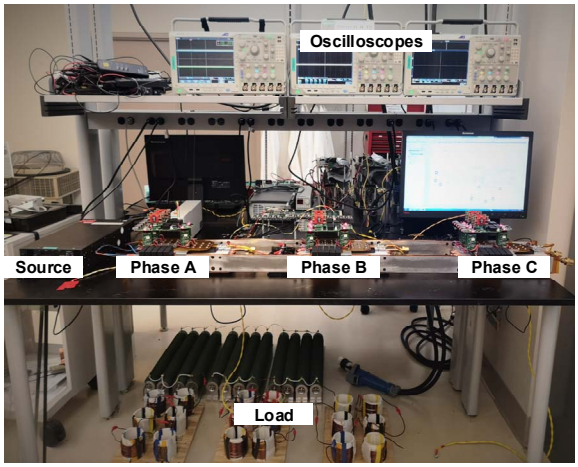


Fig. 17. Testing platform of three-phase 3L-ANPC converter.

Pulse test is conducted to evaluate the function of the converter. Fig. 18 illustrates the tested output voltage and current waveforms of the 3L-ANPC converter with five line cycles generated. The maximum current of Phase B during the first pulse is 648 A, which reaches the peak current at full load condition.

The tested switching transient waveforms are plotted in Fig. 19. The ringing frequencies of the small and large loops are 35.7 MHz and 17.2 MHz, which is very close to the simulation result in Fig. 13. With the low loop inductance, the *dv/dt* of the active switch can be 10 V/ns at full load condition. The peak drain-source voltage of S_{2H} and S_{3L} is 736 V and 754 V respectively, which is lower than the voltage rating of the SiC MOSFET (900 V). No extra snubber circuit is required in the converter.

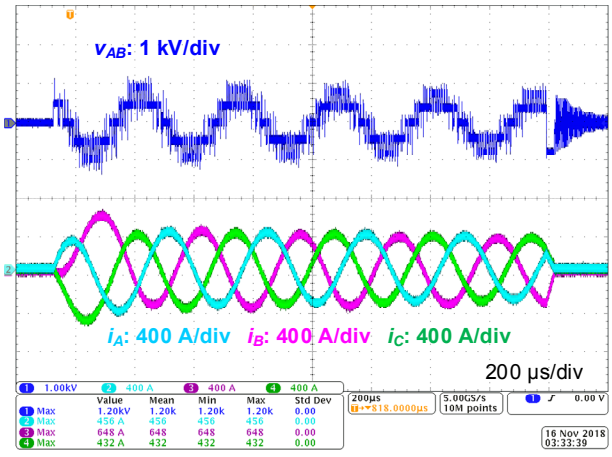
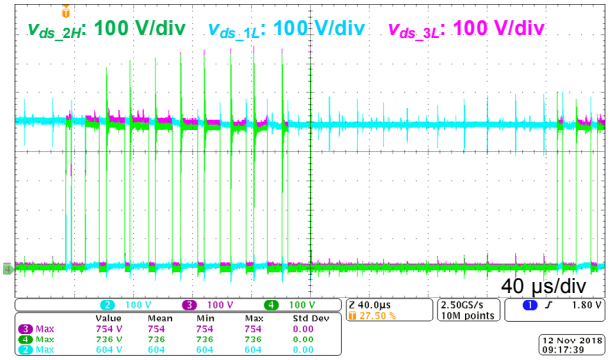
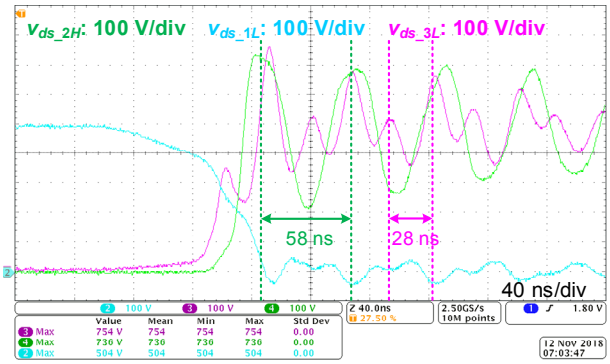


Fig. 18. Tested output waveforms of 3L-ANPC converter.



(a)



(b)

Fig. 19. Tested waveforms of switching transient, (a) one line cycle, (b) switching transient.

Table III compares the loop inductances of the busbar in this paper and those in other NPC type converters. The proposed busbar achieves significantly lower parasitic inductances for both small loop and large loop.

Table III. Loop inductance comparison.

References	This paper	[3]	[4]	[14]	[15]	[16]	[17]
Power (kVA)	500	200	1000	750	N/A	N/A	475
DC voltage (kV)	1	1.2	2.4	2	N/A	N/A	1.1
Small loop (nH)	**6.5**	55	N/A	78	96	47.9	95
Large loop (nH)	**17.5**	135	115	208	150	76.2	118

N/A: Not available

V. Conclusions

This paper presents the design of a laminated busbar for a 500 kVA three-level ANPC converter. With the consideration of multiple commutation loops and the current flowing directions in the converter, the layout of the busbar is specially designed to achieve the magnetic cancellation between adjacent busbar layers. Distributed film capacitors with special placement are adopted to serve as the DC-link capacitors. Due to the low inductance, no decoupling capacitor is needed. Together with the SiC MOSFET power module with low stray inductance, the overall parasitic inductances of small loop and large loop are 6.5 nH and 17.5 nH, respectively. Compared to the high power NPC type converters in other references, the proposed busbar achieves at least 84% and 77% reduction in small and large loop inductances. The experimental results verified the performance of the busbar.

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References

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.,* vol. 57, no. 8, pp. 2553-2580, 2010.

[2] Y. Li, H. Akagi, and F. Peng, "Multilevel converters: recent development of topologies and PWM control methods," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 1-6.

[3] Y. Jiao, S. Lu, and F. C. Lee, "Switching performance optimization of a high power high frequency three-level active neutral point clamped phase leg," *IEEE Trans. Power Electron.,* vol. 29, no. 7, pp. 3255-3266, 2014.

[4] D. Zhang, J. He, and S. Madhusoodhanan, "Three-level two-stage decoupled active NPC converter with Si IGBT and SiC MOSFET," *IEEE Trans. Ind. Appl.,* vol. 54, no. 6, pp. 6169-6178, 2018.

[5] R. Ren, Z. Zhang, B. Liu, R. Chen, H. Gui, J. Niu, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Multi-commutation loop induced over-voltage issue on non-active switches in fast switching speed three-level active neutral point clamped phase leg," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 1328-1333.

[6] H. Gui, Z. Zhang, R. Chen, R. Ren, J. Niu, B. Liu, H. Li, Z. Dong, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "A simple control to reduce device over-voltage caused by non-active switch loop in three-level ANPC converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 2019, pp. 1337-1343.

[7] B. Liu, R. Ren, E. A. Jones, H. Gui, Z. Zhang, R. Chen, F. Wang, and D. Costinett, "Effects of junction capacitances and commutation loops associated with line-frequency devices in three-level ac/dc converters," *IEEE Trans. Power Electron.,* vol. 34, no. 7, pp. 6155-6170, 2019.

[8] Y.-f. Zhu and Z. Zheng, "The impact of layer number on stray inductance of dc-link busbar in power converters," *The Open Electrical & Electronic Engineering Journal,* vol. 7, no. 1, pp. 98-102, 2013.

[9] R. Alizadeh, M. Schupbach, T. Adamson, J. C. Balda, Y. Zhao, S. Long, K. W. Jung, C. R. Kharangate, M. Asheghi, and K. E. Goodson, "Busbar design for distributed DC-link capacitor banks for traction applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 4810-4815.

[10] A. D. Callegaro, J. Guo, M. Eull, B. Danen, J. Gibson, M. Preindl, B. Bilgin, and A. Emadi, "Bus bar design for high-power inverters," *IEEE Trans. Power Electron.,* vol. 33, no. 3, pp. 2354-2367, 2018.

[11] C. Chen, X. Pei, Y. Chen, and Y. Kang, "Investigation, evaluation, and optimization of stray inductance in laminated busbar," *IEEE Trans. Power Electron.,* vol. 29, no. 7, pp. 3679-3693, 2014.

[12] J. Wang, S. Yu, and X. Zhang, "Effect of key physical structures on the laminated bus bar inductance," in *IEEE International Power Electronics and Motion Control Conference*, 2016, pp. 3689-3694.

[13] N. Chen and M. Nawaz, "Current sharing design assessment of DC link capacitor module," in *Proc. IEEE Conf. Power Electron. Appl.*, 2014, pp. 1-9.

[14] J. Wang, B. Yang, J. Zhao, Y. Deng, X. He, and X. Zhixin, "Development of a compact 750KVA three-phase NPC three-level universal inverter module with specifically designed busbar," in *Proc. IEEE Appl. Power Electron. Conf.*, 2010, pp. 1266-1271.

[15] L. Popova, T. Musikka, R. Juntunen, M. Lohtander, P. Silventoinen, O. Pyrhönen, and J. Pyrhönen, "Modelling of low inductive busbars for medium voltage three-level NPC inverter," in *Proc. IEEE Power Electron. Mach. Wind Appl.*, 2012, pp. 1-7.

[16] L. Popova, R. Juntunen, T. Musikka, M. Lohtander, P. Silventoinen, O. Pyrhönen, and J. Pyrhönen, "Stray inductance estimation with detailed model of the IGBT module," in *Proc. IEEE Conf. Power Electron. Appl.*, 2013, pp. 1-8.

[17] F.-Y. He, S.-Z. Xu, and C.-F. Geng, "Improvement on the laminated busbar of NPC three-level inverters based on a supersymmetric mirror circulation 3D cubical thermal model," *J. Power Electron.,* vol. 16, no. 6, pp. 2085-2098, 2016.

[18] H. Yu, Z. Zhao, T. Lu, L. Yuan, and S. Ji, "Laminated busbar design and stray parameter analysis of three-level converter based on HVIGBT series connection," in *Proc. IEEE Appl. Power Electron. Conf.*, 2015, pp. 3201-3207.

[19] N. R. Mehrabadi, I. Cvetkovic, J. Wang, R. Burgos, and D. Boroyevich, "Busbar design for SiC-based H-bridge PEBB using 1.7 kV, 400 a SiC MOSFETs operating at 100 kHz," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1-7.

[20] "Design considerations for designing with Cree SiC modules," Cree. 2013. [Online]. Available: http://www.cree.com.