Schematics for Diagram

Waveform showing timing of key signals

Signals: Read\_Write\_n

Delayed slightly after clock, falls afterwards

Word Signals:

Delays: clk, word register output, word enable

Word register signals first switched on rising clock

Word Output goes high on enable signal (clk\_n)

Word output switches between read and write address after read\_write\_n

Clk:

Defined by input (no delay)

Advances shift registers when valid

Latches output FF and input FF

Precharge\_en:

Tied to clock

Enable Word signal:

Not clk

Allows word outputs to be non-zero (otherwise)

Description of memory operation and design choices

Breakdown of energy contribution by function

Description of how energy was optimized

Summary of design metrics