I. Intel CPUs

A. Ice Lake

Ice Lake is Intel's codename for the 10th generation Intel Core processors based on the new Sunny Cove microarchitecture. Ice Lake was expected to replace microprocessors based on the Skylake microarchitecture.

Features:

1) *Sunny Cove* micro-architecture.
2) increase the execution units(EUs) to 64, from 24 or 48 in Gen 9.5 graphics.
3) Each EU supports 7 threads.
4) 50% increase in the size of L1, L2 cache, larger μOP cache, and larger 2nd level `TLB`.
5) 3MB L3 cache.
6) 1 TFLOPS of compute performance.

Focus: Single-thread performance, new instructions(`VPOPCNTDQ, VBMI2, BITALG, VPCLMULQDQ, GFNI, and VAES`), and scalability.

a) `VPOPCNTDQ:` Count the number of logical 1 bits in packed 32-bit integers in a, and store the results in dst.

syntax: `__m512i _mm512_popcnt_epi32 (__m512i a)`

b) `VBMI2:`

c) `BITALG:`

d) `VPCLMULQDQ:` Carry-less multiplication of one quadword of 'b' by one quadword of 'c', stores the 128-bit result in 'DEST'. The immediate 'Imm8' is used to determine which quadwords of 'b' and 'c' should be used.

syntax: `__m512i _mm512_clmulepi64_epi128 (__m512i b, __m512i c, const int Imm8)`

e) `GFNI:`

f) `VAES:` Perform one round of an AES decryption flow on data (state) in a using the round key in RoundKey, and store the results in dst.

syntax: `__m512i _mm512_aesdec_epi128 (__m512i a, __m512i RoundKey)`

B. `Tiger Lake`

`Tiger Lake` is an Intel core processor to replace `Ice Lake`.

Features:

1) Intel Willow Cove CPU cores.
2) Intel Xe ("Gen12") GPU with up to 96 execution units.
3) HEVC 12-bit, 4:2:2 & 4:4:4 fixed-function hardware decoding & VP9 12-bit & 4:4:4 fixed-function hardware decoding.
4) PCI Express 4.0.
5) Thunderbolt 4.
6) Miniaturization of CPU and motherboard into an M.2 SSD-sized small circuit board.
7) LPDDR5 memory.
8) New Deep Learning Boost (DL Boost) extensions for built-in AI training acceleration in Xeon processors.
9) A new AVX-512 instruction: Vector Pair Intersection to a Pair of Mask Registers (VP2INTERSECT).

AVX-512 Subset	F	CD	ER	PF	4FMAPS	4VNNIW	VPOPCNTDQ	VL	DQ	BW	IFMA	VBMI	VNNI	BF16	VBMI2	BITALG	VPCLMULQDQ	GFNI	VAES	VP2INTERSECT
Knights Landing (Xeon Phi x200) processors (2016)	Yes		Yes		No															
Knights Mill (Xeon Phi x205) processors (2017)					Yes		Yes	No												
Skylake-SP, Skylake-X processors (2017)			No					Yes			No									
Cannon Lake processors (2018)							No				Yes	No								
Cascade Lake processors (2019)					No						No		Yes	No						
Cooper Lake processors (2020)														Yes	No					
Ice Lake processors (2019)							Yes				Yes			No	Yes					No
Tiger Lake processors (2020)																				Yes

Fig. 1. Avx-512 instruction sets for different Intel core processor[wiki].

II. Intel GPU

Code Name: `DG1`

III. AMD Processors

A. Ryzen