CENTER OF NANOELECTRONICS & DEVICES

CND 101: Introduction to Analog Electronics

Report#: 1

Programmable CMOS Ring Oscillator

Section #: 17

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I. Abstract

The ring oscillator is an odd number of inverters connected in a series form with positive feedback & output oscillates between two voltage levels either one or zero to measure the speed of the process. In place of inverters, we can define it with NOT gates also. These oscillators have an 'N' odd number of inverters. For instance, if this oscillator has three inverters, it is called a three-stage ring oscillator. The number of inverter stages in this oscillator mainly depends on the frequency which we want to generate from this oscillator.In this paper, We focused on designing, analyzing, and implementing a ring oscillator for frequency generation.

II. Introduction

Ring oscillators are widely used in various applications, such as clock signal generation, frequency synthesizers, and delay-line elements in digital systems. Ring oscillator uses an odd number of inverters to achieve more gain than a single inverting amplifier. The inverter gives a delay to the input signal and if the numbers of inverters are increased then oscillator frequency will be decreased. So the desired oscillator frequency depends on the number of inverter stages of the oscillator. The design of the ring oscillator can be done using three inverters. If the oscillator is employed with a single-stage, then the oscillations & gain are not sufficient. If the oscillator has two inverters, then the oscillation and gain of the system are a little bit more than the single-stage ring oscillator. So this three-stage oscillator has three inverters that are connected in the form of a series with a positive feedback system. So the oscillations & the gain of the system are sufficient. This is the reason to choose the three-stage oscillator.

In this paper we designed and simulated a programmable CMOS ring oscillator using Cadence virtuoso. This Ring oscillator operates at frequencies (1 MHz, 5 MHz, 10 MHz). We achieved this outcome by changing one the Transistor sizing and Number of inverting stages. We also ensured that the output waveform should be balanced (rise time = fall time) by optimizing the Gate width ratio.

III. Background

In all physical systems, oscillatory behavior is common, particularly in optical and electronic systems. Oscillators are utilized for channel selection and information signal frequency translation in radio frequency and lightwave communication systems. Oscillators are also found in all digital electronic systems, which need a clock signal or other time reference to synchronize their processes. A perfect time reference, or periodic signal, would be produced by an ideal oscillator. Nevertheless, unwanted noise or disturbance taints every physical oscillator. Because an oscillator is a noisy physical system, it produces signals that are not exactly periodic, which makes them distinctive in how they react to noise or perturbation.

There are many different types of oscillators accessible, but each class of oscillator has a unique operating mechanism, oscillation frequency range, and noise performance. Recently, monolithic oscillators with low costs and power dissipation have become necessary for communication transceiver design in single integrated circuits. In contrast to previous monolithic oscillators like relaxation oscillators, the design of the ring oscillator in this system, which uses delay stages inside the IC, has produced significantly more relevance. Although it is not as good as sinusoidal oscillators, ring oscillators often perform better than relaxation oscillators. However, the persistent efforts of scientists and researchers have resulted in ring

oscillator performance being improved to a good degree of satisfaction which yielded highly achievable outcomes in both cases: operation speed and noise performance.

A ring oscillator is a closed-loop chain made up of a cascaded arrangement of delay stages. Due to its many practical properties, ring oscillators built with a series of delay stages have generated interest. These appealing features are: (i) Its basic structure allows for easy design using the latest integrated circuit technology (CMOS, BiCMOS); (ii) Its oscillations can be achieved at low voltage; (iii) It can provide high frequency oscillations with low power dissipation; (iv) It can be electrically tuned; (v) It can provide a wide tuning range; and (vi) It can provide multiphase outputs. These outputs can be logically coupled to create multiphase clock signals, which are useful for many different communication system applications.

IV. Technical detail and simulation results

A. Technical details

The propagation delay τd per stage and the total number of stages in the ring construction determine the oscillation frequency of a ring oscillator. The ring needs to have unity voltage gain at the oscillation frequency and a phase shift of 2π in order to produce self-sustaining oscillation. Each stage of an N-stage ring oscillator contributes a phase shift of π/N, with the remaining π phase shift coming from dc inversion. Therefore, the oscillating signal must go through each of the N delay stages once to provide the first π phase shift in a time of N* τd and it must go each stage a second time to obtain the remaining π hase shift in a time period of 2*N* τd. Thus the frequency of oscillation is given by:

$$\text{frequency} = 1 \div (2 * N * \tau d) \qquad \text{Equation 1}$$

The number of inverter stages used in the ring structure and the propagation delay of the delay stages limit the oscillation frequency of the ring oscillator.

B. Simulation results

Using Cadence Virtuoso, We designed a Ring oscillator using CMOS technology to operate at frequencies (1 MHz, 5 MHz, 10 MHz). We accomplished this by using switches to reach each frequency and also Changed the number of inverting stages and changed the transistor size by a ratio nearly 2 .

First of all, We designed the A ring Oscillator that operates at 1 MHz using 11 stages by using an 65 Nm technology and we put a capacitor after each stage with various capacitance. We used 65nm channel length for both The NMOS and PMOS transistors. We concluded that the PMOS width nearly two times the width value of the NMOS transistor size Which was 1um.Then, We did a transient analysis of 1u to obtain our result .After that, we set an initial condition for the feedback gain to be in order to start our simulation. In Addition, We set a stimulus of dc volt and set our Vdc equal to 800m to make our ring oscillator operate on low power . Furthermore, We calculated the power using the power equation VDD*iD by the calculator in the tool . Moreover, We used parametric analysis to calculate the Ratio between the Channel Width of PMOS and NMOS transistors to balance the output waveform (rise time = fall time) . Finally we calculate the delay in each stage using the Input and Output of each stage and compare them with the circuit analysis.

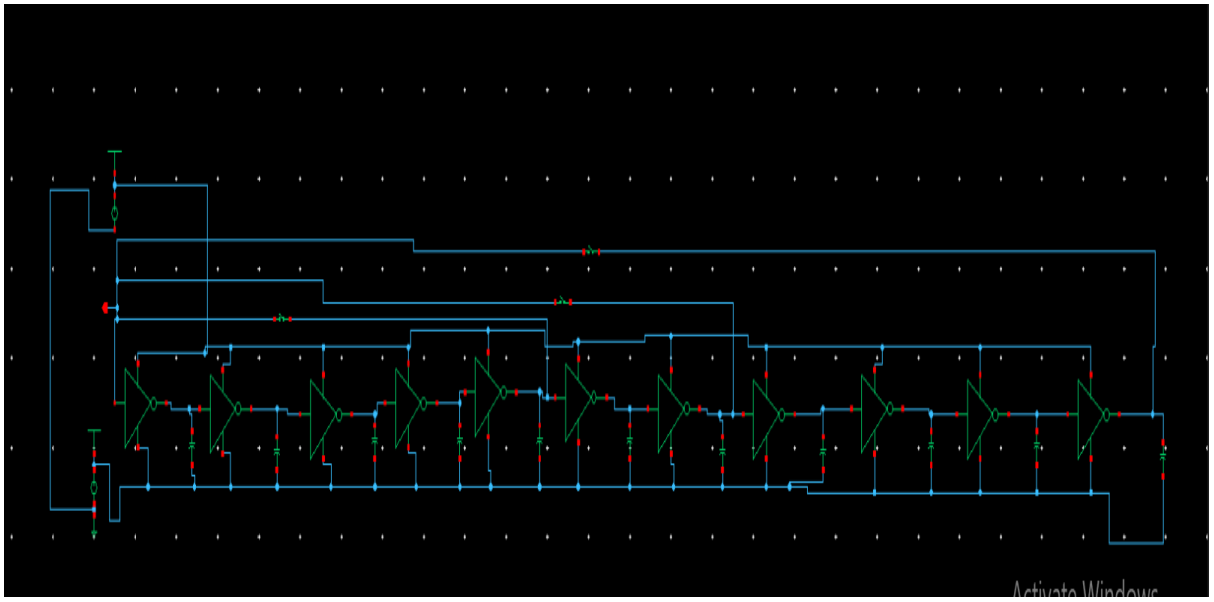

fig (1) The final design of Ring Oscillator

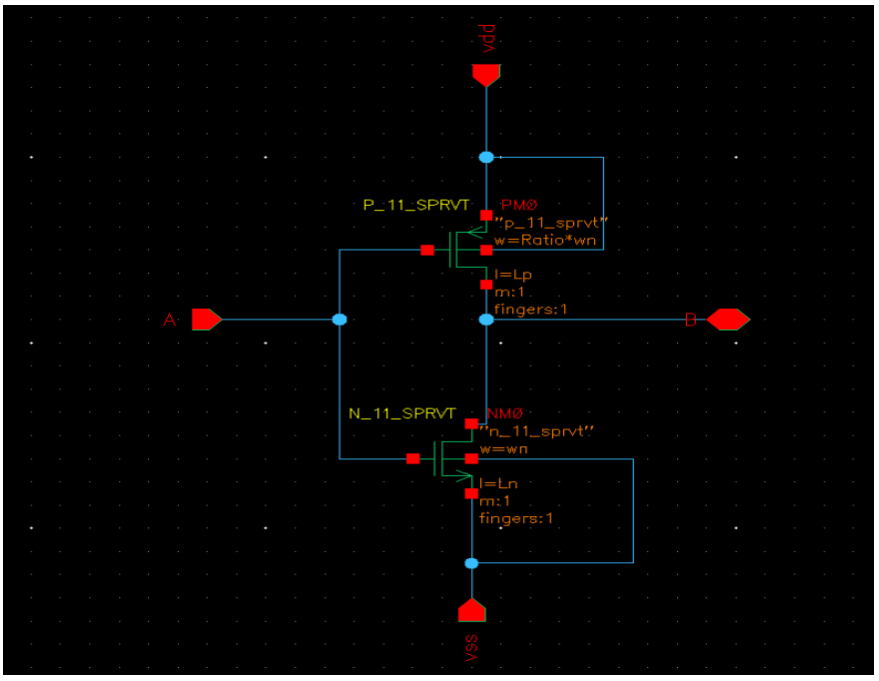

fig (2) The inverter Schematic

1. *Frequency of 10 MHz*

- *First of all , we set the switch that operates the five stages to one*
- *Then , WE did the transient analysis*
- *After that , We did Parametric analysis to get the Ratio Between the width of PMos and NMOS to make the rise time equal the fall time*
- *Moreover , we calculated the the power using ID from Vdc source*
- *Most importantly. we equate the five capacitor in this stage = 5.2pF*
- *Finally , we Calculated the delay using the input of the fifth stage and the output from the feedback loop.*

The Results we obtained in five stages ring oscillator

- ☐ *We obtained a Frequency = 10.29 MHz*
- ☐ *The Rise time = Fall time = 13ns*
- ☐ *The average power consumption = 413.209u Watts*
- ☐ *The td= 9.4511ns*

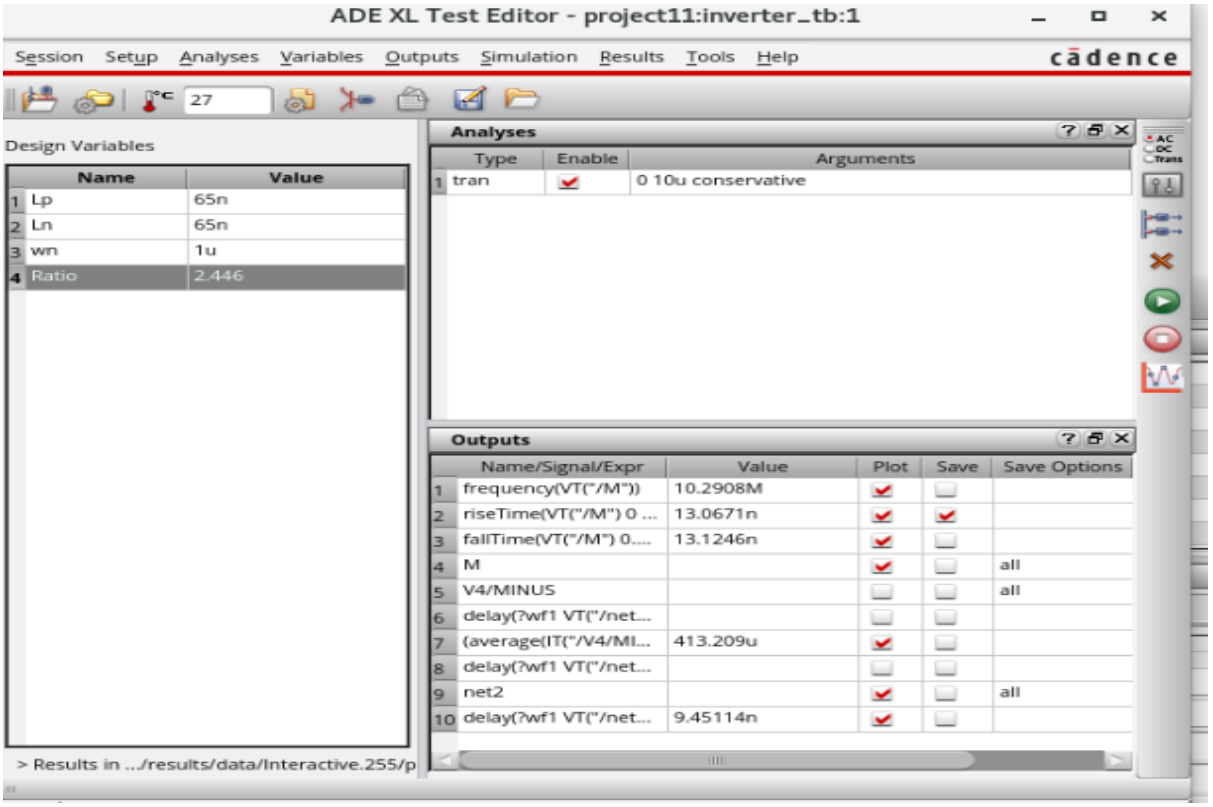

fig (3) The ADE XL showing the result of 5 stages Ring Oscillator

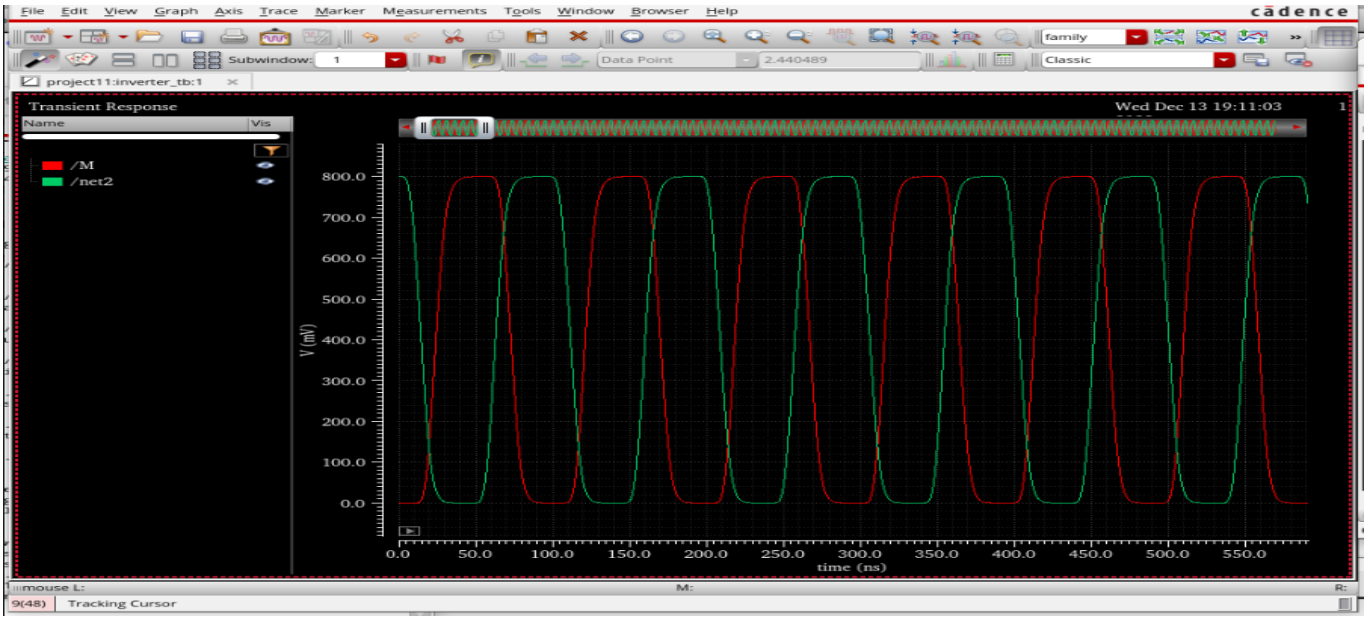

fig (4) The output waveform of 5 stages Ring Oscillator

2. *Frequency of 5 MHz*

- *First of all , we set the switch that operates the seven stages to one and opened the other two switches*
- *Then , WE did the transient analysis*
- *After that , We did Parametric analysis to get the Ratio Between the width of PMos and NMOS to make the rise time equal the fall time*
- *Moreover , we calculated the the power using ID from Vdc source*
- *Most importantly. we equate the first five capacitor in this stage = 5.2pF and the following two capacitor to 14pF*
- *Finally , we Calculated the delay using the input of the seven stage and the output from the feedback loop.*

The Results we obtained in five stages ring oscillator

- ☐ *We obtained a Frequency = 5.02153 MHz*
- ☐ *The Rise time = Fall time = 35ns*
- ☐ *The average power consumption = 343.109u Watts*
- ☐ *The td= 24.9491ns*

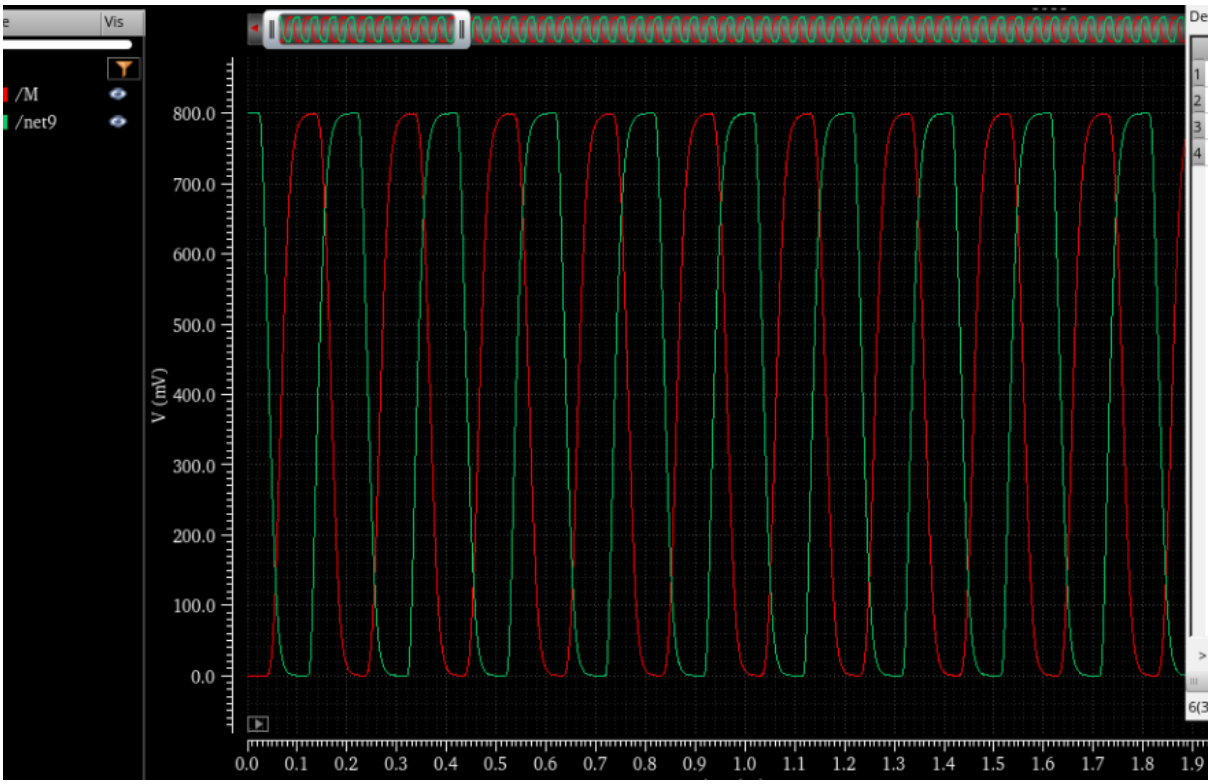

fig (5) The output waveform of 7 stages Ring Oscillator

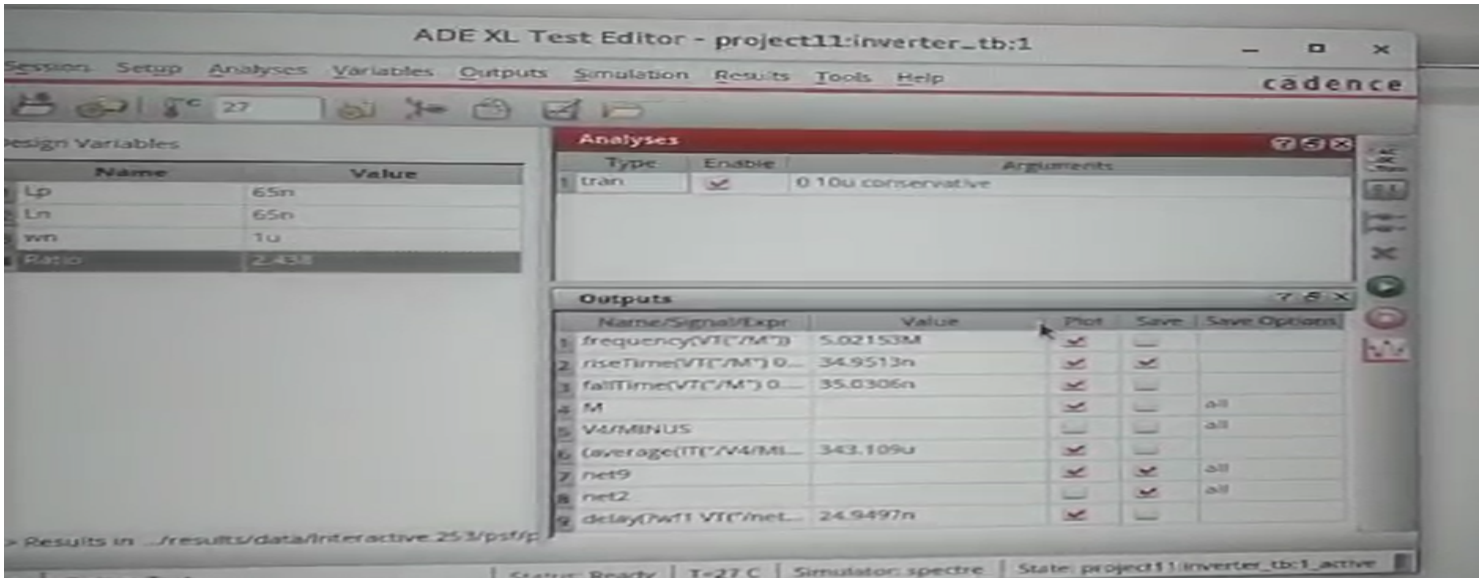

fig (6) The ADE XL showing the result of 7 stages Ring Oscillator

3. *Frequency of 1 MHz*

- *First of all , we set the switch that operates the eleven stages to one and opened the other two switches*
- *Then , WE did the transient analysis*
- *After that , We did Parametric analysis to get the Ratio Between the width of PMos and NMOS to make the rise time equal the fall time*
- *Moreover , we calculated the the power using ID from Vdc source*
- *Most importantly. we equate the first five capacitor in this stage = 5.2pF and the following two capacitor to 14pF and the final four capacitor to 49pF*
- *Finally , we Calculated the delay using the input of the eleven stage and the output from the feedback loop.*

The Results we obtained in five stages ring oscillator

- ☐ *We obtained a Frequency = 1.1142 MHz*
- ☐ *The Rise time = Fall time = 122ns*
- ☐ *The average power consumption = 178.762u Watts*
- ☐ *The td= 88.8347ns*

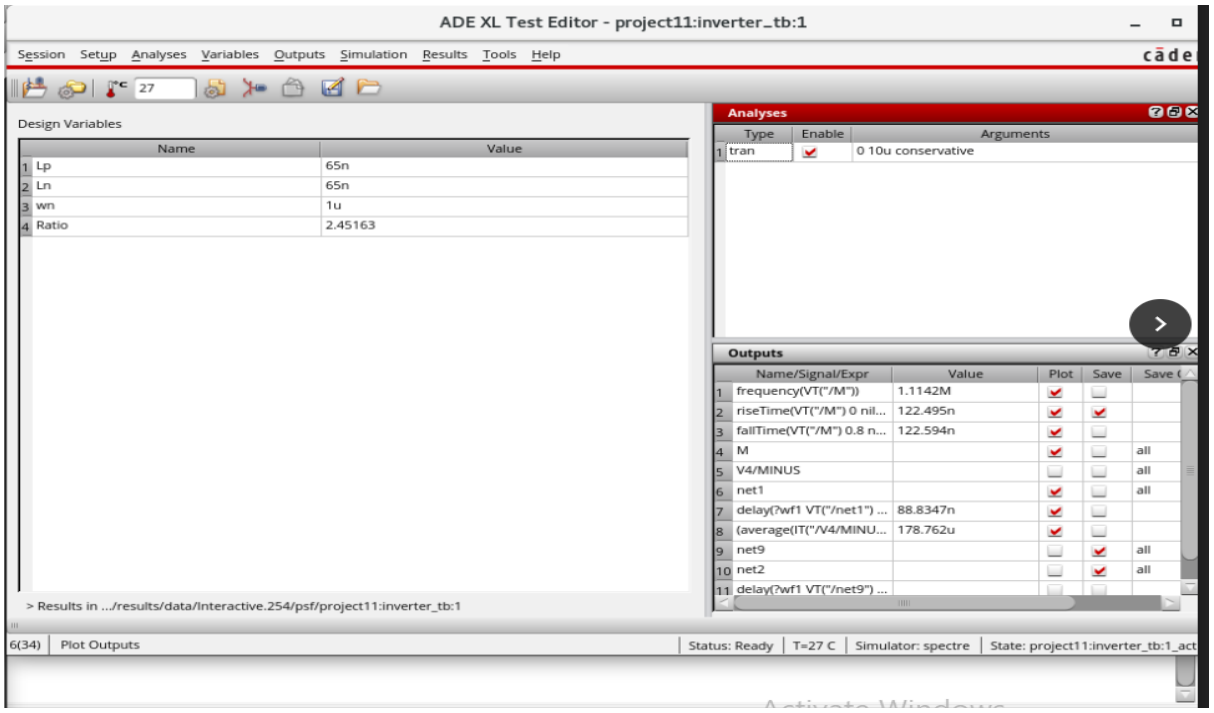

fig (7) The ADE XL showing the result of 11 stages Ring Oscillator

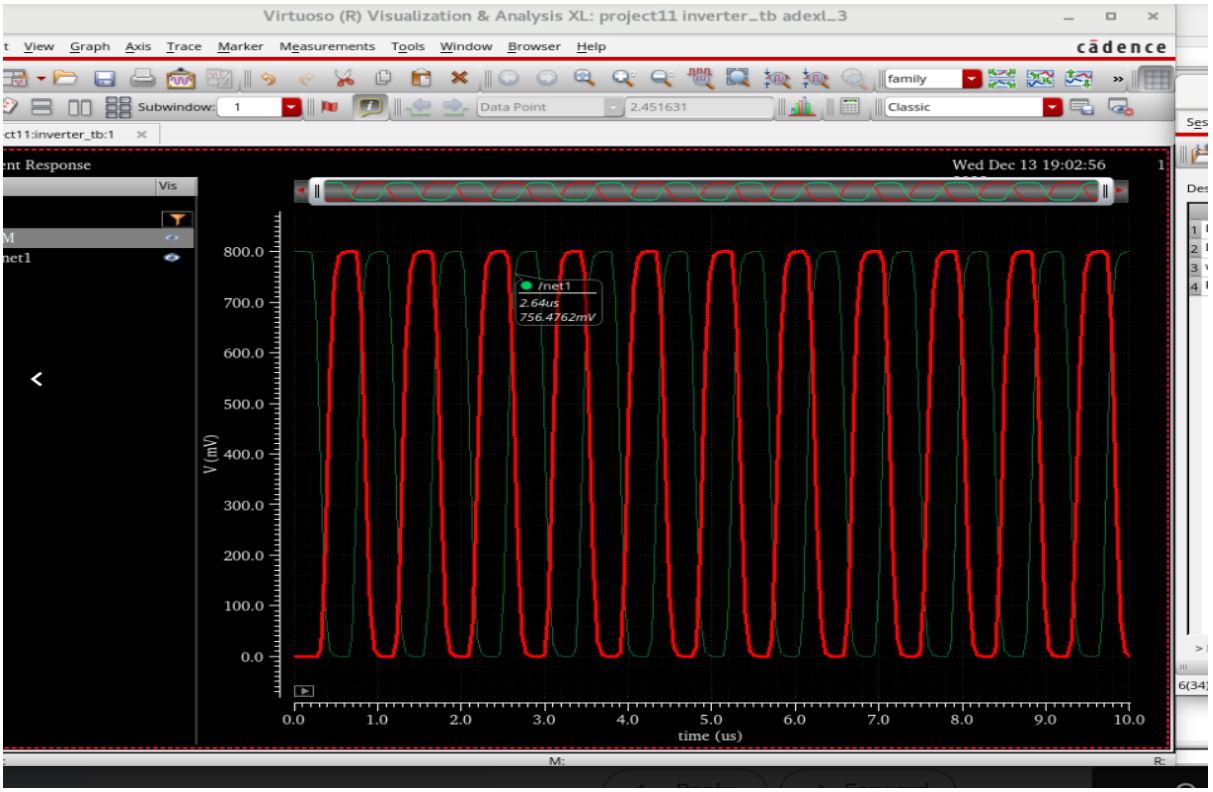

fig (8) The output waveform of 11 stages Ring Oscillator

V. *Comparison between the circuit analysis and simulation results*

From equation 1 we know that the the frequency of oscillation is given by:

$$\text{frequency} = 1 \div (2 * N * \tau d)$$

We must take in consideration that there is A capacitor charging and discharging that will cause time Constant that will add to delay as there is a variation in the value of capacitance used in the design as we equate the first five capacitor in this stage = 5.2pF and the following two capacitor to 14pF and the final four capacitor to 49pF

Ring Oscillator	***5 stages***	***7 stages***	***stages***
Frequency	*10.29 MHz*	*5.02153 MHz*	*1.1142 MHz*
Rise time & fall time	*13ns*	*35ns*	*122ns*
Power	*413.209 u Watts*	*343.109 u Watts*	*178.762 u Watts*
τd ***simulated***	*9.4511ns*	*24.9491ns*	*88.8347ns*
τd *Hand analysis*	*9.7ns*	*24ns*	*65ns*

fig (8) The Comparison table in all the stages of Ring Oscillator

VI. Bonus output sinusoidal wave

We got the output sinusoidal wave from the five stage by equating the first two capacitor to 2pF then the third capacitor to 3pF and the final 2 capacitor 10pF

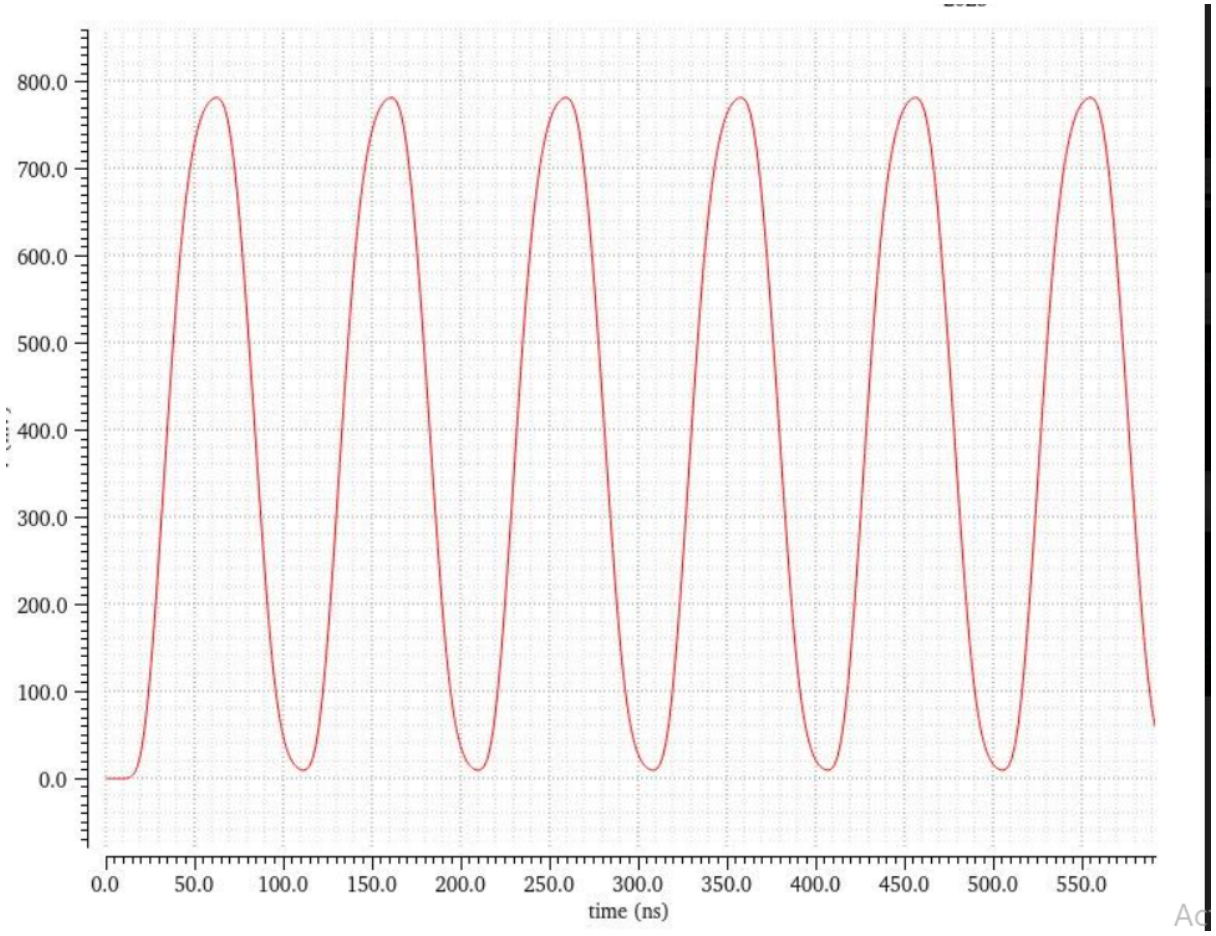

fig (9) The output waveform of sinusoidal wave

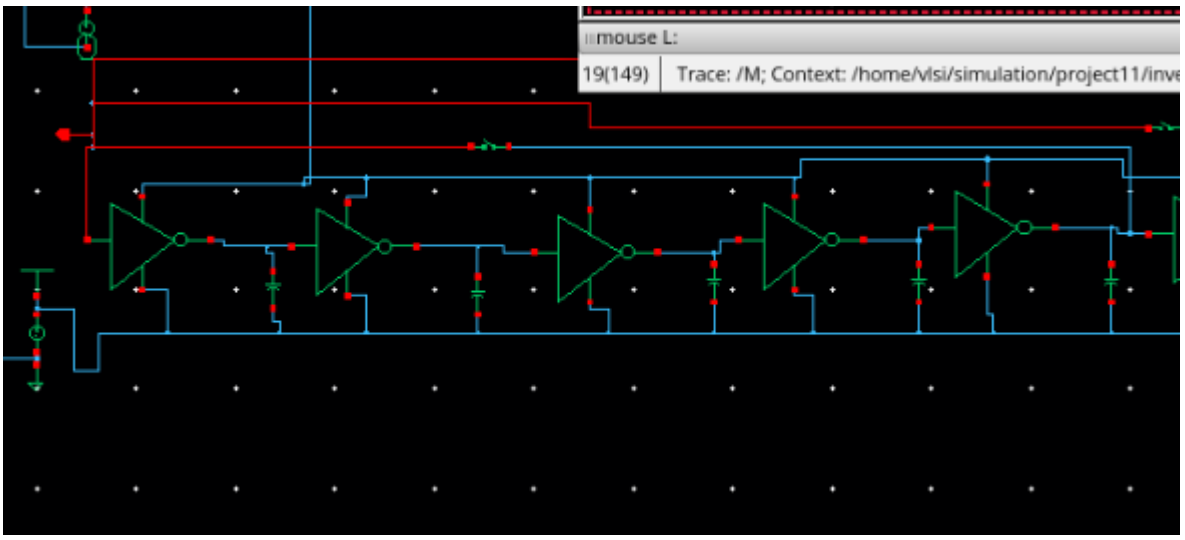

fig (11) The schematic of ring oscillator for sinusoidal wave

VII. Discussion and conclusion

Ring oscillator uses an odd number of inverters to achieve more gain than a single inverting amplifier. The inverter gives a delay to the input signal and if the numbers of inverters are increased then oscillator frequency will be decreased. So the desired oscillator frequency depends on the number of inverter stages of the oscillator. The oscillation frequency of an Ring oscillator depends on the propagation delay of the inverter stages. We determined The smallest propagation delay time by the structure of the inverter stage, transistor sizing and design technology and we increased it by incorporating additional voltage control delay (capacitive load) at the output of the inverter stage. Therefore we operated the ring oscillator at frequencies (1 MHz, 5 MHz, 10 MHz) while maintaining the balance of the waveform rise time=fall time.

VIII. Acknowledgement

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IX. References

[1] Alioto M & Palumbo G, IEEE Trans on Circuits and Syst I, 48 (2001) 210.

[2] Docking S & Sachdev M, IEEE J Solid State Circuits, 39 (2004) 533.

[3]Lee S J, Kim B & Lee K, IEEE J Solid State Circuits, 32 (1997) 289.

[4] Yan G, Zhongjian C, Wennan F & Lijiu J, IEEE Int Conf on Solid State and Integrated Circuits Technology, (2004) 1333.

[5] Sun L & Kwasniewski T A, IEEE J Solid State Circuits, 36 (2001) 910.