chipions program

second digital design project (pipeline) report

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contents

system specification - design approach

The proposed embedded system is required to :

A. monitor the temperature of a pipe line.
B. communicate and report the temperatures measured periodically to a remote database,exactly every 15 minutes.
C. have the capability of shutting down a pipeline or signaling an alarm if dangerous temperature levels are reached,automatically.

As evident from the brief specification,the system should have the following components:

1. analog subsystem consisting of the heat sensor and the analog to digital converter.
2. digital subsystem consisting of a simple finite state machine assuming control of the alarm and shutdown operations.
3. digital communication subsystem responsible for the transmission of the sensor readings to the remote host or database system,which can be implemented using the UART .

detailed specification:

- the alarm should sound if the temperature exceeds 250 degrees celsius , a shutdown signal is produced after 300 degrees.
- a complete UART system design is required ,fitted with error detection mechanisms and basic host signaling techniques.

design approach

- Both the alarming and shutting down signals could be the outputs of a simple finite state machine ‘controller’ which has as it’s input the digital reading of the temperature.
- The digital clock required has two main jobs:
  first: indicating the current time and date on a screen,
  the module has a timestamp output which could be decoded to drive a display screen.
  second: it should send an enable pulse to the UART subsystem,in particular to the Tx module, every 15 minutes.
- The UART module is designed to be a general purpose digital communication system with a input/output data buses of one byte width ,with baud rates 1200,2400,4800,9600 and with parity/overrun error detection capability, and basic host signaling mechanism.

Block diagrams of the system and subsystems

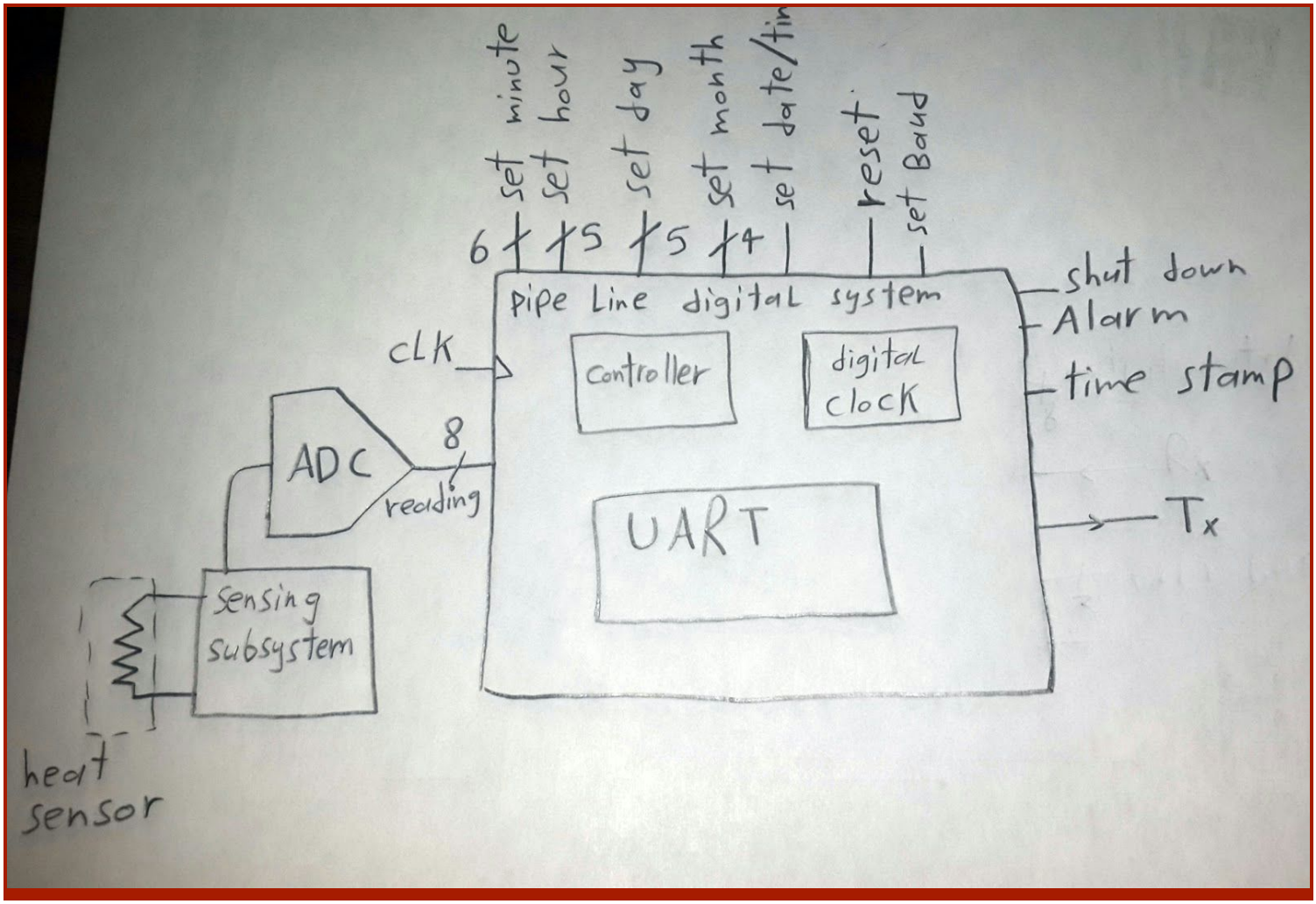


diagram for the complete system

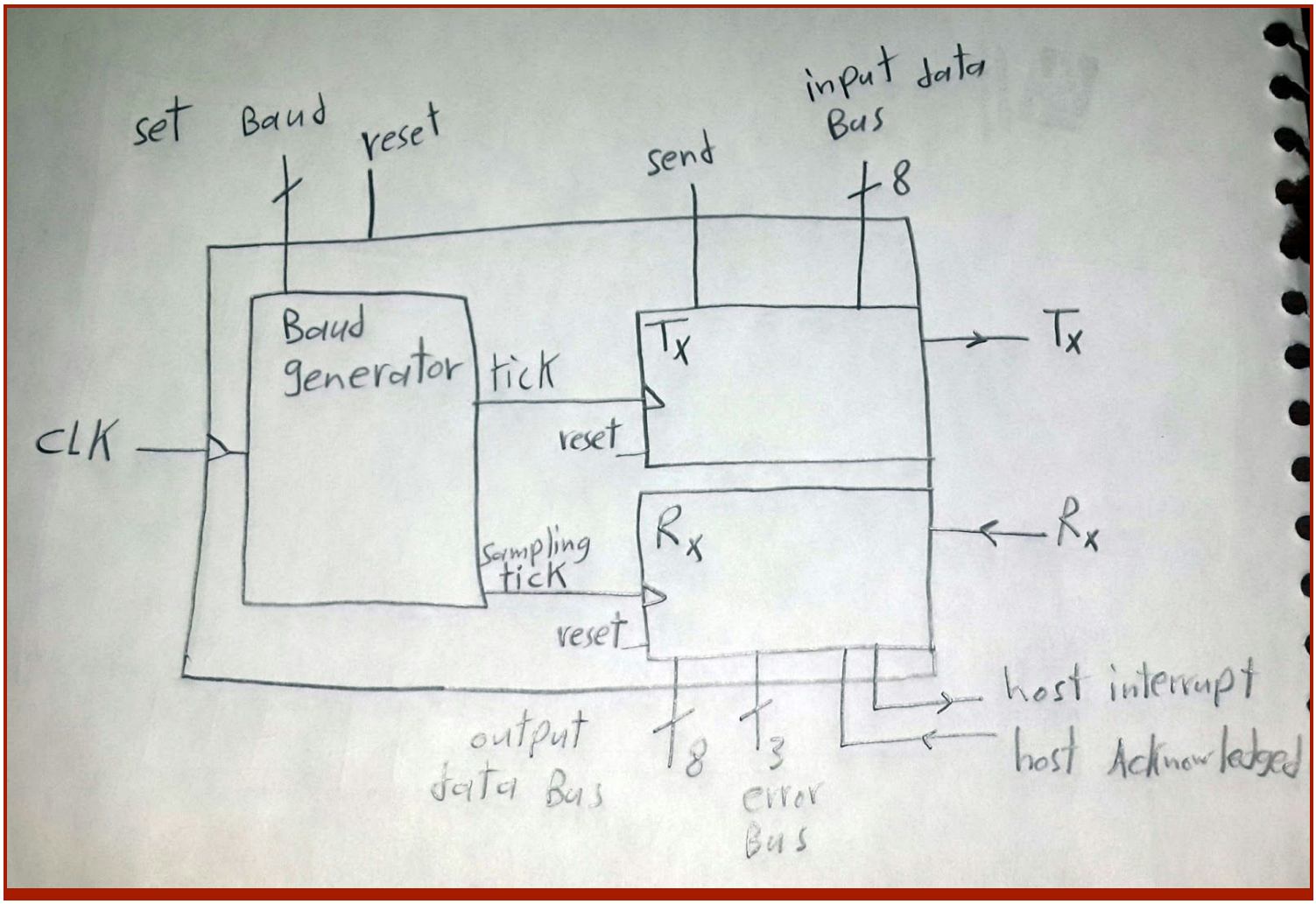
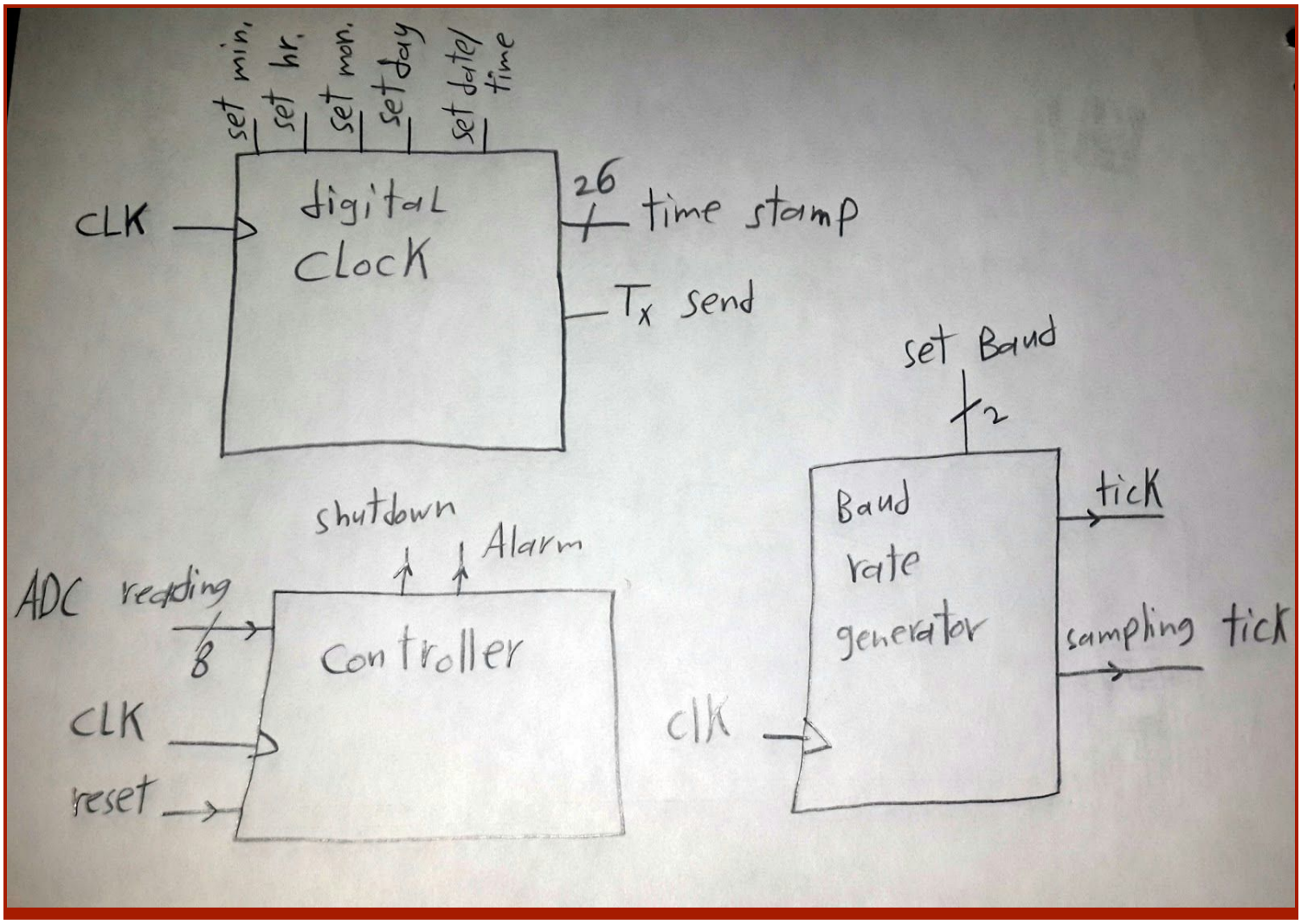


diagram for the UART system



diagrams for the baud generator,controller and digital clock modules

system ports description

top level module

port	description
CLK	input ,system clock 50 MHz
RESET	input,active low,resets the controller and UART components.
shut_down	output,signals a shutdown operation when the temperature exceeds a certain limit.
alarm	output,signals an alarm when the temperature exceeds a certain limit.
ADC_reading	input,8 bits,connected to the analog to digital converter output,carries the sensor reading in digital form.
set_min	input,6 bits,external minute setting for the digital clock.
set_hr	input,5 bits,external hour setting for the digital clock.
set_day	input,5 bits,external day setting for the digital clock.
set_mon	input,4 bits,external month setting for the digital clock.
set_date_time	input,active high,sets the digital clock counters to specific values.

tstamp	output,26 bits,timestamp output indicating time and date,to be decoded externally.
set_baud	input,2 bits,sets the UART transmission rate,encodes 4 values.
Tx	output,serial output of the system,carries the ADC reading to the remote host system.

Testing strategy

a comprehensive strategy for testing the system must assure the proper operation of all the digital system components.

a testbench of the controller module should provide the test vectors representing the cases when temperature exceeds both points of alarm and shutdown temperatures.

testing the UART module should include test vectors with edge cases for the sensor reading, for example: a data word with all 1's or 0's , also parity and overrun errors should be introduced to observe whether the receiver module detects these errors reliably.