Cairo University
Faculty of Engineering
Computer Engineering

Computer Architecture
Lab 3

You are required to build the following:

- A register file which contains 8 registers, each register has 8-bits widths. The register file has 2-read address and 1- write address. It also has 2- read ports and 1-write port. It also has a write enable and a reset signal. (What is the size of address bus? What is the size of data bus?)
- Use the given registers (DFF) to create the register files.
- Create testbench to do the following:
    - Reset all registers, set all read addresses to zero
    - Write in Reg(0) 0xFF
    - Write in Reg(1) 0x11
    - Write in Reg(7) 0x90
    - Write in Reg(3) 0x08
    - Read Reg(1) on port 0 , Reg(7) on port 1 and **write 0x03 Reg(4)**
    - Read Reg(2) on port 0 , Reg(3) on port 1
    - Read Reg(4) on port 0 , Reg(5) on port 1
    - Read Reg(6) on port 0 , Reg(0) on port 1 and **write 0x01 Reg(0)**

Assignment:

- Create the same register file using memory arrays instead of DFFs.
- Test your new register file using the same testbench.
- Use Quartus to generate RTL view for both designs to compare between them.

CYCLE#	**Read Port 0**	**Read Port 1**
1	**0**	**0**
2	**FF**	**FF**

3	**FF**	**FF**
4	**FF**	**FF**
5	**FF**	**FF**
6	**11**	**90**
7	**00**	**08**
8	**03**	**00**
9	**00**	**01**