Unsigned Fixed-point Multiplier-Accumulator Design

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***Abstract*—Design and testing of the multiplier accumulator (MAC) for fixed point. MAC unit has recently been used a lot in Digital Signal Processing (DSP) and Neural Network training and inference. The design presented in this paper can be used in both DSP and Neural Network training.**

Keywords—fixed point, multiply accumulate unit, multiplier, adder.

I. Introduction

First of all, I wanted to start by explaining what's a Multiply-Accumulate (MAC) unit, it's has been widely used in recent years in developing both deep neural network training and inference, and in Digital Signal Processing, but we're concentrated more on the neural network part. The proposed MAC unit supports 16 bits MAC operations, sum of two 8 bits multiplications added to 16 bits, sum of four 4 bits multiplication added to 16 bits, sum of eight 2 bits multiplication added to 16 bits.

II. Architecture

A. Multiplier

The multiplier is the module in which the two eight bits or four 4 bits or eight 2 bits gets multiplied. The multiplier takes 3 inputs, the multiplicand, multiplier and the mode. The mode is a 2-bit input that decides whether the multiplier mode, mode 00 being the 8 bits, mode 01 the 4 bits and mode 10 the 2 bits. The multiplier does a normal multiplication when in 8 bits mode, but when it come to the 4 bits and 2 bits mode it has to divide the input relative to the bit size, as they will all be inputted using the two 8 input registers. For example, the 4-bit mode, the multiplier divides the two input registers into two, then multiply the most significant bits to each other and the least significant bits to each other and then adds them together to form the output 16 bits. The multiplier used in this project is a shift and add multiplier, it shifts the bit relative to where in the fixed point it is, if it's before the point it's right shifter if on the other side it's left shifted. This multiplier was used in the project because it is easier to get it to parallel multiply when in the 4-bit mode or the 2-bit mode. After all the shifting are done, they are stored in a register and then the product is just the addition of all elements in the register.

B. Accumulator/Adder

The adder has two input of 16 bits, which are the product of the multiplier and the 16-bit input to the system. The adder then adds the two 16 bits and then rounds the product by looking at the rounding bit, if it is 1 then the number is added by 1, if it is 0 then it is just truncated. Also, the integer part is taken as a whole, to increase precision, the truncation of the result is only from the fraction part of the number. The adder used in this architecture is the Carry Select Adder (CSA), as it is faster than normal 16 bits adder. It uses the Full Adder (FA) in the implementation, it uses 8 FAs as shown in Figure 1. And 5 multiplexers. To make it easier I put each module you see in the figure in a different module and made a submodule that implements a slice of the CSA to be easier to implement in one module. The delay for the CSA is O($\sqrt{n}$).

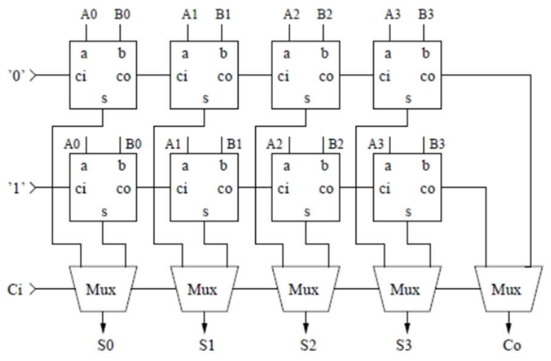


Figure 1: Caryy Save Adder architecture

C. D Flip Flop

The D-Flip Flop (DFF) is used as a pipeline to the architecture, it is used to store the products, they're placed in the beginning to store the inputs, then between the multiplier and the accumulator in order to store the product of the multiplier then in the end in order to store the result.

D. Full Architecture

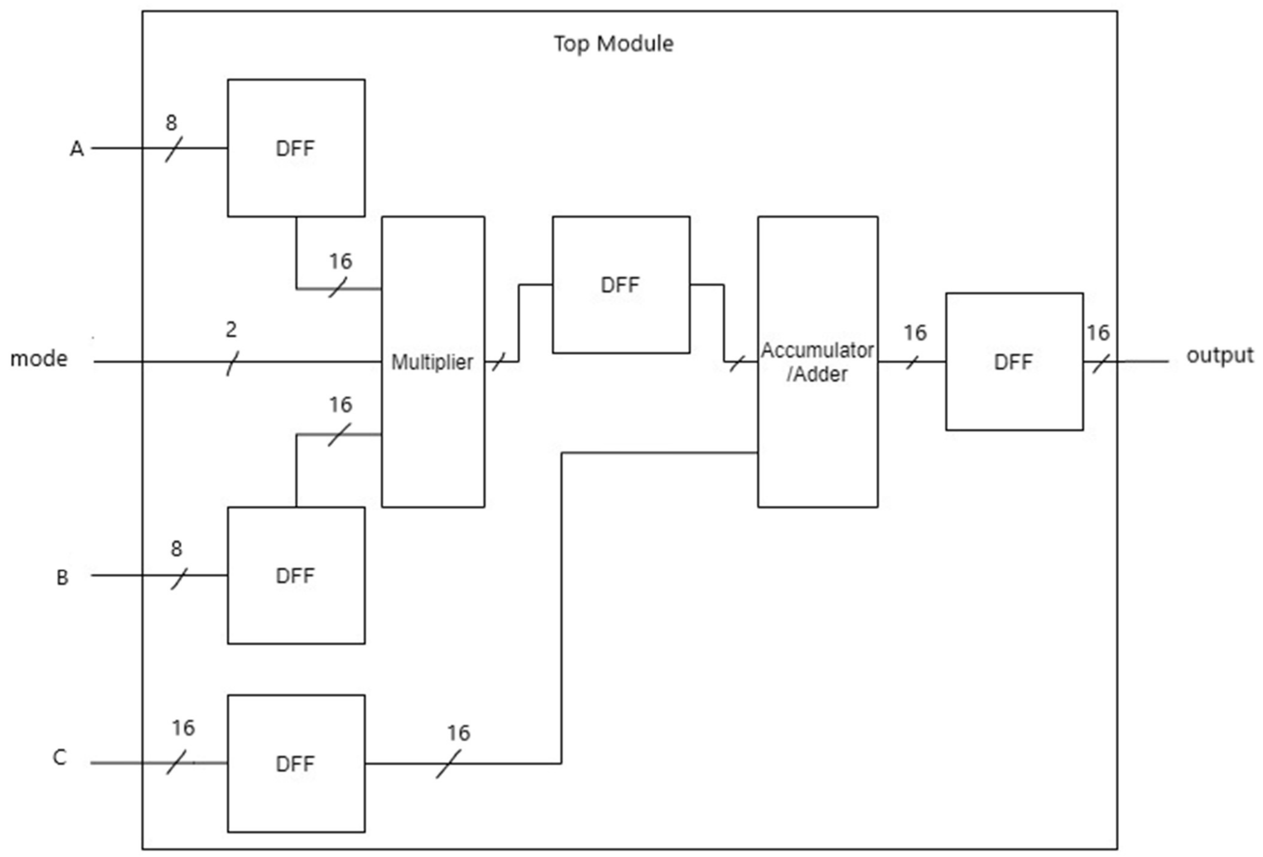


Figure 2: Architecture for MAC

III. Testing and Analysis

A. Testing

Testing the fixed point isn't an easy task as there are no libraries that can handle fixed points so I have to feed the system a string of 0s and 1s that if you do the conversion from binary to fixed point decimal would give the required number. The numbers I fed into the system for the 8-bit mode are

111.1001	7.5625
+	+
101.1011	6.6875
x	x
10100110.10111011	166.7304688
-------------------------	----------------------------
11010001.10111110	209.7421875

This is just an example. You can find all the modes with the input numbers and the related output in figure 3.

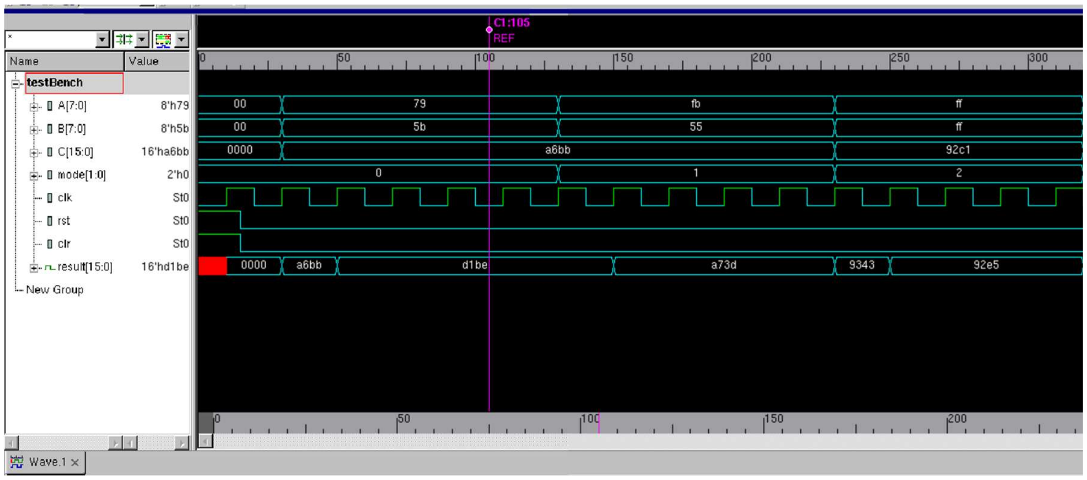
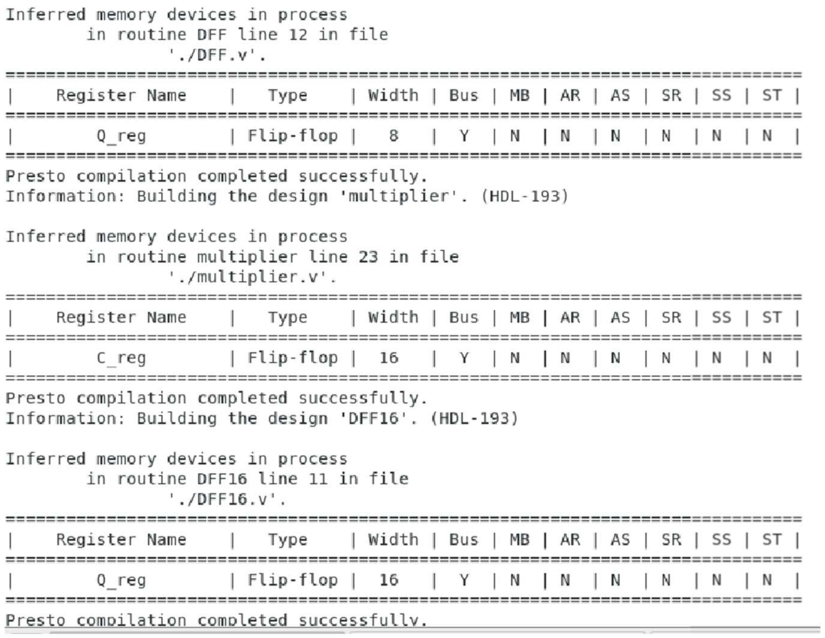


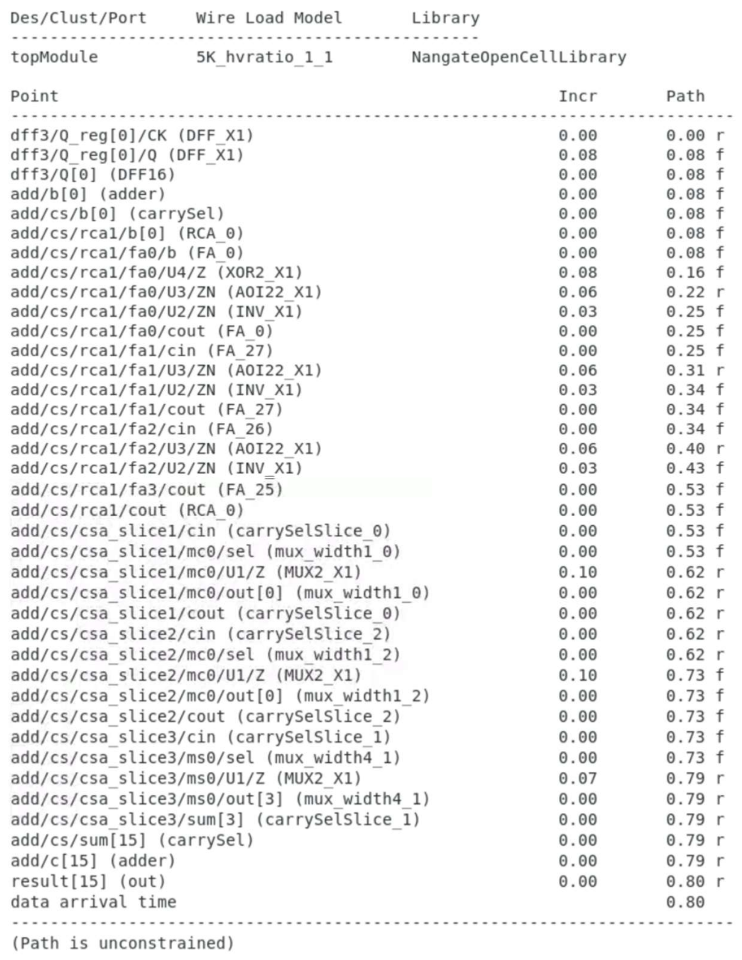
Figure 3: Wave forms for test bench

B. Synthesis and Analysis



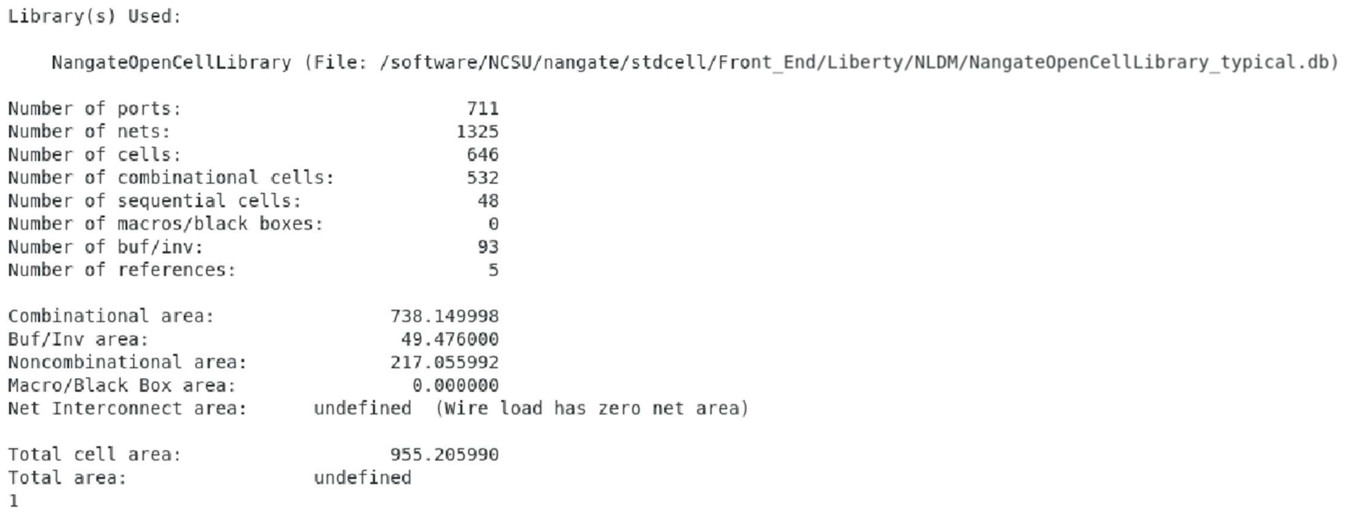
```
Inferred memory devices in process
        in routine DFF line 12 in file
                './DFF.v'.
===============================================================================
|    Register Name    |    Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|        Q_reg        | Flip-flop |   8   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Information: Building the design 'multiplier'. (HDL-193)

Inferred memory devices in process
        in routine multiplier line 23 in file
                './multiplier.v'.
===============================================================================
|    Register Name    |    Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|        C_reg        | Flip-flop |  16   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Information: Building the design 'DFF16'. (HDL-193)

Inferred memory devices in process
        in routine DFF16 line 11 in file
                './DFF16.v'.
===============================================================================
|    Register Name    |    Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|        Q_reg        | Flip-flop |  16   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
```

C. Timing without constrains



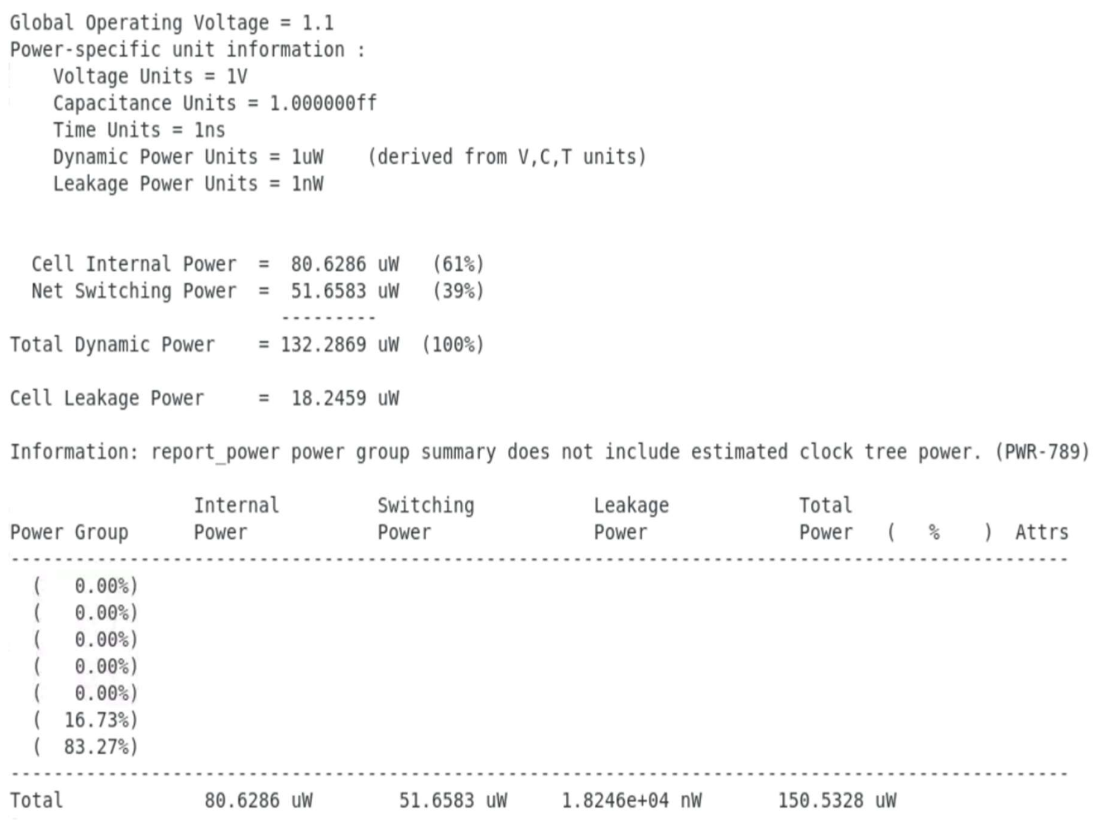
```
Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
topModule          5K_hvratio_1_1        NangateOpenCellLibrary

Point                                                 Incr       Path
------------------------------------------------------------------------
dff3/Q_reg[0]/CK (DFF_X1)                             0.00       0.00 r
dff3/Q_reg[0]/Q (DFF_X1)                              0.08       0.08 f
dff3/Q[0] (DFF16)                                     0.00       0.08 f
add/b[0] (adder)                                      0.00       0.08 f
add/cs/b[0] (carrySel)                                0.00       0.08 f
add/cs/rca1/b[0] (RCA_0)                              0.00       0.08 f
add/cs/rca1/fa0/b (FA_0)                              0.00       0.08 f
add/cs/rca1/fa0/U4/Z (XOR2_X1)                        0.08       0.16 f
add/cs/rca1/fa0/U3/ZN (AOI22_X1)                      0.06       0.22 r
add/cs/rca1/fa0/U2/ZN (INV_X1)                        0.03       0.25 f
add/cs/rca1/fa0/cout (FA_0)                           0.00       0.25 f
add/cs/rca1/fa1/cin (FA_27)                           0.00       0.25 f
add/cs/rca1/fa1/U3/ZN (AOI22_X1)                      0.06       0.31 r
add/cs/rca1/fa1/U2/ZN (INV_X1)                        0.03       0.34 f
add/cs/rca1/fa1/cout (FA_27)                          0.00       0.34 f
add/cs/rca1/fa2/cin (FA_26)                           0.00       0.34 f
add/cs/rca1/fa2/U3/ZN (AOI22_X1)                      0.06       0.40 r
add/cs/rca1/fa2/U2/ZN (INV_X1)                        0.03       0.43 f
add/cs/rca1/fa3/cout (FA_25)                          0.00       0.53 f
add/cs/rca1/cout (RCA_0)                              0.00       0.53 f
add/cs/csa_slice1/cin (carrySelSlice_0)               0.00       0.53 f
add/cs/csa_slice1/mc0/sel (mux_width1_0)              0.00       0.53 f
add/cs/csa_slice1/mc0/U1/Z (MUX2_X1)                  0.10       0.62 r
add/cs/csa_slice1/mc0/out[0] (mux_width1_0)           0.00       0.62 r
add/cs/csa_slice1/cout (carrySelSlice_0)              0.00       0.62 r
add/cs/csa_slice2/cin (carrySelSlice_2)               0.00       0.62 r
add/cs/csa_slice2/mc0/sel (mux_width1_2)              0.00       0.62 r
add/cs/csa_slice2/mc0/U1/Z (MUX2_X1)                  0.10       0.73 f
add/cs/csa_slice2/mc0/out[0] (mux_width1_2)           0.00       0.73 f
add/cs/csa_slice2/cout (carrySelSlice_2)              0.00       0.73 f
add/cs/csa_slice3/cin (carrySelSlice_1)               0.00       0.73 f
add/cs/csa_slice3/ms0/sel (mux_width4_1)              0.00       0.73 f
add/cs/csa_slice3/ms0/U1/Z (MUX2_X1)                  0.07       0.79 r
add/cs/csa_slice3/ms0/out[3] (mux_width4_1)           0.00       0.79 r
add/cs/csa_slice3/sum[3] (carrySelSlice_1)            0.00       0.79 r
add/cs/sum[15] (carrySel)                             0.00       0.79 r
add/c[15] (adder)                                     0.00       0.79 r
result[15] (out)                                      0.00       0.80 r
data arrival time                                                0.80
------------------------------------------------------------------------
(Path is unconstrained)
```

D. *Area without constrains*



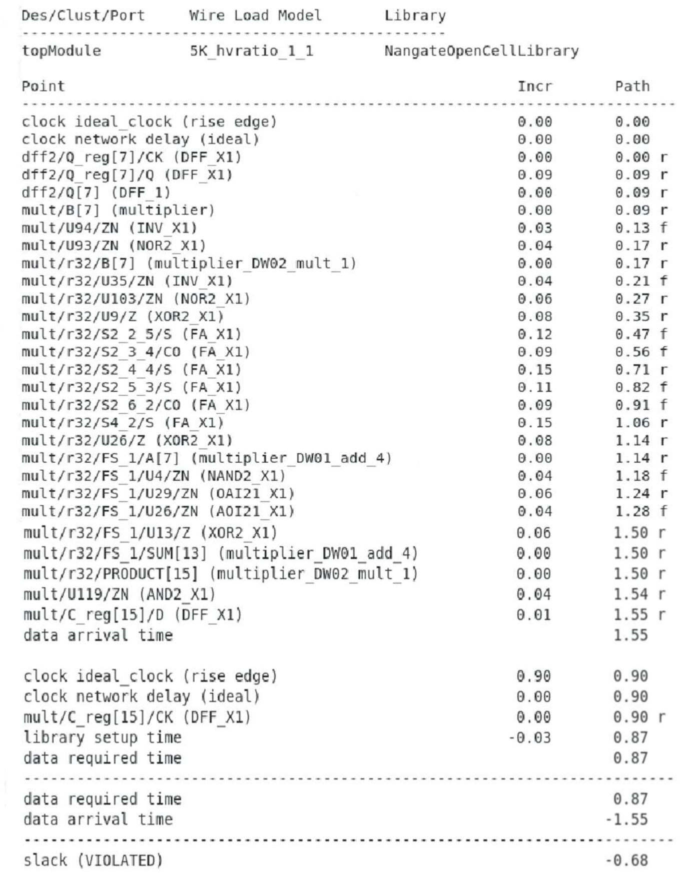
```
Library(s) Used:

    NangateOpenCellLibrary (File: /software/NCSU/nangate/stdcell/Front_End/Liberty/NLDM/NangateOpenCellLibrary_typical.db)

Number of ports:                          711
Number of nets:                          1325
Number of cells:                          646
Number of combinational cells:            532
Number of sequential cells:                48
Number of macros/black boxes:               0
Number of buf/inv:                         93
Number of references:                       5

Combinational area:                738.149998
Buf/Inv area:                       49.476000
Noncombinational area:             217.055992
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                   955.205990
Total area:                 undefined
1
```

E. Power without constrains



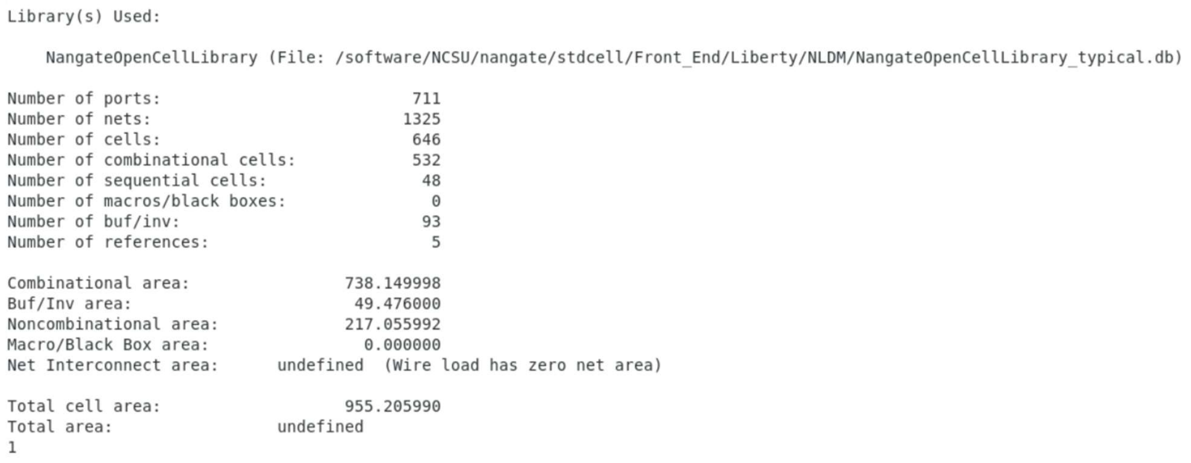
```
Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  80.6286 uW   (61%)
  Net Switching Power  =  51.6583 uW   (39%)
                         ---------
Total Dynamic Power    = 132.2869 uW  (100%)

Cell Leakage Power     =  18.2459 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
  (   0.00%)
  (   0.00%)
  (   0.00%)
  (   0.00%)
  (   0.00%)
  (  16.73%)
  (  83.27%)
--------------------------------------------------------------------------------------------------
Total             80.6286 uW        51.6583 uW     1.8246e+04 nW       150.5328 uW
```

F. Timing without constrains



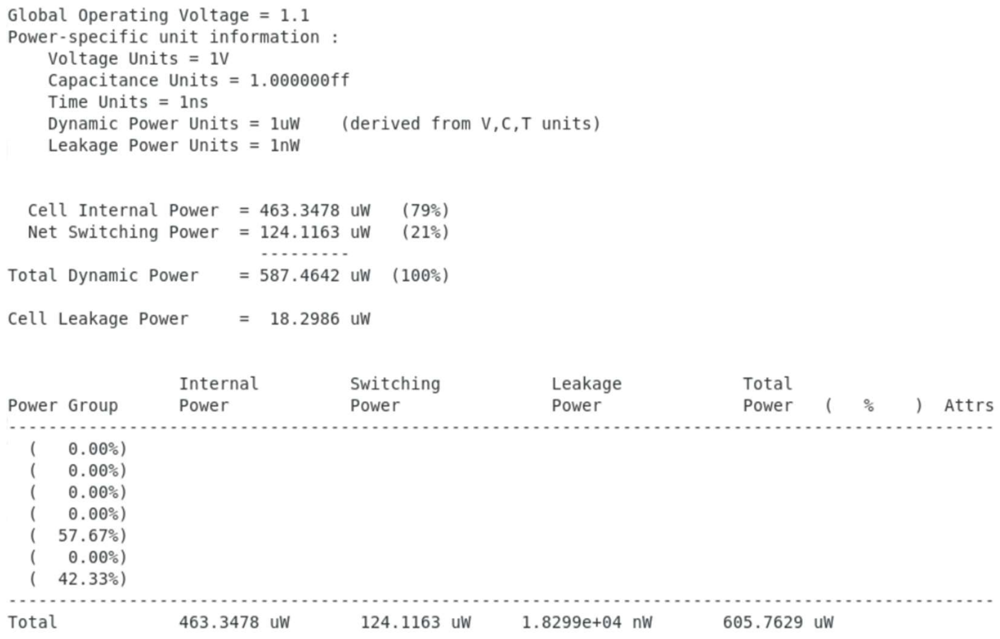
```
Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
topModule          5K_hvratio_1_1        NangateOpenCellLibrary

Point                                                   Incr       Path
---------------------------------------------------------------------------
clock ideal_clock (rise edge)                           0.00       0.00
clock network delay (ideal)                             0.00       0.00
dff2/Q_reg[7]/CK (DFF_X1)                               0.00       0.00 r
dff2/Q_reg[7]/Q (DFF_X1)                                0.09       0.09 r
dff2/Q[7] (DFF_1)                                       0.00       0.09 r
mult/B[7] (multiplier)                                  0.00       0.09 r
mult/U94/ZN (INV_X1)                                    0.03       0.13 f
mult/U93/ZN (NOR2_X1)                                   0.04       0.17 r
mult/r32/B[7] (multiplier_DW02_mult_1)                  0.00       0.17 r
mult/r32/U35/ZN (INV_X1)                                0.04       0.21 f
mult/r32/U103/ZN (NOR2_X1)                              0.06       0.27 r
mult/r32/U9/Z (XOR2_X1)                                 0.08       0.35 r
mult/r32/S2_2_5/S (FA_X1)                               0.12       0.47 f
mult/r32/S2_3_4/CO (FA_X1)                              0.09       0.56 f
mult/r32/S2_4_4/S (FA_X1)                               0.15       0.71 r
mult/r32/S2_5_3/S (FA_X1)                               0.11       0.82 f
mult/r32/S2_6_2/CO (FA_X1)                              0.09       0.91 f
mult/r32/S4_2/S (FA_X1)                                 0.15       1.06 r
mult/r32/U26/Z (XOR2_X1)                                0.08       1.14 r
mult/r32/FS_1/A[7] (multiplier_DW01_add_4)              0.00       1.14 r
mult/r32/FS_1/U4/ZN (NAND2_X1)                          0.04       1.18 f
mult/r32/FS_1/U29/ZN (OAI21_X1)                         0.06       1.24 r
mult/r32/FS_1/U26/ZN (AOI21_X1)                         0.04       1.28 f
mult/r32/FS_1/U13/Z (XOR2_X1)                           0.06       1.50 r
mult/r32/FS_1/SUM[13] (multiplier_DW01_add_4)           0.00       1.50 r
mult/r32/PRODUCT[15] (multiplier_DW02_mult_1)           0.00       1.50 r
mult/U119/ZN (AND2_X1)                                  0.04       1.54 r
mult/C_reg[15]/D (DFF_X1)                               0.01       1.55 r
data arrival time                                                  1.55

clock ideal_clock (rise edge)                           0.90       0.90
clock network delay (ideal)                             0.00       0.90
mult/C_reg[15]/CK (DFF_X1)                              0.00       0.90 r
library setup time                                     -0.03       0.87
data required time                                                 0.87
---------------------------------------------------------------------------
data required time                                                 0.87
data arrival time                                                 -1.55
---------------------------------------------------------------------------
slack (VIOLATED)                                                  -0.68
```

G. Area constrained



```
Library(s) Used:

    NangateOpenCellLibrary (File: /software/NCSU/nangate/stdcell/Front_End/Liberty/NLDM/NangateOpenCellLibrary_typical.db)

Number of ports:                          711
Number of nets:                          1325
Number of cells:                          646
Number of combinational cells:            532
Number of sequential cells:                48
Number of macros/black boxes:               0
Number of buf/inv:                         93
Number of references:                       5

Combinational area:                738.149998
Buf/Inv area:                       49.476000
Noncombinational area:             217.055992
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                   955.205990
Total area:                 undefined
1
```

H. Power constrained



```
Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 463.3478 uW   (79%)
  Net Switching Power  = 124.1163 uW   (21%)
                         ---------
Total Dynamic Power    = 587.4642 uW  (100%)

Cell Leakage Power     =  18.2986 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
  (   0.00%)
  (   0.00%)
  (   0.00%)
  (   0.00%)
  (  57.67%)
  (   0.00%)
  (  42.33%)
--------------------------------------------------------------------------------------------------
Total            463.3478 uW       124.1163 uW     1.8299e+04 nW       605.7629 uW
```

I. Results summerized

Timing before constrains: 0.80 ns

After constrains: 0.87 ns

Area before constrains: 894.82 µm²

After constrains: 955.21 µm²

Power before constrains: 150.53 µW

After constrains: 605.76 µW

CONCLUSION

This project was really informative, it showed me how to actually research and implement what I read about. The architecture can be further modified, by tuning the multiplier into a faster multiplier with less area and more fixed-point precision. Making all the variable dynamic so that it could be easily changed and manipulated in order to support more functions. All in all, I am proud of this implementation as the Area and power are nearly half that of the AI paper I presented, and the timing is the only factor that could've been improved further.