

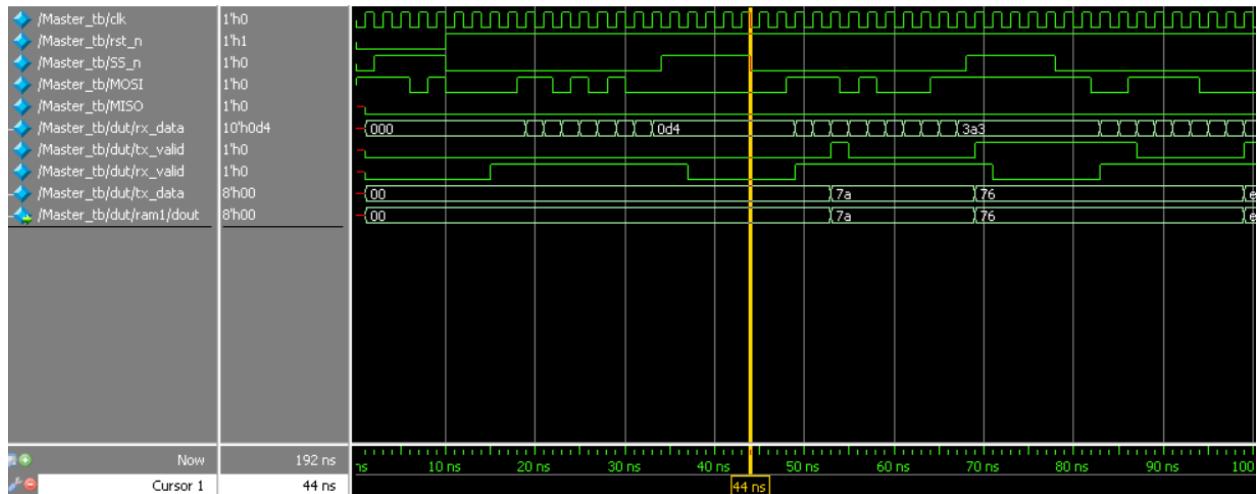
Project 2

SPI

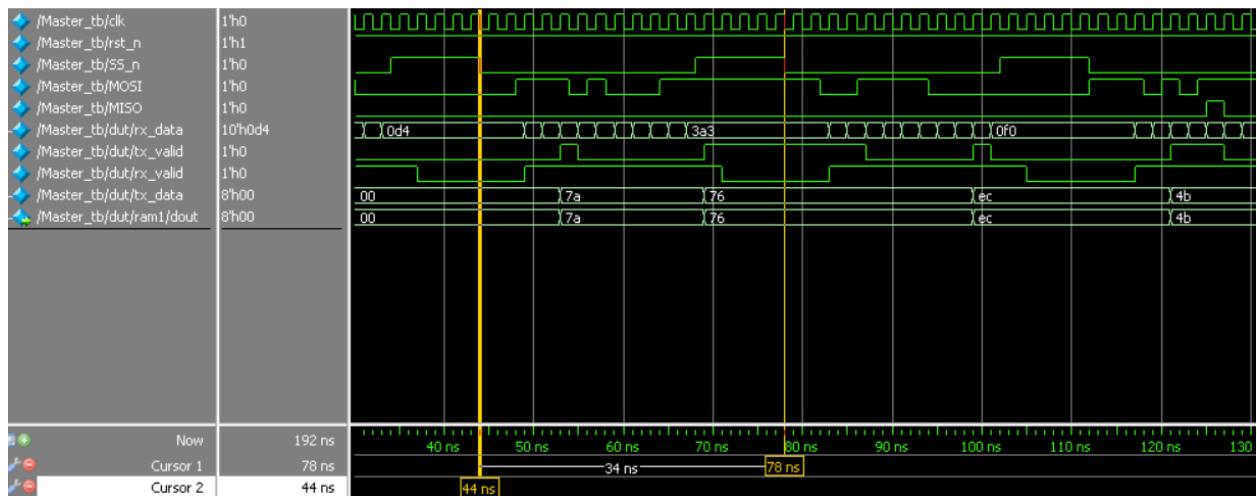
Maryam Ahmed Kamal
Maryam Hossam Abd El-Ghaffar
Yasmin Hany Momtaz Abo El-Magd

Snippets from the waveform

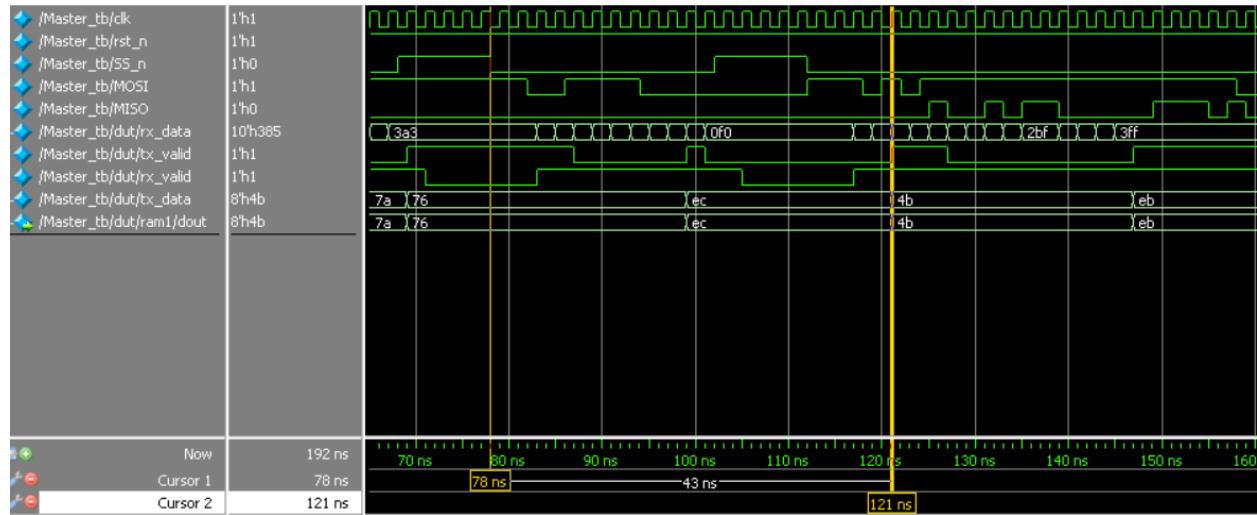
- Determine write address



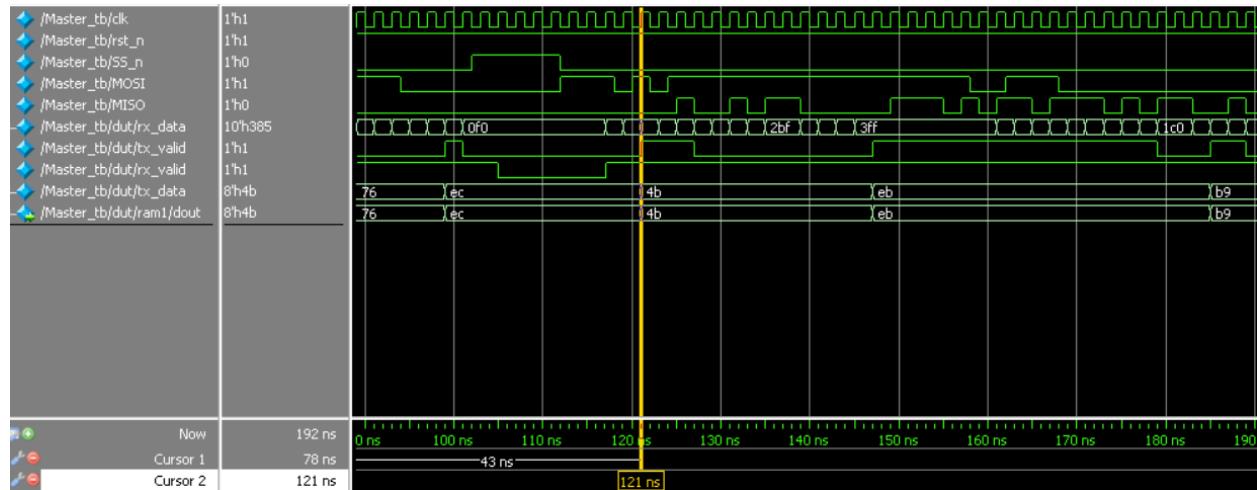
- Write in memory



- Determine read address

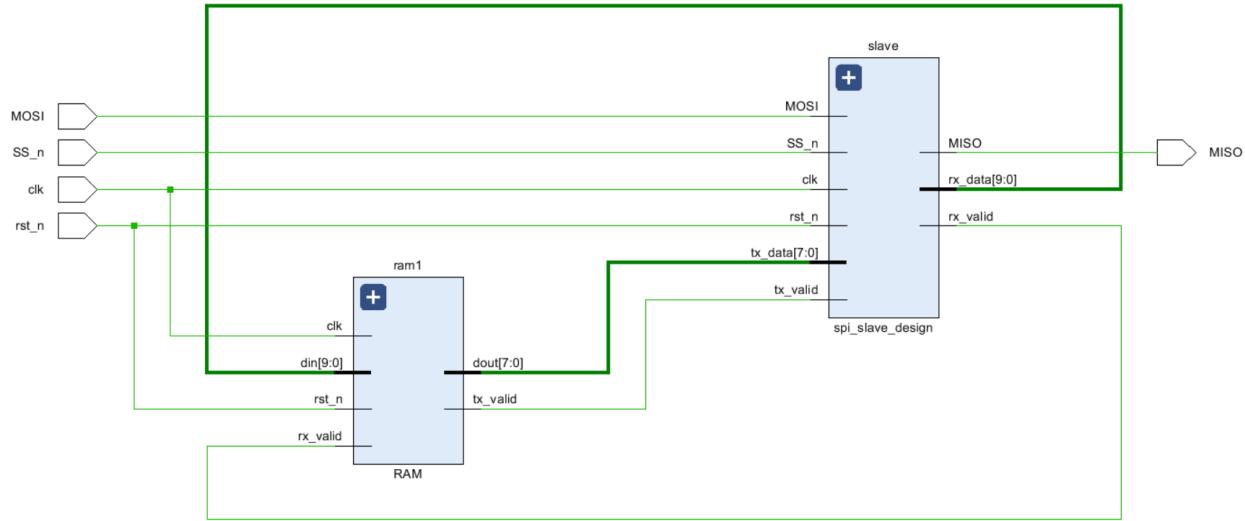


- Read from memory

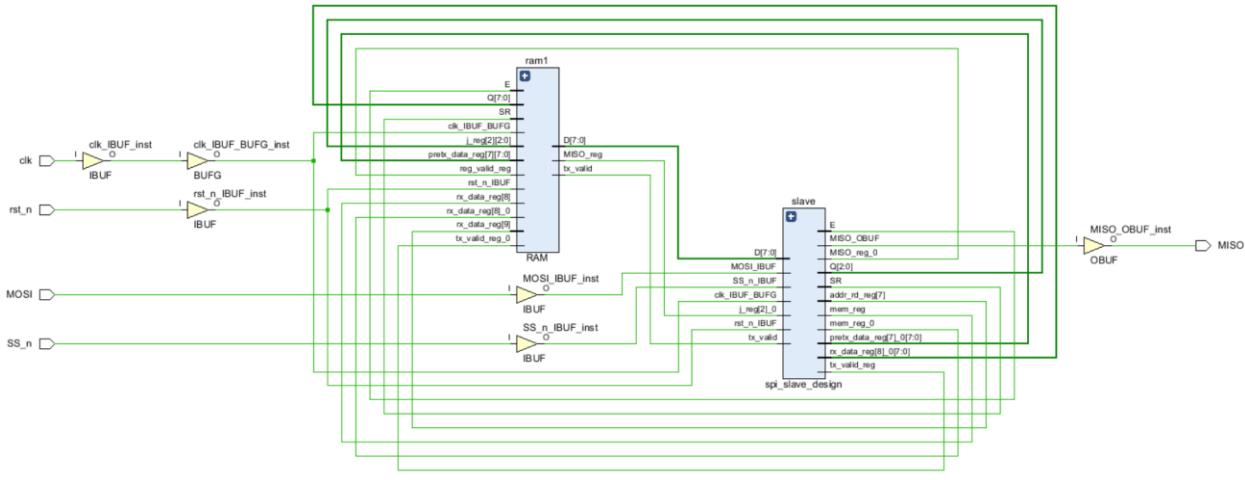


• Sequential encoding

Schematic after Elaboration



Schematic after synthesis



Synthesis report showing the used encoding

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_DATA	01000	100
READ_ADD	10000	011

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave_design'
 WARNING: [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [E:/Diploma/SPI/MYM_Project2/SPI.v:33]
 WARNING: [Synth 8-327] inferring latch for variable 'memorize_addr_reg' [E:/Diploma/SPI/MYM_Project2/SPI.v:44]

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:32 ; elapsed = 00:00:34 . Memory (MB): peak = 766.086 ; gain = 508.910

Timing report after synthesis

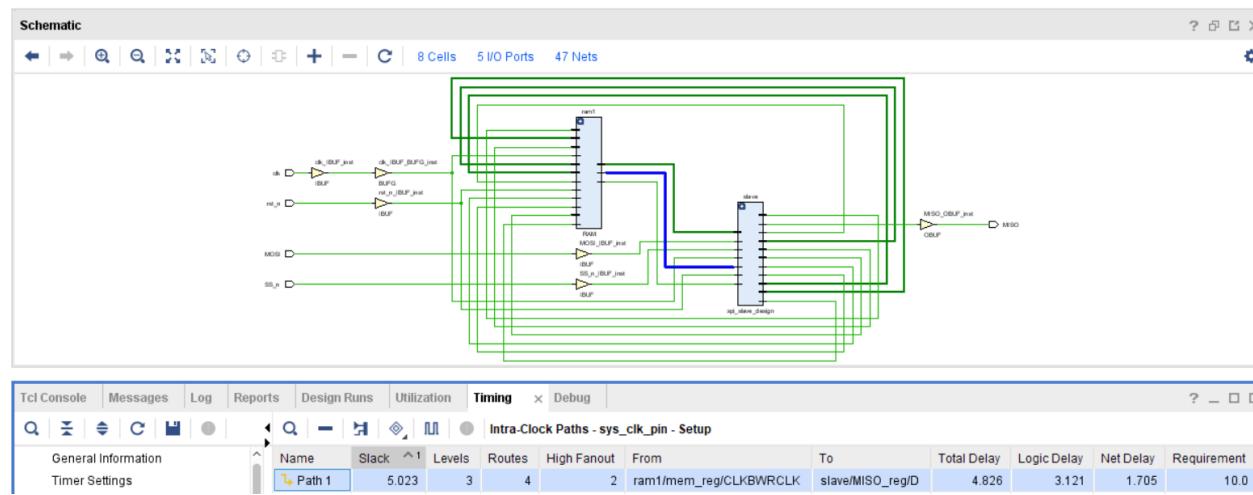


The screenshot shows the Xilinx Vivado interface with the 'Timing' tab selected. The 'Design Timing Summary' section is displayed, showing the following data:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.023 ns	Worst Hold Slack (WHS): 0.139 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 258	Total Number of Endpoints: 258	Total Number of Endpoints: 110

All user specified timing constraints are met.

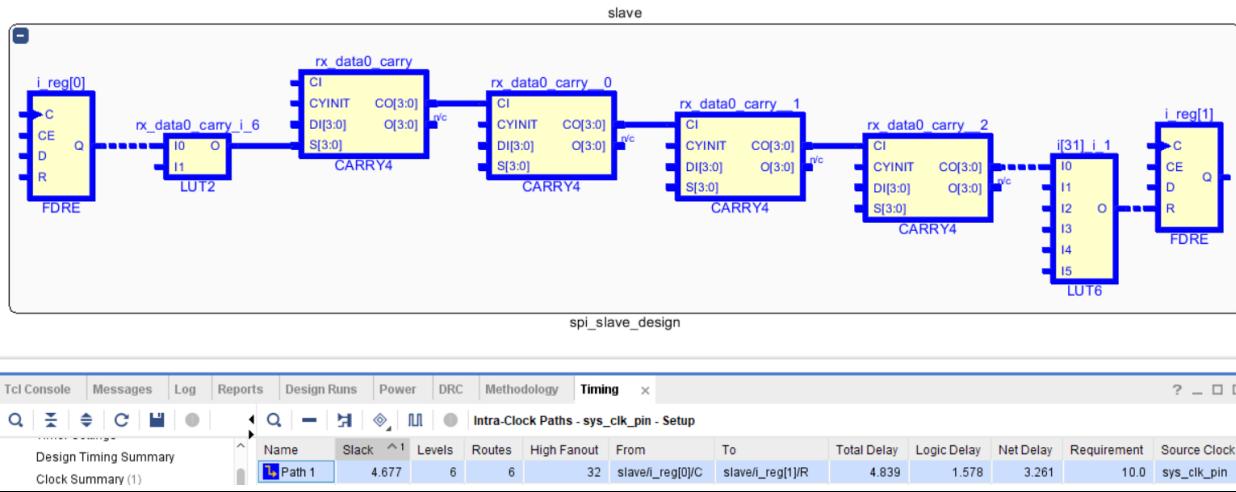
Critical path for synthesis



The screenshot shows the Xilinx Vivado interface with the 'Timing' tab selected. The 'Intra-Clock Paths - sys_clk_pin - Setup' report is displayed, showing the following data:

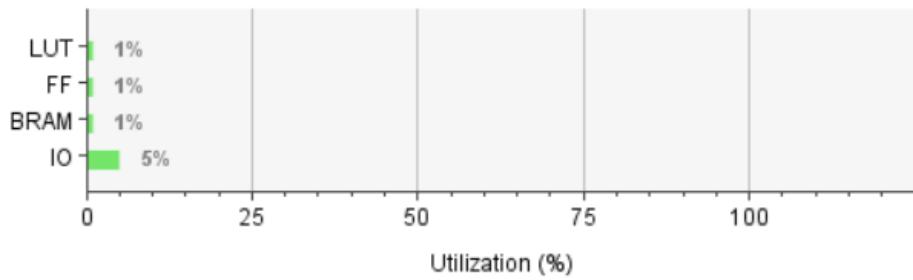
Name	Slack	^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	5.023		3	4	2	ram1/mem_reg/CLKBWRCLK	slave/MISO_reg/D	4.826	3.121	1.705	10.0

Critical path for implementation



Utilization report

Resource	Utilization	Available	Utilization %
LUT	107	20800	0.51
FF	113	41600	0.27
BRAM	0.50	50	1.00
IO	5	106	4.72

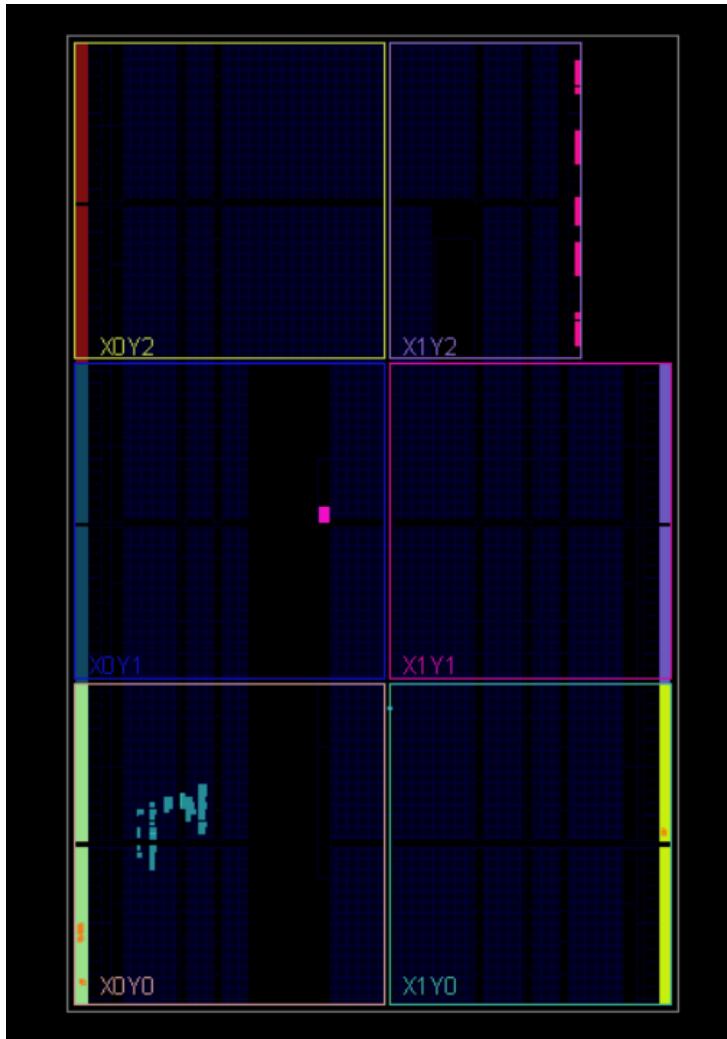


Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
interface		107	113	2	0.5	5	1
ram1 (RAM)		9	17	2	0.5	0	0
slave (spi_slave_desi...)		98	96	0	0	0	0

Timing report after implementation



FPGA device



Messages tab for Synthesis

Tcl Console **Messages** x Log Reports Design Runs Utilization Timing Debug

Search:

Q | X | D | T | E | B | Warning (15) Info (283) Status (503) Show All

> Vivado Commands (3 infos)

< Elaborated Design (5 warnings, 14 infos)

< General Messages (5 warnings, 14 infos)

> [Synth 8-6157] synthesizing module 'interface' [[Interface.v:1](#)] (2 more like this)

< [Synth 8-155] case statement is not full and has no default [[SPI.v:30](#)]

< [Synth 8-567] referenced signal 'T' should be on the sensitivity list [[SPI.v:29](#)]

> [Synth 8-6090] variable 'T' is written by both blocking and non-blocking assignments, entire logic could be removed [[SPI.v:96](#)] (3 more like this)

> [Synth 8-6155] done synthesizing module 'spi_slave_design' (1#1) [[SPI.v:1](#)] (2 more like this)

< [Project 1-570] Preparing netlist for logic optimization

< [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

< [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

> [Timing 38-253] The multi-corner and the min_max analysis have been enable for the timing DRC (1 more like this)

> [DRC 23-133] Running Methodology with 2 threads (1 more like this)

> Synthesis (10 warnings, 36 infos)

< Synthesized Design (19 infos)

< General Messages (19 infos)

< [Netlist 29-17] Analyzing 38 Unisim elements for replacement

< [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

< [Project 1-479] Netlist was created with Vivado 2018.2

< [Project 1-570] Preparing netlist for logic optimization

< [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

< [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

< [Timing 38-35] Done setting XDC timing constraints.

< [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.

< [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

> [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max. (4 more like this)

> [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (4 more like this)

> Implementation (99 infos)

< Implemented Design (17 infos)

< General Messages (17 infos)

< [Netlist 29-17] Analyzing 38 Unisim elements for replacement

< [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

< [Project 1-479] Netlist was created with Vivado 2018.2

< [Project 1-570] Preparing netlist for logic optimization

< [Timing 38-478] Restoring timing data from binary archive.

< [Timing 38-479] Binary timing data restore complete.

< [Project 1-856] Restoring constraints from binary archive.

< [Project 1-853] Binary constraint restore complete.

< [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

> [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max. (3 more like this)

> [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (3 more like this)

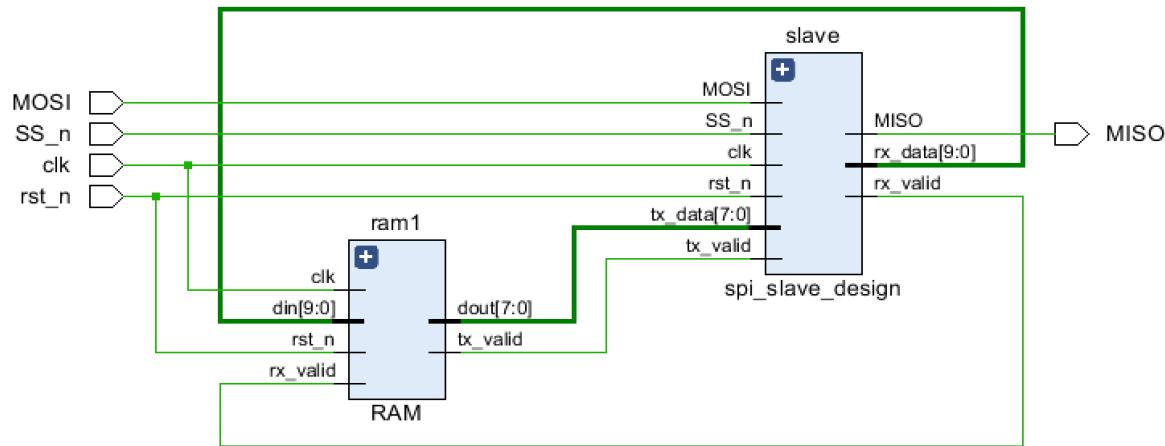
Messages tab for Implementation

- > Vivado Commands (3 infos)
 - > Elaborated Design (5 warnings, 12 infos)
 - > Synthesis (10 warnings, 36 infos)
 - > Synthesized Design (17 infos)
 - > General Messages (17 infos)
 - i* [Netlist 29-17] Analyzing 38 Unisim elements for replacement
 - i* [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - i* [Project 1-479] Netlist was created with Vivado 2018.2
 - i* [Project 1-570] Preparing netlist for logic optimization
 - i* [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - i* [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
 - i* [Timing 38-35] Done setting XDC timing constraints.
 - i* [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
 - i* [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
 - > *i* [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max. (3 more like this)
 - > *i* [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (3 more like this)
-

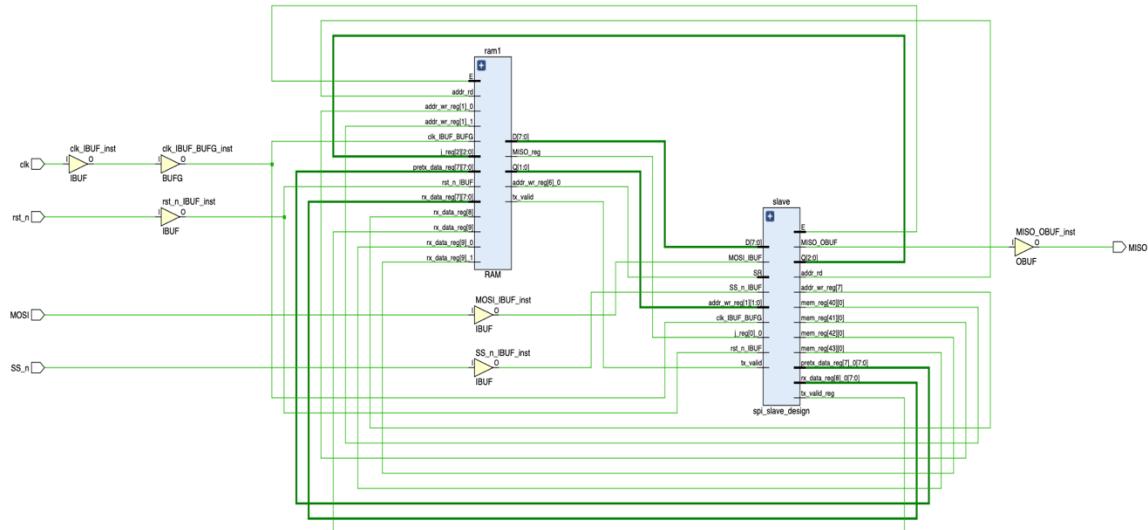
- > Implementation (99 infos)
 - > Implemented Design (17 infos)
 - > General Messages (17 infos)
 - i* [Netlist 29-17] Analyzing 38 Unisim elements for replacement
 - i* [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - i* [Project 1-479] Netlist was created with Vivado 2018.2
 - i* [Project 1-570] Preparing netlist for logic optimization
 - i* [Timing 38-478] Restoring timing data from binary archive.
 - i* [Timing 38-479] Binary timing data restore complete.
 - i* [Project 1-856] Restoring constraints from binary archive.
 - i* [Project 1-853] Binary constraint restore complete.
 - i* [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
 - > *i* [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max. (3 more like this)
 - > *i* [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (3 more like this)
-

• Gray encoding

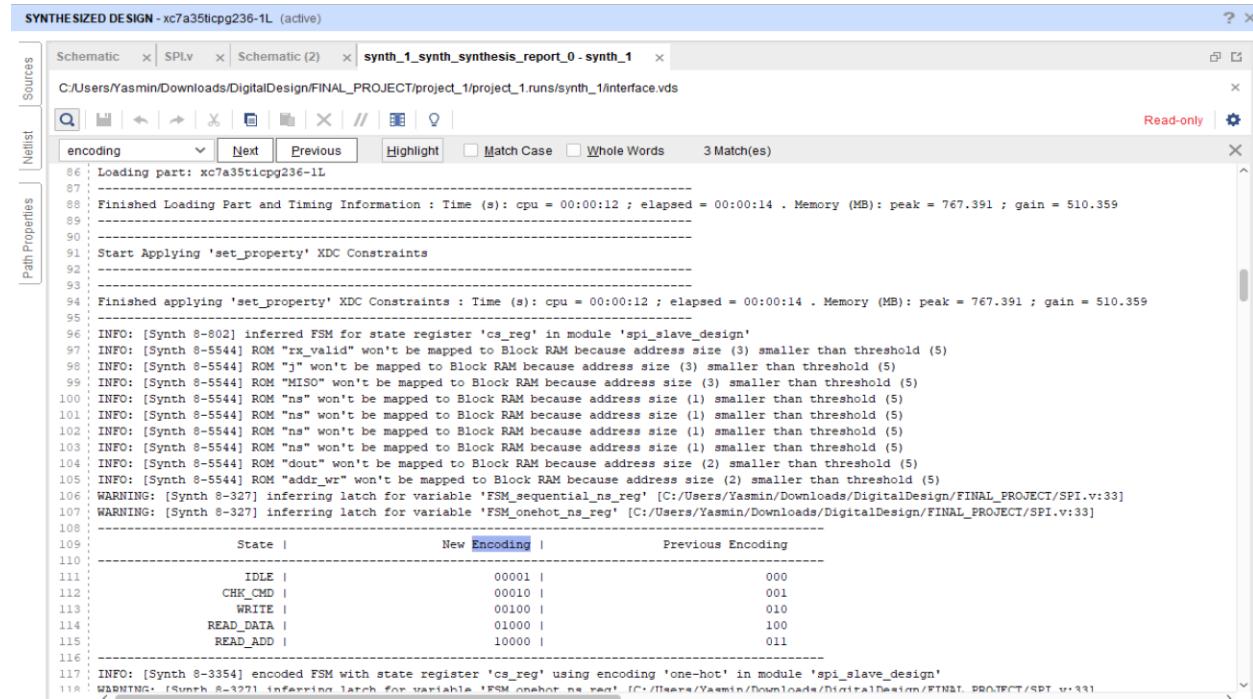
Schematic after Elaboration



Schematic after synthesis



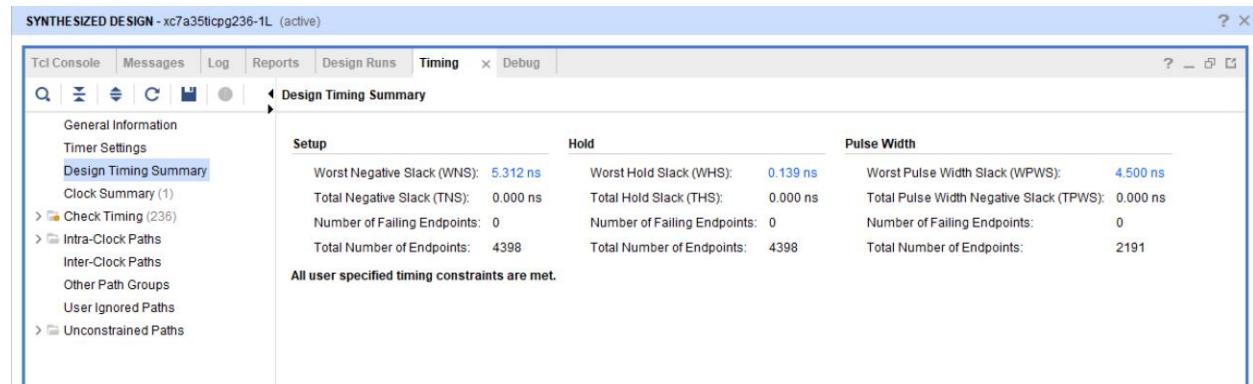
Synthesis report showing the used encoding



The screenshot shows a synthesis report window titled "SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)". The search bar at the top contains the text "encoding". The report lists various synthesis messages and a table of state encodings.

```
SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)
Schematic × SPLv × Schematic (2) × synth_1_synth_synthesis_report_0 - synth_1 ×
C:/Users/Yasmin/Downloads/DigitalDesign/FINAL_PROJECT/project_1/project_1.runs/synth_1/interface.vds
Sources × Neリスト × Path Properties ×
encoding Next Previous Highlight Match Case Whole Words 3 Match(es) Read-only ×
86 : Loading part: xc7a35ticpg236-1L
87 -----
88 : Finished Loading Part and Timing Information : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 767.391 ; gain = 510.359
89 -----
90 -----
91 : Start Applying 'set_property' XDC Constraints
92 -----
93 -----
94 : Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 767.391 ; gain = 510.359
95 -----
96 : INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'spi_slave_design'
97 : INFO: [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
98 : INFO: [Synth 8-5544] ROM "j" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
99 : INFO: [Synth 8-5544] ROM "MISO" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
100 : INFO: [Synth 8-5544] ROM "na" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
101 : INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
102 : INFO: [Synth 8-5544] ROM "nq" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
103 : INFO: [Synth 8-5544] ROM "nq" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
104 : INFO: [Synth 8-5544] ROM "dout" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
105 : INFO: [Synth 8-5544] ROM "addr_wr" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
106 : WARNING: [Synth 8-327] inferring latch for variable 'FSM_sequential_ns_reg' [C:/Users/Yasmin/Downloads/DigitalDesign/FINAL_PROJECT/SPI.v:33]
107 : WARNING: [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_Reg' [C:/Users/Yasmin/Downloads/DigitalDesign/FINAL_PROJECT/SPI.v:33]
108 -----
109 State | New Encoding | Previous Encoding
110 -----
111 IDLE | 00001 | 000
112 CHK_CMD | 00010 | 001
113 WRITE | 00100 | 010
114 READ_DATA | 01000 | 100
115 READ_ADD | 10000 | 011
116 -----
117 : INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave_design'
118 : WARNING: [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_Reg' [C:/Users/Yasmin/Downloads/DigitalDesign/FINAL_PROJECT/SPI.v:33]
```

Timing report after synthesis

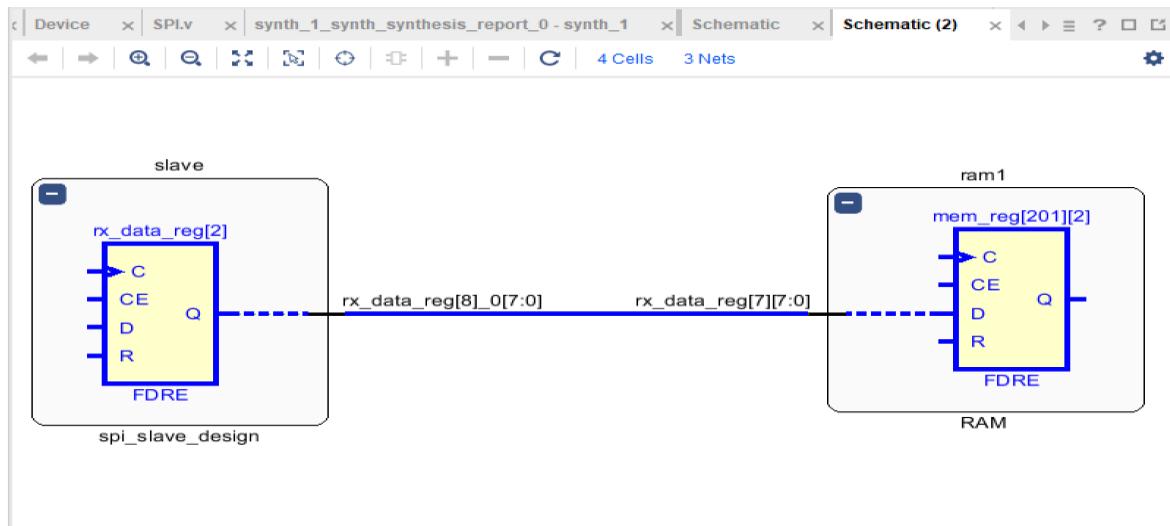
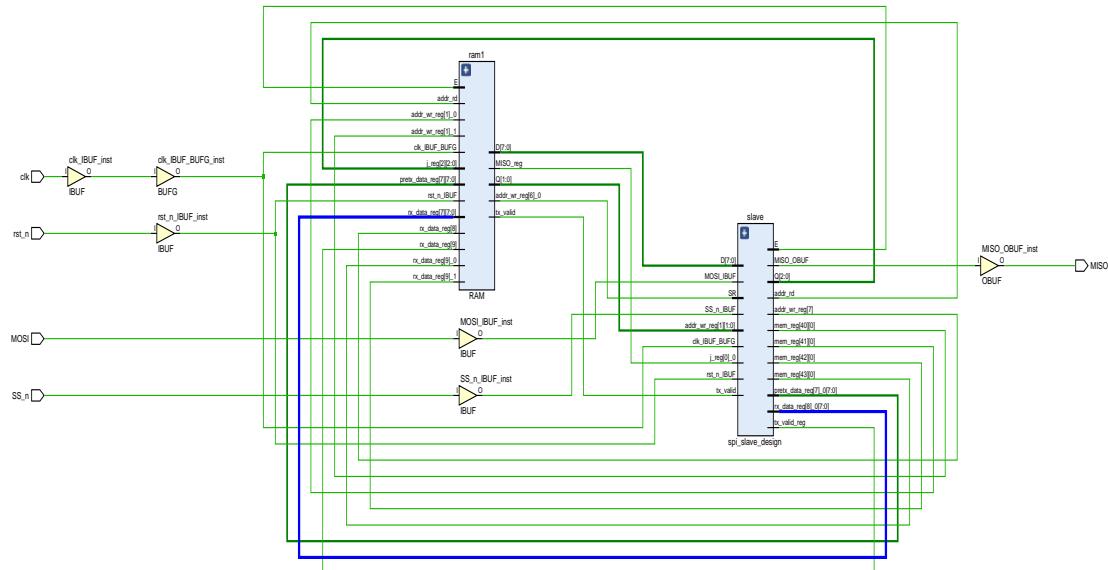


The screenshot shows a timing report window titled "SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)". The "Timing" tab is selected. The left sidebar shows a tree view of timing analysis categories. The main panel displays the "Design Timing Summary" table.

Design Timing Summary					
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.312 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4398	Total Number of Endpoints:	4398	Total Number of Endpoints:	2191

All user specified timing constraints are met.

Critical path for implementation



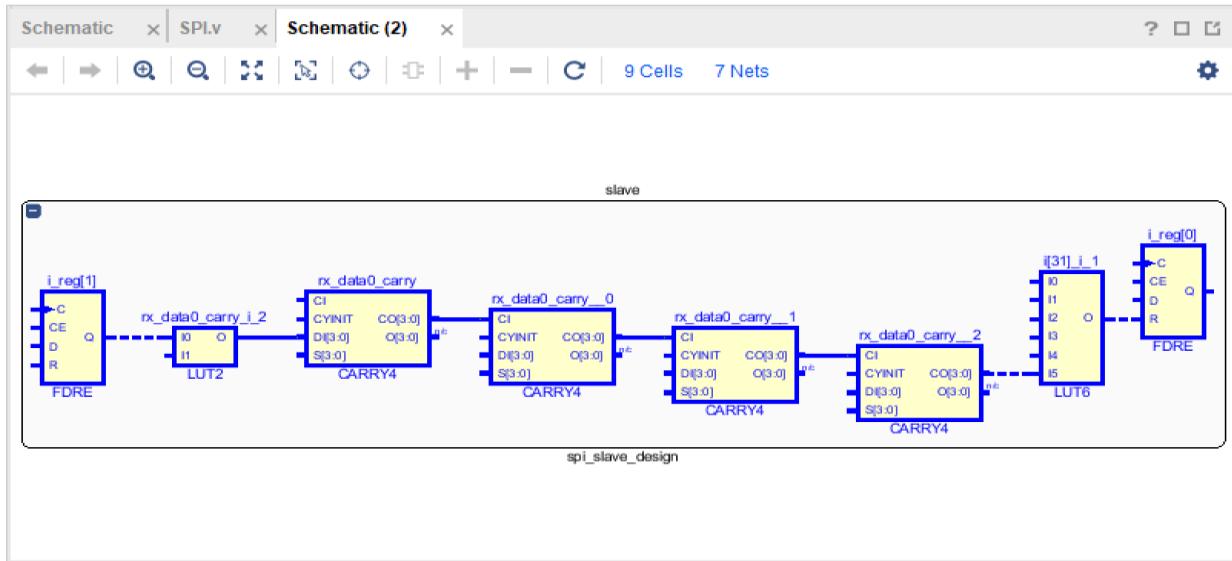
Critical path for synthesis

SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)

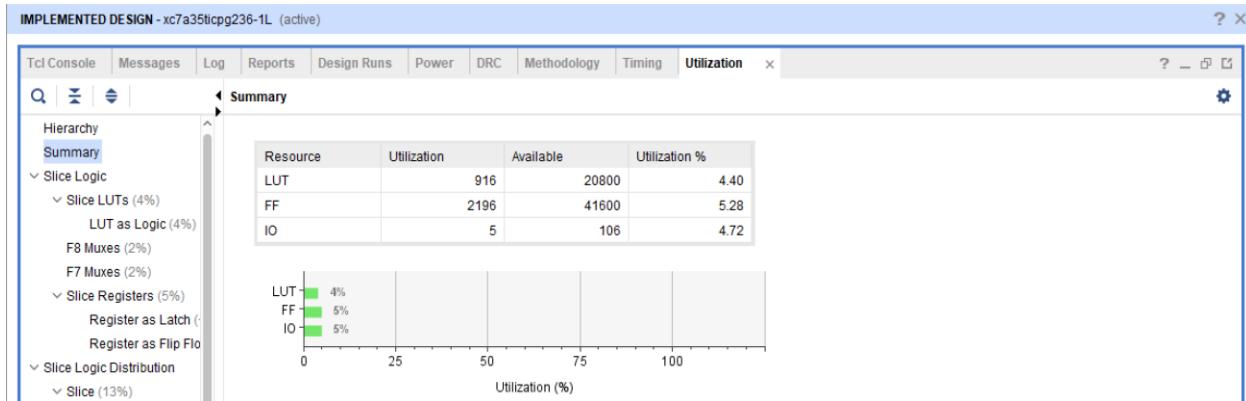
Tcl Console | Messages | Log | Reports | Design Runs | **Timing** | Debug

Intra-Clock Paths - sys_clk_pin - Setup

General Ir	Name	Slack	^ 1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Timer Set	Path 1	5.312		6	7	32	slave/i_reg[1]/C	slave/i_reg[0]/R	4.075	1.796	2.279	10.0	sys_clk_pin	sys_clk_pin
Design Ti	Path 2	5.312		6	7	32	slave/i_reg[1]/C	slave/i_reg[10]/R	4.075	1.796	2.279	10.0	sys_clk_pin	sys_clk_pin
Clock Sur	Path 3	5.312		6	7	32	slave/i_reg[1]/C	slave/i_reg[11]/R	4.075	1.796	2.279	10.0	sys_clk_pin	sys_clk_pin
> Check Tin	Path 4	5.312		6	7	32	slave/i_reg[1]/C	slave/i_reg[12]/R	4.075	1.796	2.279	10.0	sys_clk_pin	sys_clk_pin
Intra-Cloc	Path 5	5.312		6	7	32	slave/i_reg[1]/C	slave/i_reg[13]/R	4.075	1.796	2.279	10.0	sys_clk_pin	sys_clk_pin
sys_c	Path 6	5.312		6	7	32	slave/i_reg[1]/C	slave/i_reg[14]/R	4.075	1.796	2.279	10.0	sys_clk_pin	sys_clk_pin
St	Path 7	5.312		6	7	32	slave/i_reg[1]/C	slave/i_reg[15]/R	4.075	1.796	2.279	10.0	sys_clk_pin	sys_clk_pin
Hc	Path 8	5.312		6	7	32	slave/i_reg[1]/C	slave/i_reg[16]/R	4.075	1.796	2.279	10.0	sys_clk_pin	sys_clk_pin
Pt	Path 9	5.312		6	7	32	slave/i_reg[1]/C	slave/i_reg[17]/R	4.075	1.796	2.279	10.0	sys_clk_pin	sys_clk_pin
Inter-Cloc	Path 10	5.312		6	7	32	slave/i_reg[1]/C	slave/i_reg[18]/R	4.075	1.796	2.279	10.0	sys_clk_pin	sys_clk_pin
Other Path														
User Ignor														
> Unconstr														



Utilization report



IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Utilization										
Hierarchy	Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
Summary										
Slice Logic										
Slice LUTs (4%)		916	2196	274	136	1096	916	34	5	1
LUT as Logic (4%)	ram1 (RAM)	815	2100	273	136	1057	815	9	0	0
F8 Muxes (2%)	slave (spi_slave_desi...	101	96	1	0	56	101	21	0	0
F7 Muxes (2%)										

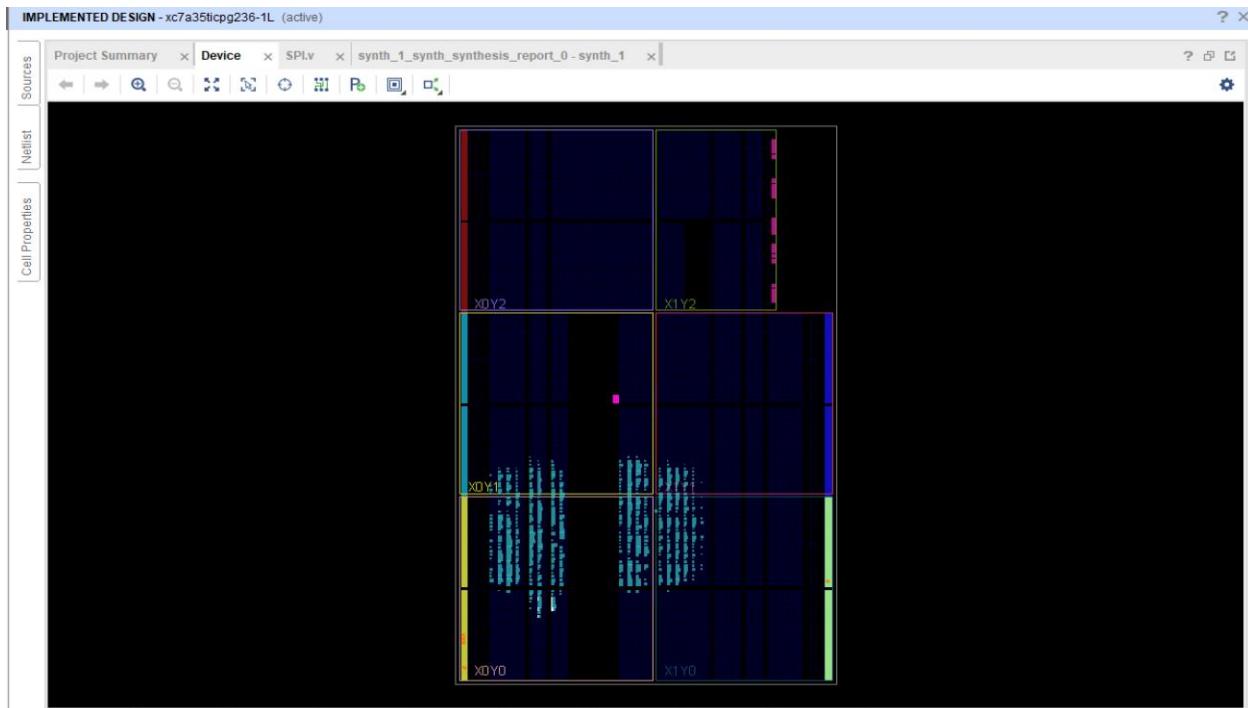
Timing report after implementation

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

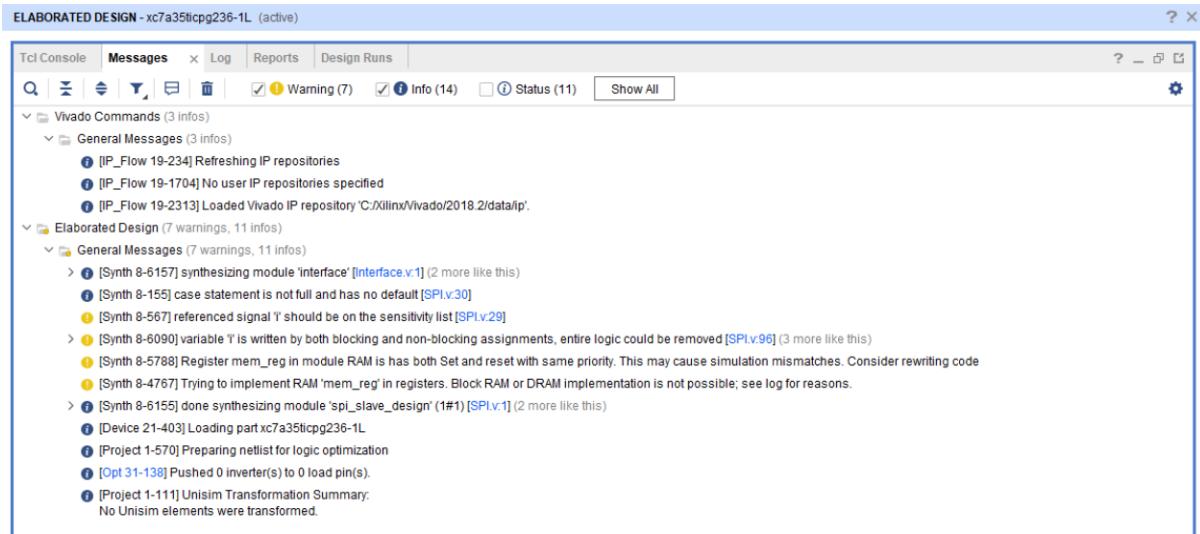
Design Timing Summary		
General Information	Setup	Hold
	Worst Negative Slack (WNS): 0.697 ns	Worst Hold Slack (WHS): 0.199 ns
Timer Settings	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns
Design Timing Summary	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Clock Summary (1)	Total Number of Endpoints: 4398	Total Number of Endpoints: 4398
Check Timing (236)		
Intra-Clock Paths		
Inter-Clock Paths		
Other Path Groups		
User Ignored Paths		
Unconstrained Paths		

All user specified timing constraints are met.

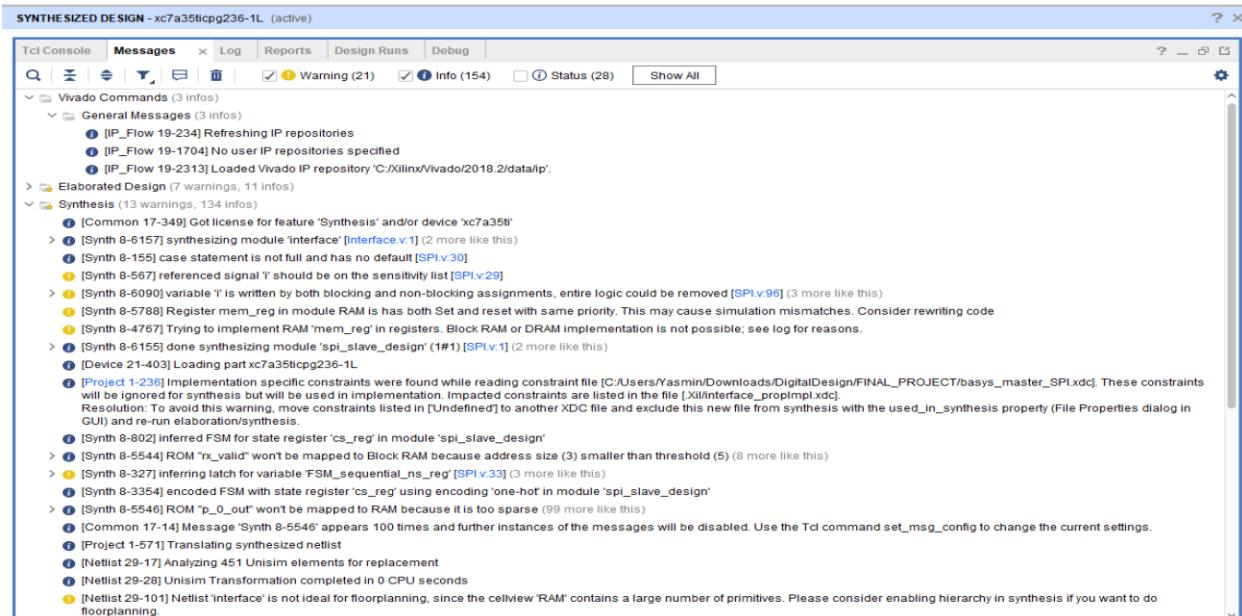
FPGA device



Messages tab for Elaboration



Messages tab for Synthesis



```

> ⓘ [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
> ⓘ [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed. (1 more like this)
  ⓘ [Common 17-83] Releasing license: Synthesis
  ⓘ [Constraints 18-5210] No constraint will be written out.
  ⓘ [Common 17-1381] The checkpoint 'C:/Users/Yasmin/Downloads/DigitalDesign/FINAL_PROJECT/project_1/project_1.runs/synth_1/interface.dcp' has been generated.
  ⓘ [runtcl-4] Executing : report_utilization -file interface_utilization_rpt.rpt -pb interface_utilization_synth.pb
  ⓘ [Common 17-206] Exiting Vivado at Tue Mar 12 17:23:17 2024...
  ⓘ [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed.

  ⓘ [Synthesized Design (1 warning, 6 infos)]
    ⓘ General Messages (1 warning, 6 infos)
      ⓘ [Netlist 29-17] Analyzing 445 Unisim elements for replacement
      ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
      ⓘ [Netlist 29-101] Netlist 'interface' is not ideal for floorplanning, since the celview 'RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
      ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
      ⓘ [Project 1-570] Preparing netlist for logic optimization
      ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
      ⓘ [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.

```

Messages tab for Implementation

IMPLEMENTED DESIGN - xc7a35tci236-1L (active)

Vivado Commands (3 infos)

- General Messages (3 infos)
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'

Elaborated Design (7 warnings, 11 infos)

Synthesis (13 warnings, 134 infos)

Synthesized Design (1 warning, 10 infos)

Implementation (1 warning, 90 infos)

- Design Initialization (1 warning, 11 infos)
 - [Netlist 29-17] Analyzing 445 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Netlist 29-101] Netlist 'interface' is not ideal for floorplanning, since the celview 'RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a35tci236-1L
 - [Project 1-570] Preparing netlist for logic optimization
 - [Timing 38-478] Restoring timing data from binary archive.
 - [Timing 38-479] Binary timing data restore complete.
 - [Project 1-856] Restoring constraints from binary archive.
 - [Project 1-853] Binary constraint restore complete.
 - [Project 1-111] Unisim Transformation Summary:
 - No Unisim elements were transformed.
 - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
- Opt Design (23 infos)
- Place Design (21 infos)
- Route Design (35 infos)

Implemented Design (1 warning, 11 infos)

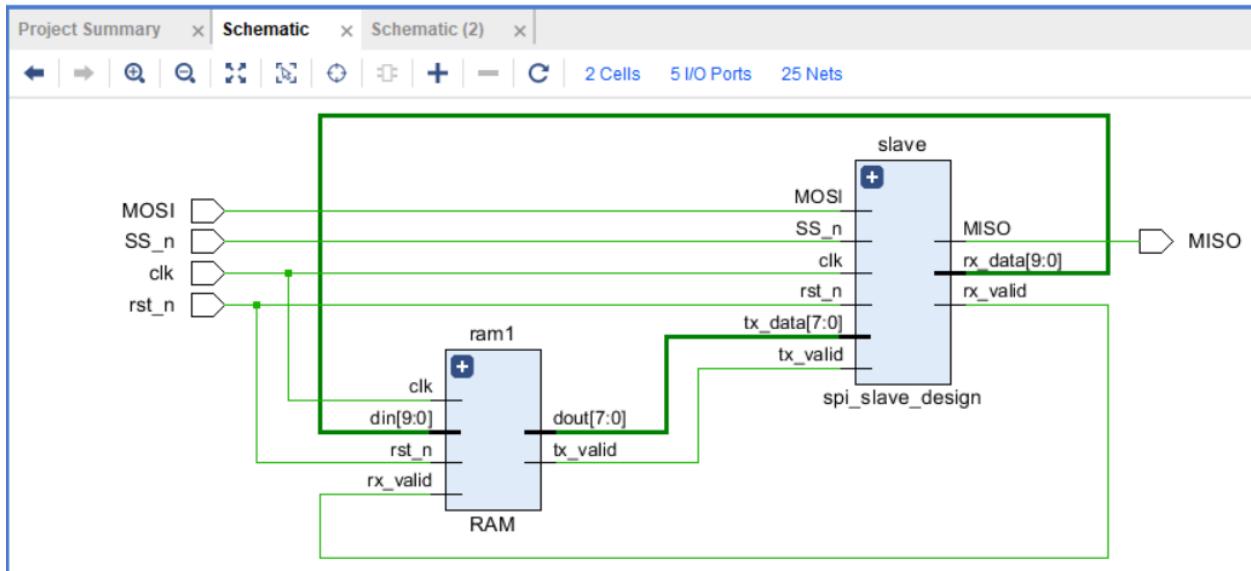
- General Messages (1 warning, 11 infos)
 - [Netlist 29-17] Analyzing 445 Unisim elements for replacement

Implemented Design (1 warning, 11 infos)

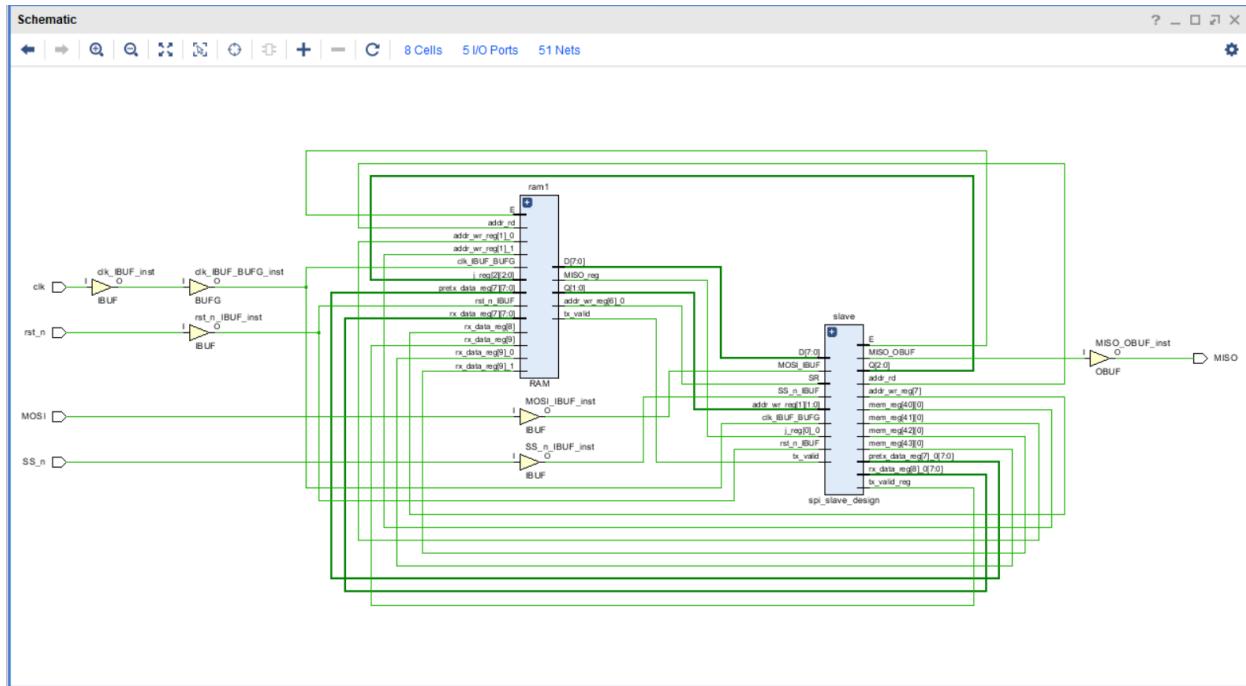
- General Messages (1 warning, 11 infos)
 - [Netlist 29-17] Analyzing 445 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Netlist 29-101] Netlist 'interface' is not ideal for floorplanning, since the celview 'RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Project 1-570] Preparing netlist for logic optimization
 - [Timing 38-478] Restoring timing data from binary archive.
 - [Timing 38-479] Binary timing data restore complete.
 - [Project 1-856] Restoring constraints from binary archive.
 - [Project 1-853] Binary constraint restore complete.
 - [Project 1-111] Unisim Transformation Summary:
 - No Unisim elements were transformed.
 - [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
 - [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

• One hot encoding

Schematic after Elaboration



Schematic after synthesis



Synthesis report showing the used encoding

```

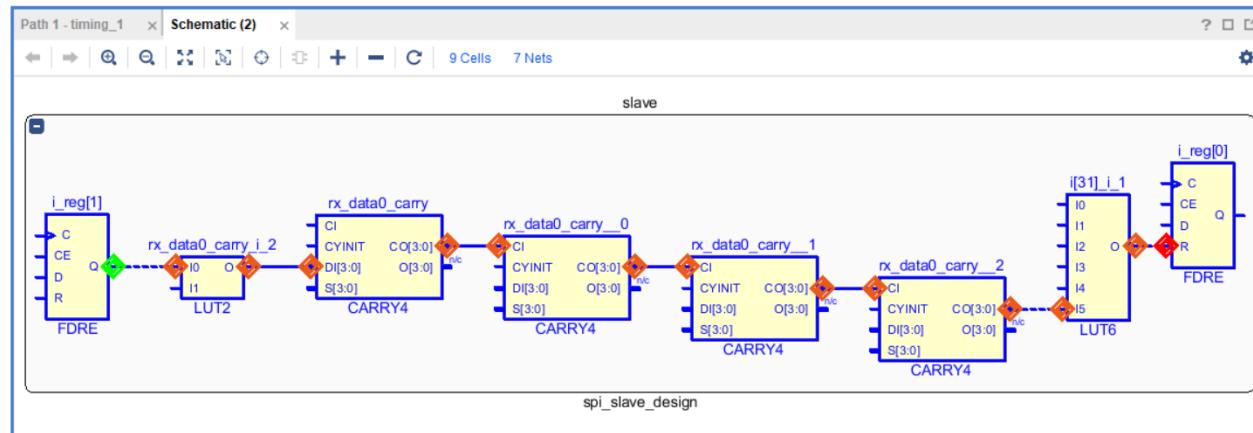
108
109          State |           New Encoding |           Previous Encoding
110
111          IDLE |           00001 |           000
112          CHK_CMD |          00010 |           001
113          WRITE |          00100 |           010
114          READ_DATA |         01000 |           100
115          READ_ADD |         10000 |           011
116
117 NFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave_design'
118 ARNING: [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [C:/Users/Lenovo/Desktop/project2/spislave.v:33]
119 ARNING: [Synth 8-327] inferring latch for variable 'memorize_addr_reg' [C:/Users/Lenovo/Desktop/project2/spislave.v:44]
120
121 'finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:21 ; elapsed = 00:00:25 . Memory (MB): peak = 787.594 ; gain = 530.812

```

Timing report after synthesis

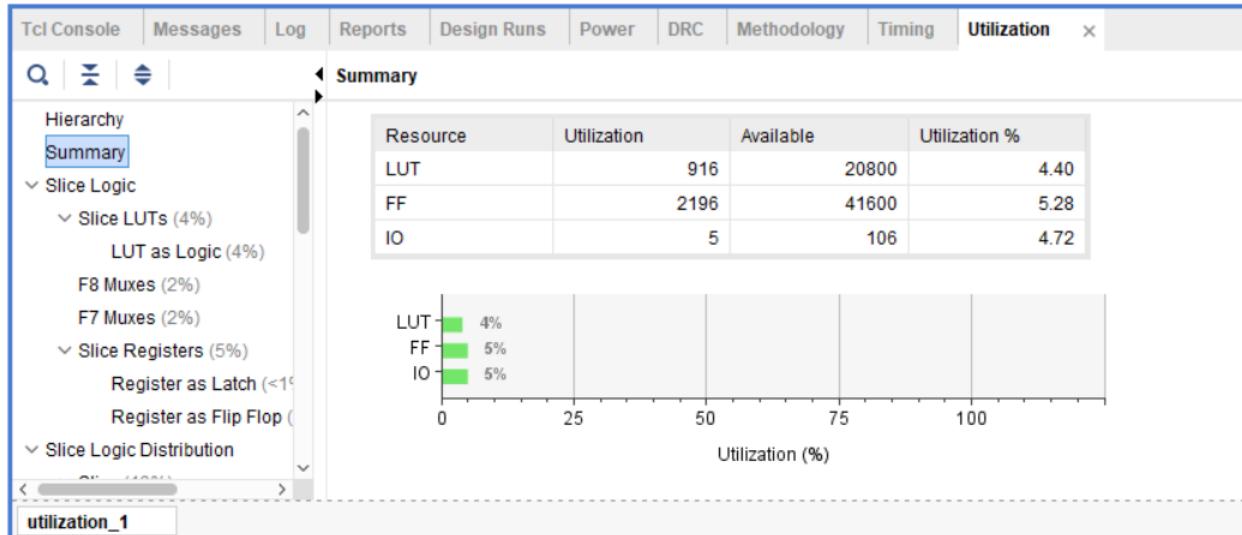
Intra-Clock Paths - sys_clk_pin - Setup											
Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination
Path 1	5.312	6	32	slave/i_reg[1]/C	slave/i_reg[0]/R	4.075	1.796	2.279	10.000	sys_clk_pin	sys_clk_pin
Path 2	5.312	6	32	slave/i_reg[1]/C	slave/i_reg[10]/R	4.075	1.796	2.279	10.000	sys_clk_pin	sys_clk_pin
Path 3	5.312	6	32	slave/i_reg[1]/C	slave/i_reg[11]/R	4.075	1.796	2.279	10.000	sys_clk_pin	sys_clk_pin
Path 4	5.312	6	32	slave/i_reg[1]/C	slave/i_reg[12]/R	4.075	1.796	2.279	10.000	sys_clk_pin	sys_clk_pin
Path 5	5.312	6	32	slave/i_reg[1]/C	slave/i_reg[13]/R	4.075	1.796	2.279	10.000	sys_clk_pin	sys_clk_pin
Path 6	5.312	6	32	slave/i_reg[1]/C	slave/i_reg[14]/R	4.075	1.796	2.279	10.000	sys_clk_pin	sys_clk_pin
Path 7	5.312	6	32	slave/i_reg[1]/C	slave/i_reg[15]/R	4.075	1.796	2.279	10.000	sys_clk_pin	sys_clk_pin
Path 8	5.312	6	32	slave/i_reg[1]/C	slave/i_reg[16]/R	4.075	1.796	2.279	10.000	sys_clk_pin	sys_clk_pin

Critical path

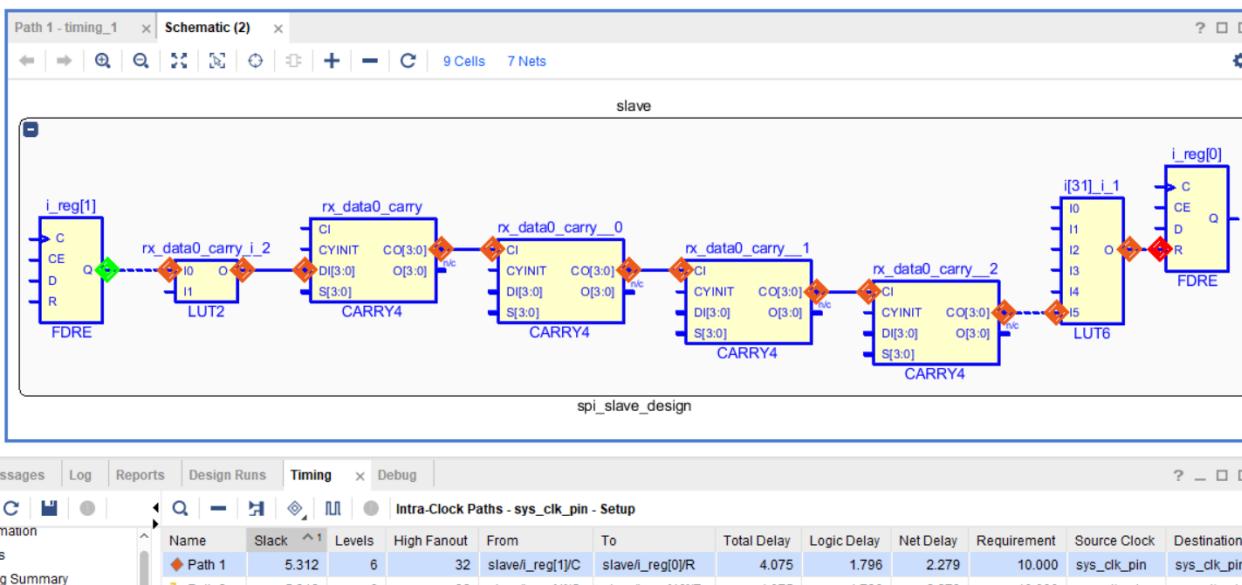


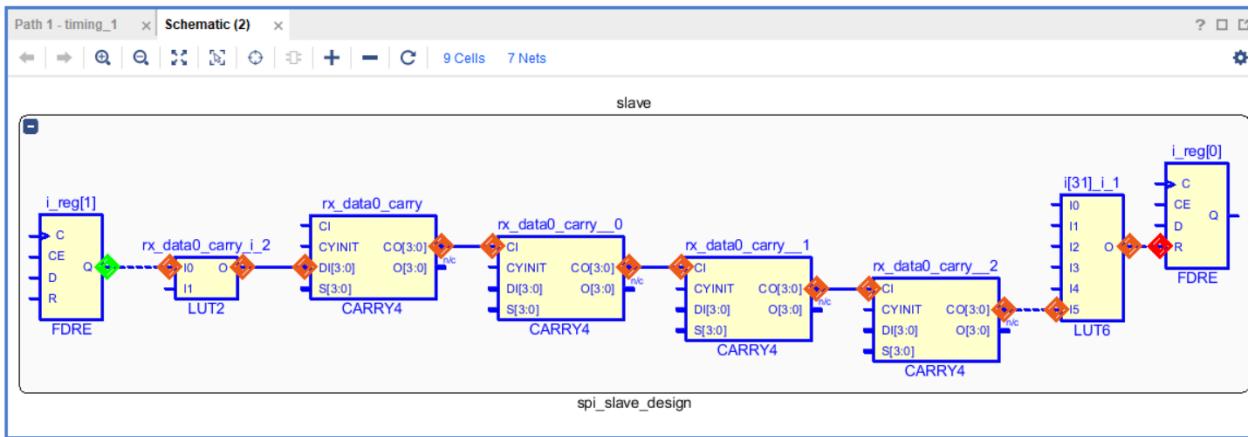
Intra-Clock Paths - sys_clk_pin - Setup											
Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination
Path 1	5.312	6	32	slave/i_reg[1]/C	slave/i_reg[0]/R	4.075	1.796	2.279	10.000	sys_clk_pin	sys_clk_pin

Utilization report



Timing report after implementation



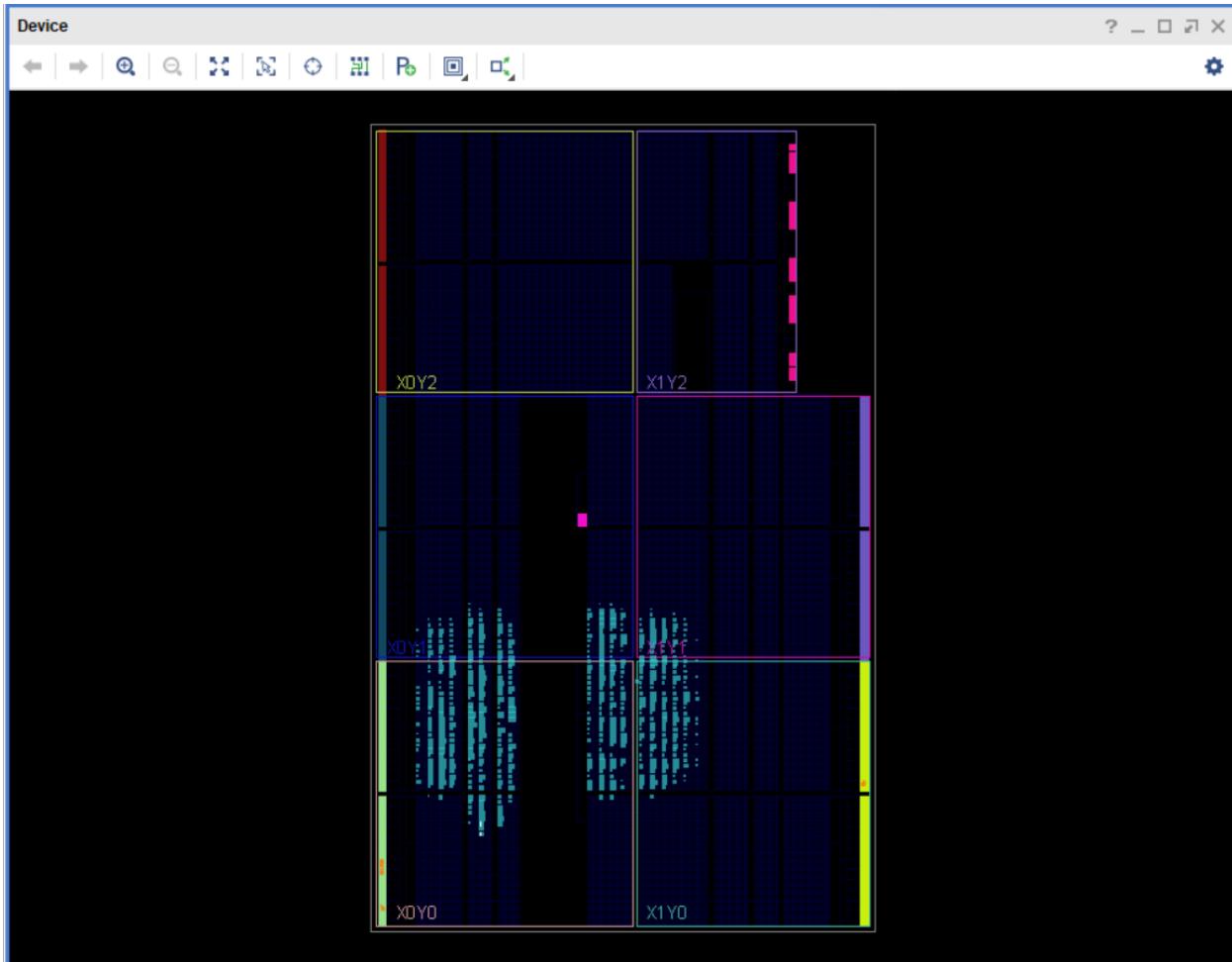


Timing x Debug

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination
Path 1	5.312	6	32	slave/i_reg[1]/C	slave/i_reg[0]/R	4.075	1.796	2.279	10.000	sys_clk_pin	sys_clk_pin

FPGA device



Messages tab for Elaboration

- ✓ Elaborated Design (7 warnings, 11 infos)
 - ✓ General Messages (7 warnings, 11 infos)
 - > ⓘ [Synth 8-6157] synthesizing module 'interface' [[interface.v:1](#)] (2 more like this)
 - ⓘ [Synth 8-155] case statement is not full and has no default [[spislave.v:30](#)]
 - ⓘ [Synth 8-567] referenced signal 'T' should be on the sensitivity list [[spislave.v:29](#)]
 - > ⓘ [Synth 8-6090] variable 'i' is written by both blocking and non-blocking assignments, entire logic could be removed [[spislave.v:96](#)] (3 more like this)
 - ⓘ [Synth 8-5788] Register mem_reg in module RAM is has both Set and reset with same priority. This may cause simulation mismatches. Consider rewriting code
 - ⓘ [Synth 8-4767] Trying to implement RAM 'mem_reg' in registers. Block RAM or DRAM implementation is not possible; see log for reasons.
 - > ⓘ [Synth 8-6155] done synthesizing module 'spi_slave_design' (1#1) [[spislave.v:1](#)] (2 more like this)
 - ⓘ [Device 21-403] Loading part xc7a35tcipg236-1L
 - ⓘ [Project 1-570] Preparing netlist for logic optimization

Messages tab for Synthesis

```
▼ Synthesis (13 warnings, 134 infos)
  ⓘ [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35tI'
  > ⓘ [Synth 8-6157] synthesizing module 'interface' [interface.v:1] (2 more like this)
  ⓘ [Synth 8-155] case statement is not full and has no default [spislave.v:30]
  ⓘ [Synth 8-567] referenced signal 'l' should be on the sensitivity list [spislave.v:29]
  > ⓘ [Synth 8-6090] variable 'l' is written by both blocking and non-blocking assignments, entire logic could be removed [spislave.v:96] (3 more like this)
  ⓘ [Synth 8-5788] Register mem_reg in module RAM is has both Set and reset with same priority. This may cause simulation mismatches. Consider rewriting code
  ⓘ [Synth 8-4767] Trying to implement RAM 'mem_reg' in registers. Block RAM or DRAM implementation is not possible; see log for reasons.
  > ⓘ [Synth 8-6155] done synthesizing module 'spi_slave_design' (1#1) [spislave.v:1] (2 more like this)
  ⓘ [Device 21-403] Loading part xc7a35tcpg236-1L
  ⓘ [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/Lenovo/Desktop/project2/basys_master_SPI.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [xil/interface_propImpl.xdc].
```

Activate Windows

Messages tab for Implementation

The screenshot shows the 'Messages' tab in the Xilinx Vivado IDE. The tab bar includes 'Tcl Console', 'Messages', 'Log', 'Reports', and 'Design Runs'. The 'Messages' tab is active, indicated by a blue border. Below the tab bar is a toolbar with icons for search, filter, and message types: Warning (26), Info (282), and Status (279). A 'Show All' button is also present. The main area displays a hierarchical list of messages under 'Implemented Design'. The first node is 'General Messages (1 warning, 13 infos)', which contains several informational messages related to netlist analysis and preparation. To the right of the message list, there is a promotional banner for Windows activation.

```
Tcl Console Messages Log Reports Design Runs
? - □
Q | H | D | T | M | B | Show All
▼ Implemented Design (1 warning, 13 infos)
  ▼ General Messages (1 warning, 13 infos)
    ⓘ [Netlist 29-17] Analyzing 445 Unisim elements for replacement
    ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    ⓘ [Netlist 29-101] Netlist interface' is not ideal for floorplanning, since the cellview 'RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
    ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
    ⓘ [Project 1-570] Preparing netlist for logic optimization
    ⓘ [Timing 38-478] Restoring timing data from binary archive.
    ⓘ [Timing 38-479] Binary timing data restore complete.
    ⓘ [Project 1-856] Restoring constraints from binary archive.
    ⓘ [Project 1-853] Binary constraint restore complete.
```

Activate Windows
Go to Settings to activate Windows.