CONVERGING (PRAGMATIST)

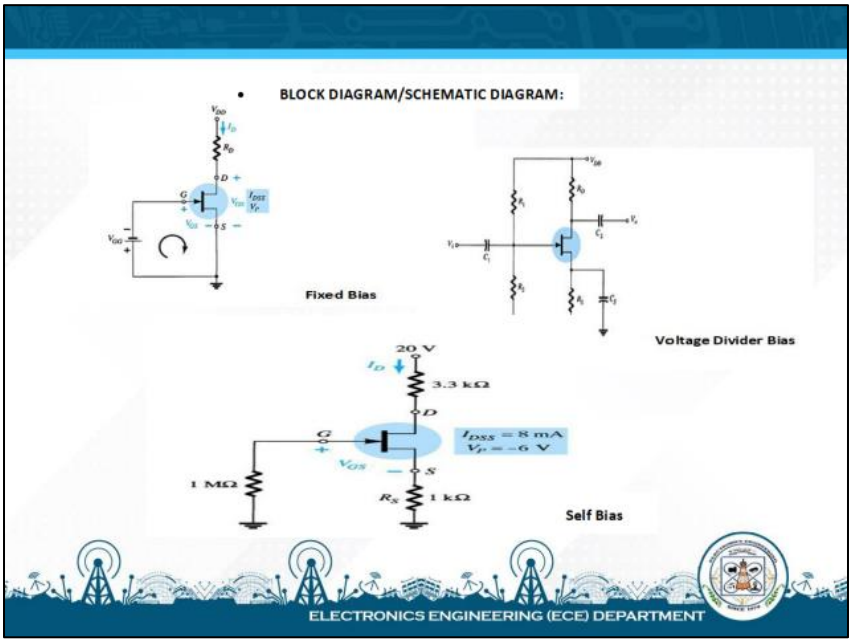
EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

BEGINNER

I. **Main Objective:** To practice basic FET bias circuit building and measurement skills by assembling a simple circuit, taking voltage and current readings, and applying simple formulas to check circuit behavior.

II. **Procedure:**

1. Enter the virtual lab and watch the presentation to learn the basic concepts of FET bias circuits, suggested VDD values, and how to choose resistor and capacitor values.
2. Based on the presentation, manually select appropriate resistor and capacitor values for your circuit during the simulation.
3. Assemble the FET bias circuit below in the VR environment using the virtual breadboard, FET, resistors, and capacitors provided.
4. Use the virtual voltmeter and ammeter to measure the voltage and current at the input and output terminals of the circuit.
5. Record your measurements manually in a worksheet outside the VR environment.
6. Calculate basic voltage and current values manually using the formulas explained during the VR presentation and put in the worksheet.
7. Create a basic block diagram that shows how the voltmeter and ammeter were connected to the circuit during your simulation.



EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

1. OBJECTIVES	
A. Content Standards	• Learners demonstrate understanding of the basic operation of a FET bias circuit by assembling a given circuit correctly in a VR laboratory. • Learners apply safe handling practices of virtual instruments (breadboard, voltmeter, ammeter) for basic measurement tasks.
B. Performance Standards	• Learners accurately follow a guided procedure to assemble a simple FET bias circuit in VR. • Learners take basic voltage and current readings at specified points with minimal error. • Learners record and compute basic voltage and current values using straightforward formulas.
C. Learning Competencies/Objectives	• Assemble the given FET bias circuit in VR following basic guided instructions. • Perform simple voltage and current measurements using VR instruments. • Record measurements in a basic table and apply simple formulas to compute voltage and current values. • Create a basic block diagram showing instrument connections.
2. CONTENT	Experiment 5: Field Effect Transistor Biasing
3. LEARNING RESOURCES	
A. References	• ECEN 30034 Experiments Material Module 9 • ECEN 30034 Instructional Material • Electronics Devices and Circuit Theory by Robert L. Boylestad and Louis Nashelsky 10 ed.
4. PROCEDURES	
A. Pre-Activity Preparation	**NAVIGATION OF VIRTUAL LABORATORY** • Students enter the VR laboratory environment and are given 5 minutes to practice basic navigation • Teachers will facilitate the activity by giving instructions, answering questions, and ensuring students are familiar with the VR setup while they explore. **LEARNING STYLE IDENTIFICATION** • Students are given 5 minutes to complete a quick Learning Style Questionnaire to determine if they are Pragmatist, Theorist, Reflector, or Activist.

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	KNOWLEDGE LEVEL ASSESSMENT • Students are given 10 minutes to take a pre-test assessing their understanding of FET bias circuits. This will classify them into Beginner, Intermediate, or Advanced levels. **ASSIGNMENT OF TRACKS** • Based on learning style and knowledge level results, students are assigned the appropriate version of the VR presentation and activity procedure.
B. Discussion of Concepts	**INTRODUCTION** A pleasant morning everyone! I'm excited to see you here in our virtual classroom today! Welcome to the Electrosphere! Today, we will explore how to assemble and measure a basic FET bias circuit. We'll work step-by-step, applying only what's practical and needed to complete the task. Don't worry about complex theories right now. We'll focus on doing the circuit using tools properly, reading voltages, and understanding how a circuit works through real actions. Are you ready to get started? Let's jump into our virtual world and bring these circuits to life! **PART 1: WHY FET BIAS CIRCUIT?** FET bias circuits help set the right operating point for the transistor. If we don't set it correctly, the transistor won't work properly. In real devices, like amplifiers or radios, wrong biasing can cause failure. ***Key Points Shown in VR Presentation:*** • *A basic FET circuit diagram (simple view)* • *Highlight where the resistors and capacitors go* • *Highlight where to connect the power supply (VDD)* Today, we will assemble the circuit to make sure the FET operates correctly and check if our measurements match basic expectations.

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PART 2: WHAT IS VDD AND WHY DOES IT MATTER?

VDD is the voltage we supply to the drain of the FET. It powers the entire circuit. Choosing the right value for VDD ensures the FET operates in the active/linear region and avoids distortion, overheating, or cutoff.

Typical Ranges:

- Low-power FET applications (amplifiers, sensors):
  VDD = 5V to 9V (Common in battery-powered or digital systems.)
- Standard analog amplifier circuits (lab use):
  VDD = 12V to 15V (Allows higher headroom for signal swings and biasing range.)
- Power applications or RF circuits:
  VDD = 18V to 24V (used with heat management and protective components).

Practical Tip:

Start with 12V in the virtual lab unless your design specifically needs more or less. This value gives enough room to observe proper VDS and ID values in most biasing methods (especially self-bias and voltage divider).

PART 3: COMPONENTS' PREVIEW

Here are the main components you'll use:

- ***Resistors (pre-selected values)***
- ***Capacitors (pre-selected values)***
- ***Breadboard***
- ***Multimeter (to measure voltage and current)***

Quick Tip for Pragmatists:

Always double-check connections. A simple wrong plug can cause wrong readings.

PART 4: DIFFERENT WAYS TO BIAS A FET

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Let's take a quick look at different ways to bias a Field Effect Transistor (FET). Just like in Bipolar Junction Transistors (BJTs), biasing helps us set the transistor to the point where it works best.

There are four common biasing methods:

1. Fixed Bias – The simplest form. A resistor connects the gate directly to the power supply. It's fast and easy to build, but not very stable with temperature changes.
2. Self-Bias – This method uses a resistor in the source leg (RS). It improves stability by creating a negative feedback effect. Good for learning and prototyping.
3. Voltage Divider Bias – This setup uses two resistors (a divider) to give a more stable gate voltage. It's very common and reliable. To analyze this circuit, we use Thevenin's Theorem for easier calculations.
4. Feedback Bias – Commonly used for enhancement-type MOSFETs. A resistor connects from output back to the input (gate), feeding some signal back and helping stabilize the circuit.

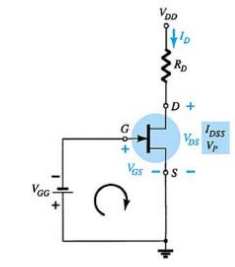
PART 5: BASIC FORMULAS

We'll use only simple formulas today to help pick resistor values.

Key Formulas Presented:

- *Ohm's Law: V = IR (to find correct resistor values for gate, drain, and source)*
- *Fixed-Bias Calculations*

$$V_{DS} = V_{DD} - I_D R_D$$
$$V_S = 0V$$
$$V_C = V_{DS}$$
$$V = V_{GS}$$
$$V_{GS} = -V_{GG}$$



EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

- *Self-Bias Calculations*

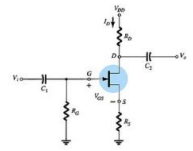
For the indicated loop, $V_{GS} = -I_D R_S$

To solve this equation:

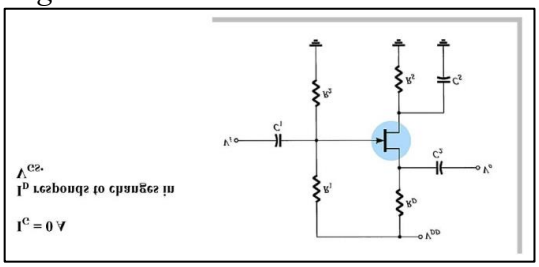
- Select an $I_D < I_{DSS}$ and use the component value of R_S to calculate V_{GS}
- Plot the point identified by I_D and V_{GS}. Draw a line from the origin of the axis to this point.
- Plot the transfer curve using I_{DSS} and V_P ($V_P = V_{GSoff}$ in specification sheets) and a few points such as $I_D = I_{DSS}/4$ and $I_D = I_{DSS}/2$ etc.

The Q-point is located where the first line intersects the transfer curve. Use the value of I_D at the Q-point (I_{DQ}) to solve for the other voltages:

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$
$$V_S = I_D R_S$$
$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$



- *Voltage-Divider Bias Calculations*



V_G is equal to the voltage across divider resistor R_2:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

The Q point is established by plotting a line that intersects the transfer curve.

Voltage-Divider Q-point

Step 1

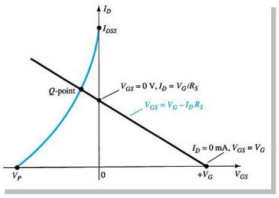
Plot the line by plotting two points:
- $V_{GS} = V_G$, $I_D = 0$ A
- $V_{GS} = 0$ V, $I_D = V_G / R_S$

Step 2

Plot the transfer curve by plotting I_{DSS}, V_P and the calculated values of I_D

Step 3

The Q-point is located where the line intersects the transfer curve



Using the value of I_D at the Q-point, solve for the other variables in the voltage-divider bias circuit:

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$V_D = V_{DD} - I_D R_D$$
$$V_S = I_D R_S$$
$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

- *Reminder that capacitors help smooth out voltages*

EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

	PART 6: BASIC SETUP ***Teacher Demonstrates in VR (with voice guide):*** • *Drag and drop the FET into the breadboard* • *Insert resistors and capacitors into proper places* • *Connect the power supply (VDD) carefully* • *Show where the multimeter probes should touch* You are encouraged to copy exactly at first. Focus on completing the setup without worrying about memorizing theories yet. **PART 7: WHAT TO MEASURE** Once your circuit is ready, you'll use the multimeter to measure: • *VGS — Gate-to-Source Voltage* • *VDS — Drain-to-Source Voltage* • *ID — Drain Current* We'll record these values in our worksheet. After measuring, you'll apply very basic formulas to double-check if your circuit behaves properly. **PART 8: CONCLUSION** You now have everything you need to start building your first FET bias circuit. Today, you learned the essentials: what a bias circuit does, how VDD powers the circuit, how to use simple formulas and how to choose the right resistors and capacitors. Now, it's your turn to make your FET bias circuit!
C. Presentation of the Experiment and Establishing a Purpose	**EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING** **Materials:** VR headset and controller, worksheet **Main Objective:** To practice basic FET bias circuit building and measurement skills by assembling a simple circuit, taking voltage and current readings,

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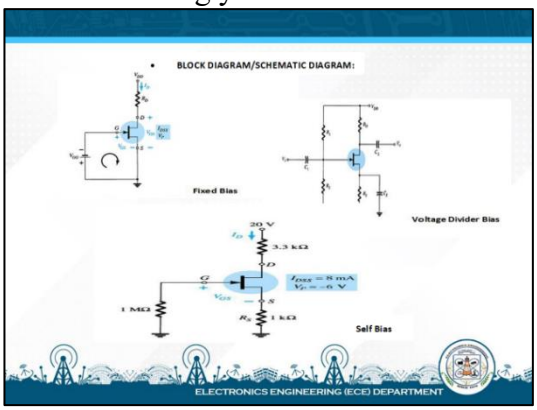
	and applying simple formulas to check circuit behavior. **Procedures:** **1.** Enter the virtual lab and watch the presentation to learn the basic concepts of FET bias circuits, suggested VDD values, and how to choose resistor and capacitor values. **2.** Based on the presentation, manually select appropriate resistor and capacitor values for your circuit during the simulation. **3.** Assemble the FET bias circuit below in the VR environment using the virtual breadboard, FET, resistors, and capacitors provided. **4.** Use the virtual voltmeter and ammeter to measure the voltage and current at the input and output terminals of the circuit. **5.** Record your measurements manually in a worksheet outside the VR environment. **6.** Calculate basic voltage and current values manually using the formulas explained during the VR presentation and put in the worksheet. **7.** Create a basic block diagram that shows how the voltmeter and ammeter were connected to the circuit during your simulation. 
D. Post-Assessment (Knowledge Check)	Students are given 10 minutes to take a post-test inside VR to measure knowledge improvement by comparing pre-test and post-test results.
E. Experiment Conclusion	The teacher summarizes key learnings, discusses results, and addresses common challenges observed during the VR activities.

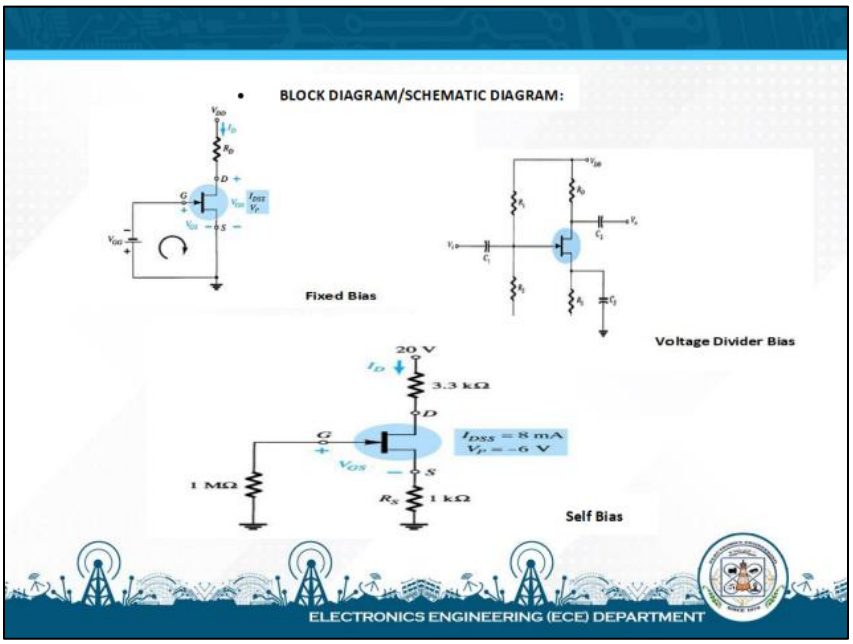
EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

INTERMEDIATE

I. **Main Objective:** To build, measure, and validate FET bias circuits in a virtual lab, applying formulas and comparing real behavior directly to expected outcomes.

II. **Procedure:**

1. Enter the virtual lab and watch the presentation to review the FET bias principles, typical VDD values, and resistor-capacitor selection.
2. Compute resistor and capacitor values using appropriate design formulas.
3. Assemble the FET bias circuit below in the VR environment.
4. Use the virtual voltmeter and ammeter to measure voltages and currents accurately at different points in your circuit.
5. Record your measurements manually in a worksheet outside the VR environment.
6. Compute and compare measured values with expected results using formulas discussed during the VR presentation and record it in the worksheet.
7. Create a block diagram showing actual measurement setups you used.



EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

I. OBJECTIVES	
A. Content Standards	• Learners demonstrate understanding of FET bias circuit behavior through independent assembly and theoretical validation using measurement results. • Learners apply analytical thinking to recognize and explain minor discrepancies between theoretical and practical measurements.
B. Performance Standards	• Learners independently assemble the given FET bias circuit in VR, selecting appropriate resistor and capacitor values based on calculations. • Learners perform accurate multi-point measurements and organize data for analysis. • Learners compare theoretical and measured results and explain possible causes of deviations.
C. Learning Competencies/Objectives	• Assemble the given FET bias circuit in VR independently with minimal guidance. • Select suitable resistor and capacitor values based on theoretical calculations. • Accurately measure voltages and currents across multiple circuit points. • Organize data systematically, compare theoretical and measured values, and reflect on minor discrepancies. • Create a functional block diagram of the actual VR measurement setup.
II. CONTENT	Experiment 5: Field Effect Transistor Biasing
III. LEARNING RESOURCES	
A. References	• ECEN 30034 Experiments Material Module 9 • ECEN 30034 Instructional Material • Electronics Devices and Circuit Theory by Robert L. Boylestad and Louis Nashelsky 10 ed.
IV. PROCEDURES	
A. Pre-Activity Preparation	**NAVIGATION OF VIRTUAL LABORATORY** • Students enter the VR laboratory environment and are given 5 minutes to practice basic navigation • Teachers will facilitate the activity by giving instructions, answering questions, and ensuring students are familiar with the VR setup while they explore. **LEARNING STYLE IDENTIFICATION** • Students are given 5 minutes to complete a quick Learning Style Questionnaire to determine if they are Pragmatist, Theorist, Reflector, or Activist.

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	KNOWLEDGE LEVEL ASSESSMENT • Students are given 10 minutes to take a pre-test assessing their understanding of FET bias circuits. This will classify them into Beginner, Intermediate, or Advanced levels. **ASSIGNMENT OF TRACKS** Based on learning style and knowledge level results, students are assigned the appropriate version of the VR presentation and activity procedure.
B. Discussion of Concepts	**INTRODUCTION** Good day. Welcome to the Electrosphere! Today, we're diving deeper into the practical side of FET biasing, not just wiring up components but understanding why we choose certain values and how each part affects the transistor's operation. In this session, we'll revisit and apply key concepts like typical VDD, resistor, and capacitor values, biasing methods, and formulas. This goes beyond basic connection because we'll talk about setting the correct operating point, avoiding distortion, and ensuring your FET performs reliably. Let's start! **PART 1. REVIEW OF FET BIASING METHODS** In this section, we'll revisit the key FET biasing configurations you'll encounter in real-world circuits. While in VR, you'll see how each method affects component values and placement especially in relation to VDD selection and how resistors and capacitors shape circuit behavior. You're expected to be familiar with basic transistor operation, so let's focus on practical differences between methods and when to use each: 1. Fixed Bias • Gate is connected through a resistor to VDD. • Simple to implement but lacks thermal stability. • Useful for controlled lab conditions and basic switching applications.

EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

2. Self-Bias
    - Source resistor (RS) introduces negative feedback.
    - Improves stability over fixed bias.
    - VGS is derived from voltage drop across RS.
    - Watch how source voltage influences gate biasing in the simulation.
3. Voltage Divider Bias
    - Uses two resistors (R1 and R2) to set a stable gate voltage.
    - Offers better control over VGS and consistent Q-point.
    - In VR, observe how Thevenin's equivalent helps simplify analysis.
4. Feedback Bias
    - A resistor connects from the drain back to the gate.
    - Enhances stability, especially for enhancement-mode MOSFETs.
    - Circuit responds dynamically to drain current changes.

During the VR walkthrough, pay close attention to how VDD levels (typically 9V–15V) and RC time constants (determined by resistor-capacitor values) influence signal behavior and bias point stability. You'll be adjusting or reviewing these to match the biasing method used.

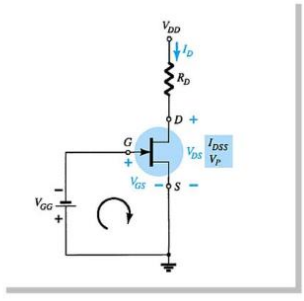
PART 2. REVIEW OF BASIC FORMULAS

We'll use only simple formulas today to help pick resistor values.

Key Formulas Presented:

- *Ohm's Law: V = IR (to find correct resistor values for gate, drain, and source)*
- *Fixed-Bias Calculations*

$V_{DS} = V_{DD} - I_D R_D$
$V_S = 0V$
$V_C = V_{DS}$
$V = V_{GS}$
$V_{GS} = -V_{GG}$



EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

- *Self-Bias Calculations*

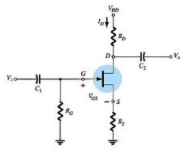
For the indicated loop, $V_{GS} = -I_D R_S$

To solve this equation:

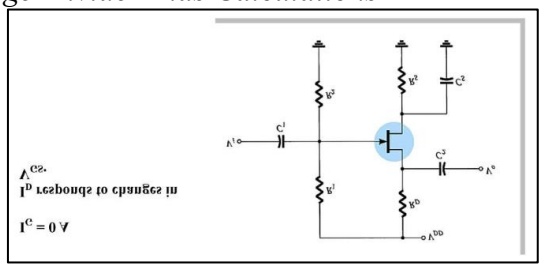
- Select an $I_D < I_{DSS}$ and use the component value of R_S to calculate V_{GS}
- Plot the point identified by I_D and V_{GS}. Draw a line from the origin of the axis to this point.
- Plot the transfer curve using I_{DSS} and V_P ($V_P = V_{GSoff}$ in specification sheets) and a few points such as $I_D = I_{DSS}/4$ and $I_D = I_{DSS}/2$ etc.

The Q-point is located where the first line intersects the transfer curve. Use the value of I_D at the Q-point (I_{DQ}) to solve for the other voltages:

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$
$$V_S = I_D R_S$$
$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$



- *Voltage-Divider Bias Calculations*



V_G is equal to the voltage across divider resistor R_2:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

The Q point is established by plotting a line that intersects the transfer curve.

Voltage-Divider Q-point

Step 1

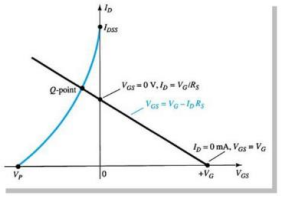
Plot the line by plotting two points:
- $V_{GS} = V_G$, $I_D = 0$ A
- $V_{GS} = 0$ V, $I_D = V_G / R_S$

Step 2

Plot the transfer curve by plotting I_{DSS}, V_P and the calculated values of I_D

Step 3

The Q-point is located where the line intersects the transfer curve



Using the value of I_D at the Q-point, solve for the other variables in the voltage-divider bias circuit:

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$V_D = V_{DD} - I_D R_D$$
$$V_S = I_D R_S$$
$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

- *Reminder that capacitors help smooth out voltages*

EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

	PART 3: CONCLUSION Great job following through the discussion! You've now reviewed the key principles behind FET biasing, including how to set VDD correctly, and how resistor-capacitor combinations shape the transistor's performance. It's now your turn to put these concepts into action. Begin your virtual lab activity by assembling the bias circuit, measuring VGS, VDS, and ID, and analyzing whether your design aligns with expected values.
C. Presentation of the Experiment and Establishing a Purpose	**EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING** **Materials:** VR headset and controller, worksheet **Main Objective:** To build, measure, and validate FET bias circuits in a virtual lab, applying formulas and comparing real behavior directly to expected outcomes. **Procedure:** **1.** Enter the virtual lab and watch the presentation to review the FET bias principles, and basic formulas. **2.** Compute resistor and capacitor values using appropriate design formulas. **3.** Assemble the FET bias circuit below in the VR environment. **4.** Use the virtual voltmeter and ammeter to measure voltages and currents accurately at different points in your circuit. **5.** Record your measurements manually in a worksheet outside the VR environment. **6.** Compute and compare measured values with expected results using formulas discussed during the VR presentation and record it in the worksheet. **7.** Create a block diagram showing actual measurement setups you used.
D. Post-Assessment (Knowledge Check)	Students are given 10 minutes to take a post-test inside VR to measure knowledge improvement by comparing pre-test and post-test results.
E. Experiment Conclusion	The teacher summarizes key learnings, discusses results, and addresses common challenges observed during the VR activities.

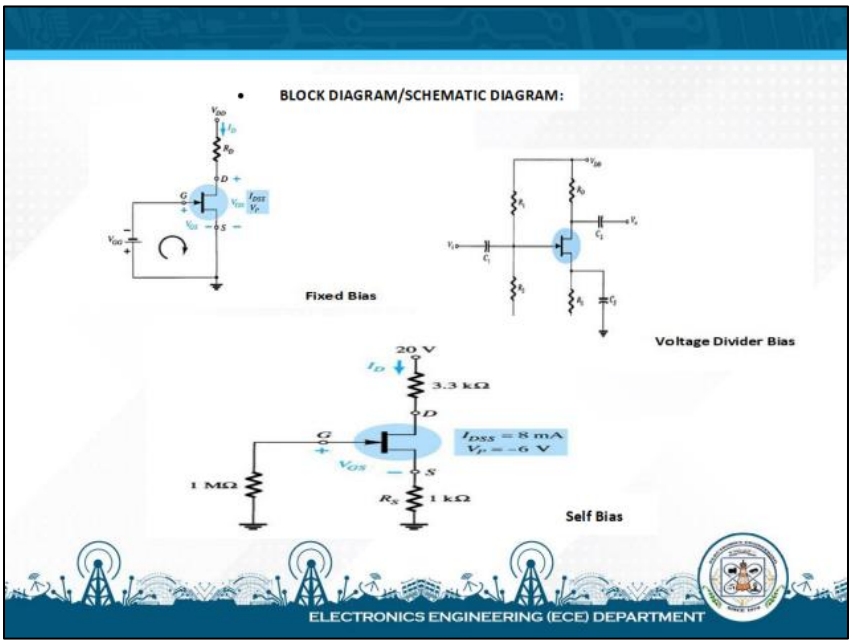
EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

DIFFICULT

V. Main Objective: To design, optimize, and troubleshoot FET bias circuits for specific goals, using practical VR measurements, manual calculations, and direct evaluation of circuit performance.

VI. Procedure:

1. Enter the virtual lab and watch the presentation regarding bias circuit optimization, and strategies for fine-tuning circuit behavior.
2. Select optimized resistor and capacitor values based on the design guidelines provided.
3. Assemble the given FET bias circuit below inside VR using the virtual breadboard and components based on your chosen values.
4. Use the virtual voltmeter and ammeter to measure voltages and currents.
5. Record your measurements manually in a worksheet outside the VR environment.
6. Manually compute expected voltages and currents using known equations and compare them with your actual VR measurements.
7. Document your results systematically and identify any design-related anomalies.
8. Draw a detailed block diagram that clearly illustrates the signal flow and instrument connections in your setup.



EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

I. OBJECTIVES	
A. Content Standards	• Learners demonstrate advanced understanding of FET bias circuit performance, identifying causes of real-world measurement deviations and proposing optimizations. • Learners apply troubleshooting strategies and critical analysis to enhance circuit reliability and performance.
B. Performance Standards	• Learners optimize resistor and capacitor values based on theoretical understanding and practical VR results. • Learners troubleshoot and refine the assembled FET bias circuit to achieve closer alignment between measured and expected values. • Learners develop a detailed block diagram showing refined signal and measurement flows based on their analysis.
C. Learning Competencies/Objectives	• Independently select optimized resistor and capacitor values for improved FET bias performance. • Assemble, measure, and troubleshoot the given FET bias circuit in VR with minimal supervision. • Analyze significant deviations between expected and measured results, diagnose causes, and propose refined solutions. • Develop a detailed block diagram illustrating instrument signal flow and finalized circuit setup.
II. CONTENT	Experiment 5: Field Effect Transistor Biasing
III. LEARNING RESOURCES	
A. References	• ECEN 30034 Experiments Material Module 9 • ECEN 30034 Instructional Material • Electronics Devices and Circuit Theory by Robert L. Boylestad and Louis Nashelsky 10 ed.
IV. PROCEDURES	
A. Pre-Activity Preparation	**NAVIGATION OF VIRTUAL LABORATORY** • Students enter the VR laboratory environment and are given 5 minutes to practice basic navigation • Teachers will facilitate the activity by giving instructions, answering questions, and ensuring students are familiar with the VR setup while they explore.

EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

	LEARNING STYLE IDENTIFICATION • Students are given 5 minutes to complete a quick Learning Style Questionnaire to determine if they are Pragmatist, Theorist, Reflector, or Activist. **KNOWLEDGE LEVEL ASSESSMENT** • Students are given 10 minutes to take a pre-test assessing their understanding of FET bias circuits. This will classify them into Beginner, Intermediate, or Advanced levels. **ASSIGNMENT OF TRACKS** Based on learning style and knowledge level results, students are assigned the appropriate version of the VR presentation and activity procedure.
B. Discussion of Concepts	**INTRODUCTION** A pleasant morning everyone! It's great to welcome you here to the Electrosphere! Today, we're leveling up! This session is crafted for those who already have a strong grasp of basic biasing. We'll focus not just on building circuits, but on optimizing bias circuits for the best performance. You'll learn practical strategies to fine-tune circuit behavior, balancing parameters like gain, linearity, power efficiency, and stability. Ready to elevate your circuit design skills? Let's dive into advanced biasing optimization in our virtual world! **PART 1: WHY OPTIMIZE BIAS CIRCUITS?** Even if a transistor works with basic biasing, it might not perform optimally. Poor optimization can cause: • Non-linearity (distortion in amplifiers) • Thermal runaway (increased current leading to overheating) • Reduced gain or wrong operating region • Poor noise performance (especially in low-noise applications) ***Optimization ensures:***

	• Stable Q-point (Operating point) • Maximum symmetrical signal swing (avoid clipping) • Minimum distortion • Controlled power dissipation ***Key Points Shown in VR Presentation:*** • *Importance of setting the Q-point in the middle of the load line* • *How device parameters (like β for BJTs, or Vth for FETs) shift with temperature* • *Real-world factors: load variations, temperature drift, and manufacturing tolerances* **PART 2: STRATEGIES FOR BIAS OPTIMIZATION** Let's go over the practical methods shown in the presentation for fine-tuning bias circuits: 1. Use of Emitter (or Source) Degeneration • Add a resistor to the emitter (BJT) or source (FET). • It introduces negative feedback which improves thermal stability and linearity. 2. Fine Adjustment of Base/Gate Voltage • Instead of fixed resistors only, use a voltage divider with trimmer potentiometer. • Let's you "dial in" the exact Vb (BJT) or Vg (FET) needed to set the desired operating point. 3. Implement Temperature Compensation • Use temperature-sensitive components like thermistors or diode junctions. • As temperature rises, these components adjust biasing automatically to prevent thermal runaway. ***Example:*** *Adding a silicon diode in the bias path whose Vbe drops with temperature to counteract transistor Vbe drop*.

EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

4. Load Line Shifting

- After setting the initial bias, recalculate the load line based on real component behavior (not just ideal).
- Adjust collector/drain resistor (RC or RD) for symmetrical voltage swing, ensuring maximum undistorted output.

Aim for the Q-point roughly halfway between VCC and ground for amplifier circuits.

5. Bypass Capacitor Optimization

- Bypass capacitors across emitter/source resistors restore AC gain while preserving DC stability.
- Fine-tune capacitor value to control lower cutoff frequency (fL) in amplifier designs.

Formula:

$$f_L = \frac{1}{2\pi R_E C}$$

Larger C → Lower cutoff frequency
Smaller C → Higher cutoff frequency

PART 3: WHAT TO MEASURE AND FINE-TUNE

Once you've applied optimization techniques, verify performance by measuring:

- VCE / VDS (Collector-to-Emitter / Drain-to-Source voltage) - Check if the Q-point is centered.
- IC / ID (Collector / Drain current) - Confirm bias stability under temperature changes.
- Gain (Av) - Confirm amplifier gain matches design specs.
- Distortion - Check output waveform symmetry.
- Power Dissipation - Ensure within safe device limits.

EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

	Slight changes (±10%) in resistors or VDD should not cause major drift in biasing. If it does, your circuit needs better stabilization. **PART 4: CONCLUSION** Today, you explored how bias circuit optimization is not just about making circuits "work," but making them perform reliably and efficiently. You learned practical fine-tuning strategies. Now, it's your turn! Do the experiment and apply these techniques. Let's start!
C. Presentation of the Experiment and Establishing a Purpose	**EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING** **Materials:** VR headset and controller, worksheet **Main Objective:** To design, optimize, and troubleshoot FET bias circuits for specific goals, using practical VR measurements, manual calculations, and direct evaluation of circuit performance. **Procedure:** **1.** Enter the virtual lab and watch the presentation regarding bias circuit optimization, and strategies for fine-tuning circuit behavior. **2.** Select optimized resistor and capacitor values based on the design guidelines provided. **3.** Assemble the given FET bias circuit below inside VR using the virtual breadboard and components based on your chosen values. **4.** Use the virtual voltmeter and ammeter to measure voltages and currents. **5.** Record your measurements manually in a worksheet outside the VR environment. **6.** Manually compute expected voltages and currents using known equations and compare them with your actual VR measurements. **7.** Document your results systematically and identify any design-related anomalies. **8.** Draw a detailed block diagram that clearly illustrates the signal flow and instrument connections in your setup.

EXPERIMENT 5: FIELD EFFECT TRANSISTOR BIASING

D. Post-Assessment (Knowledge Check)	Students are given 10 minutes to take a post-test inside VR to measure knowledge improvement by comparing pre-test and post-test results.
E. Experiment Conclusion	The teacher summarizes key learnings, discusses results, and addresses common challenges observed during the VR activities.