CLASS 18*=CSCI 160
Spring'21

Project questions
will be detailed next class

PROJECT - ***Octal Full-Adder***

Input: A, B = octal digits (see representation below); C_{in}= binary digit

Output: S = octal digit (see representation below); C_{out}= binary digit

Task: Using only binary FAs to perform the actual addition, design a circuit that performs as an octal FA. More specifically, this circuit would input the two octal digits A, B, convert them into binary numbers, add them using three binary FAs, convert the binary result back to octal, and output the sum as an octal digit, and the binary carry out.

PROJECT - OCTAL FA

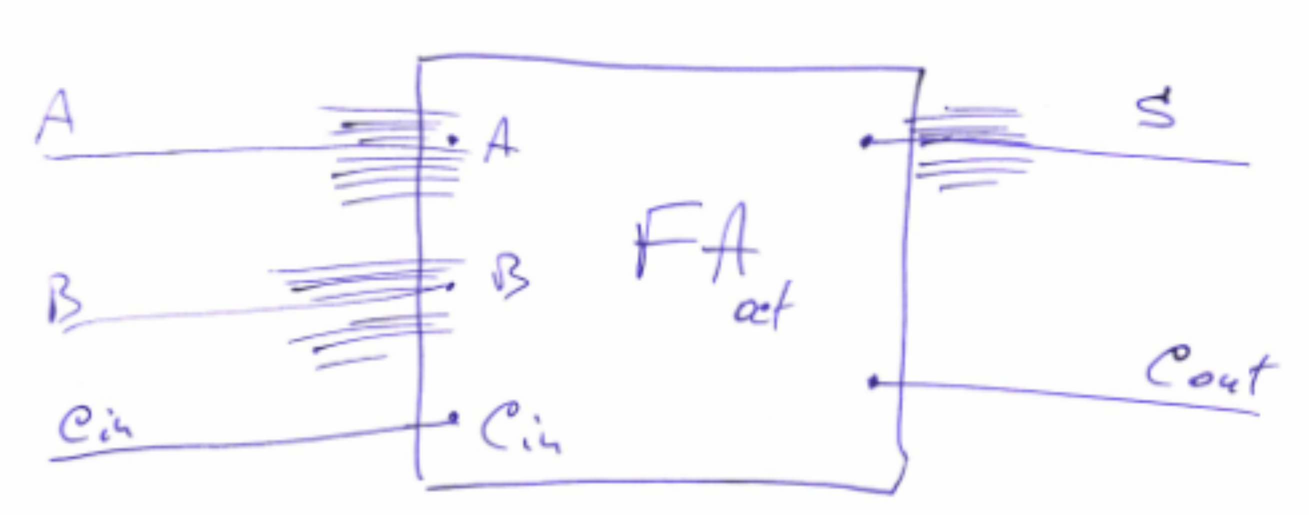
Input: A, B = octal digits (see representation below); C_{in} = binary digit

Output: S = octal digit (see representation below); C_{out} = binary digit

Modular approach:

Big Picture:

Task: Using only binary FAs to perform the actual addition, design a circuit that performs as an octal FA. More specifically, this circuit would input the two octal digits A, B, convert them into binary numbers, add them using only binary FAs, convert the binary result back to octal, and output the sum as an octal digit, and the binary carry out.



Example:

Performance-how it should work (big picture):

If Input:
A = 6_8
B = 5_8
$C_{in} = 0$

$$\xrightarrow{FA_{oct} \text{ (or } FA_8)}$$

Output:
S = 3_8
$C_{out} = 1$

$$6_8 + 5_8 = 11_{10} = 1 \times 8^1 + 3 \times 8^0 = \underset{C_{out}}{1}\underset{S}{3}{}_8$$

Inside:

$$6_8 \xrightarrow{Cv_{8\to2}} 110_2$$

$$5_8 \xrightarrow{Cv_{8\to2}} 101_2$$

Next:

Add 110_2 and 101_2 using several FA_2

Get sum 011_2 and $C_{out} = 1$

$$011_2 \xrightarrow{Cv_{2\to8}} 3_8$$

Output:
S = 3_8 and $C_{out} = 1$

Separate Modules (= diagrams) for:

1) $Cv_{8\to2}$

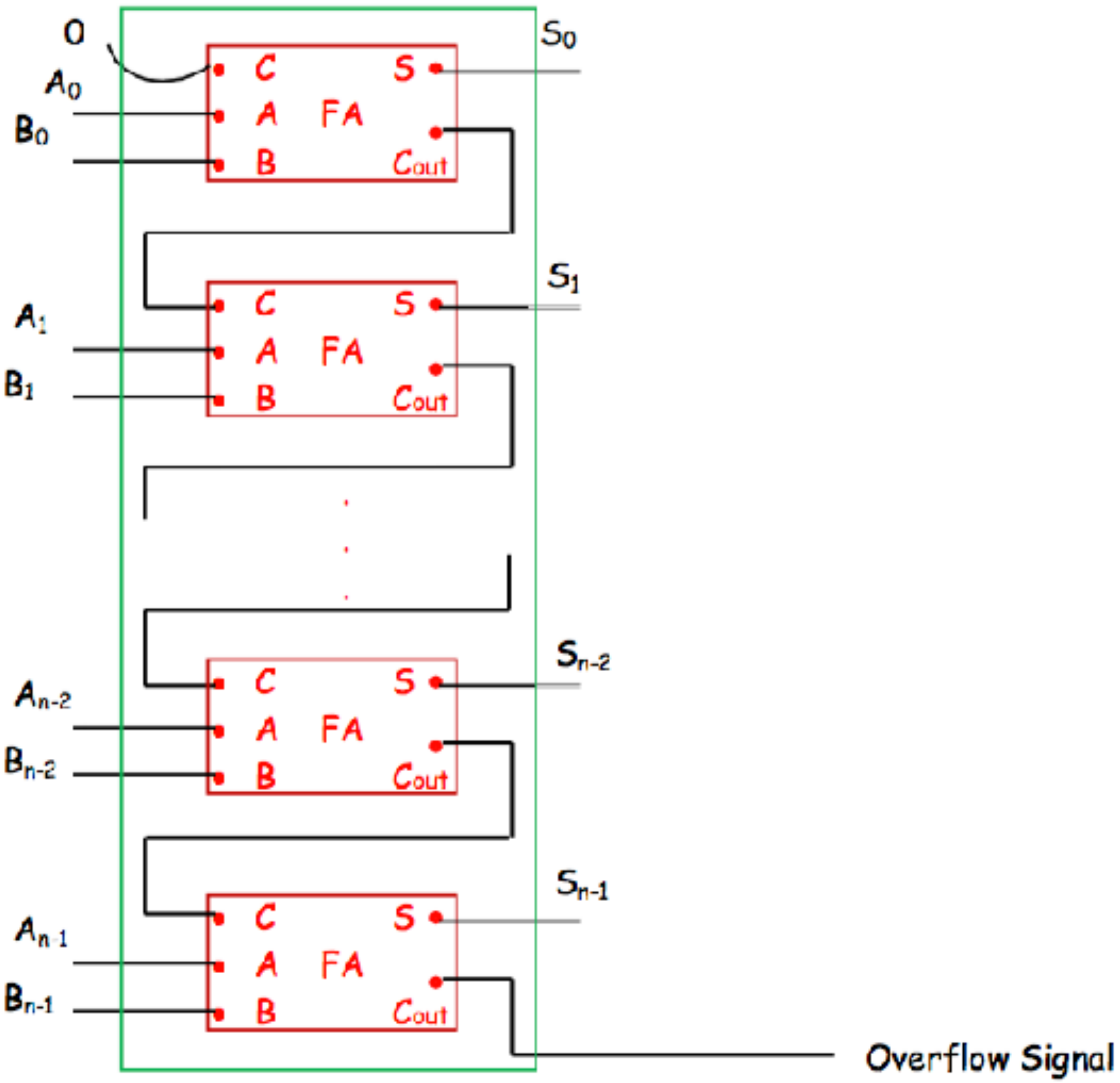
2) $Cv_{2\to8}$

3) general diagram using boxes for FA_2, $Cv_{8\to2}$ and $Cv_{2\to8}$, connecting Inputs to Outputs.

Adding multiple digit numbers

Suppose we have two n-digit binary numbers: $A = A_{n-1}\,A_{n-2}\,.\,.\,.\,A_1\,A_0$ **and** $B = B_{n-1}\,B_{n-2}\,.\,.\,.\,B_1\,B_0$

We obtain their sum $S = S_{n-1}\,S_{n-2}\,.\,.\,.\,S_1\,S_0$ using binary FAs, by adding them bit by bit starting with the lsd's:

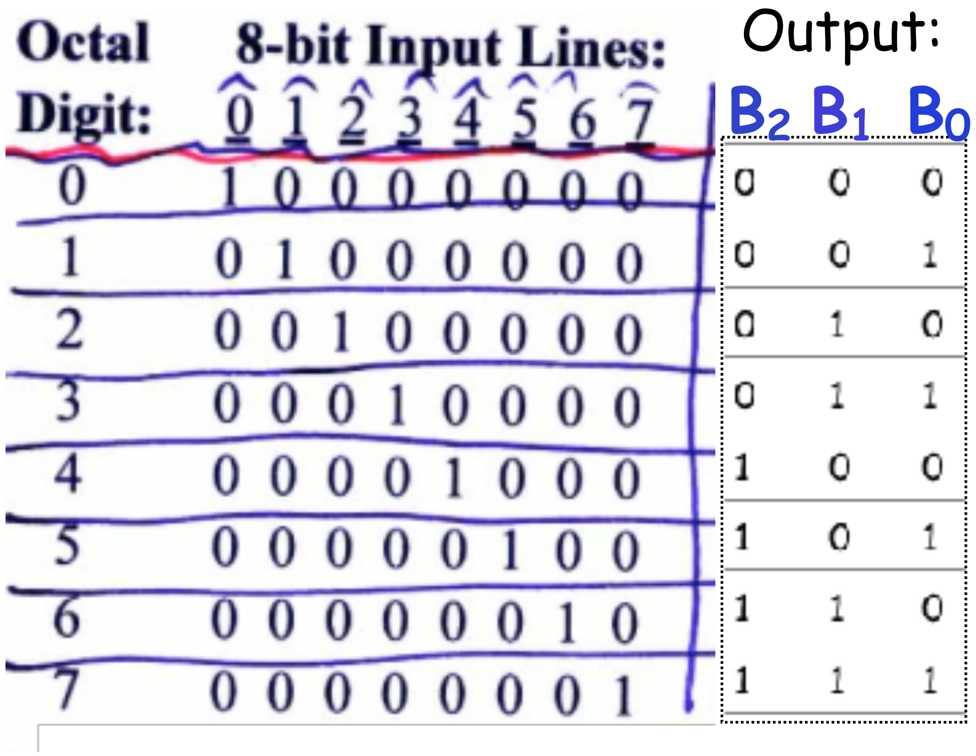


Input/Output binary representation of octal digits

Every octal digit will be represented using the following **8-bit binary representation:**

Octal Digit:	**8-bit Input Lines:**							
	0	1	2	3	4	5	6	7
0	1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0
3	0	0	0	1	0	0	0	0
4	0	0	0	0	1	0	0	0
5	0	0	0	0	0	1	0	0
6	0	0	0	0	0	0	1	0
7	0	0	0	0	0	0	0	1

Converter Base 8 ---> Base 2



Octal	8-bit Input Lines:								Output:		
Digit:	$\hat{0}$	$\hat{1}$	$\hat{2}$	$\hat{3}$	$\hat{4}$	$\hat{5}$	$\hat{6}$	$\hat{7}$	B_2	B_1	B_0
0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	1
2	0	0	1	0	0	0	0	0	0	1	0
3	0	0	0	1	0	0	0	0	0	1	1
4	0	0	0	0	1	0	0	0	1	0	0
5	0	0	0	0	0	1	0	0	1	0	1
6	0	0	0	0	0	0	1	0	1	1	0
7	0	0	0	0	0	0	0	1	1	1	1

$B_2 = \hat{4} + \ldots + \hat{7}$

$B_1 = \ldots$

$B_0 = \ldots$

You are required to design this circuit in a structured, top-down approach. You must give on separate pages all three modules described on the slide #3 of Class 18*, and use the hints from of same Class 18* for the first module. You must encircle your diagrams to clearly show all the Input/Output lines: all inputs must come from left and all outputs must go to the right.

*If you can, use **teams** of 1-4 students. Give all names. Each submit the project as you submit your HW.*

The presentation of the project is very important.

Note: I set aside the class on Monday, May 3 for you to work on this group project, and submit by the end of May 4.
We will not meet for class during this day, while you need to organize your work in groups, and submit it.

Due: ***Tuesday, May 4, midnight.***