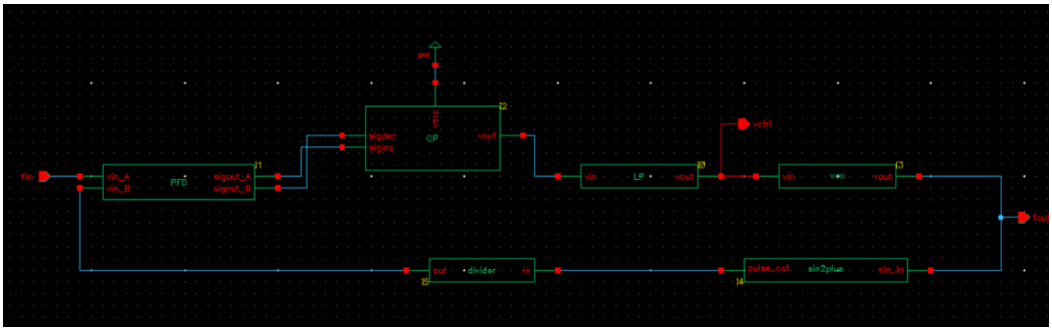
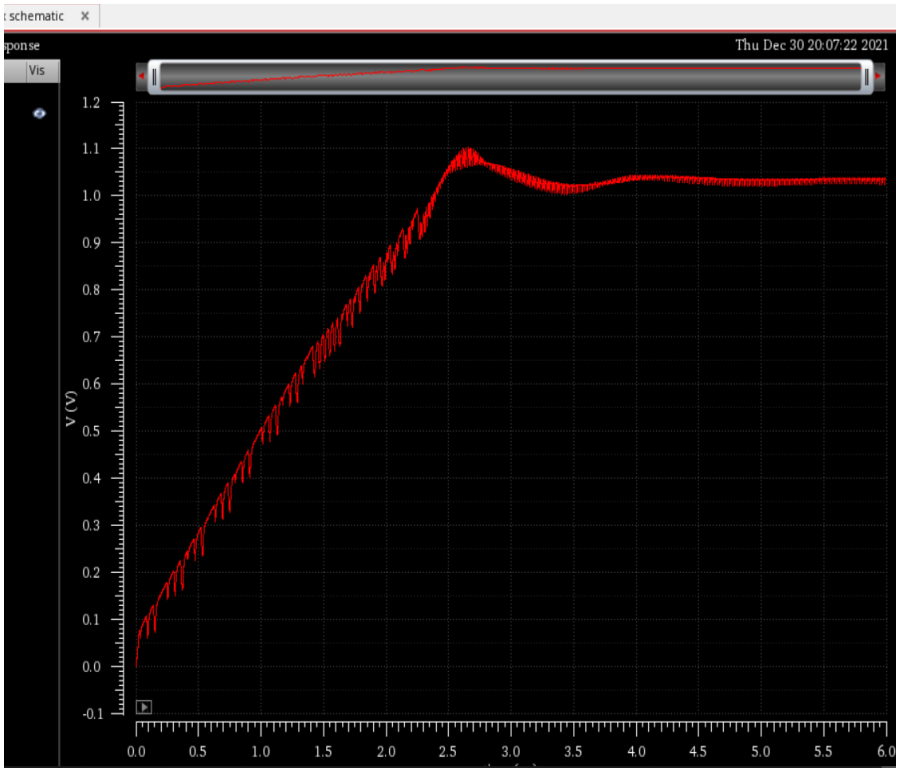
Lab4_mini_report

Lab1:

1.schematic

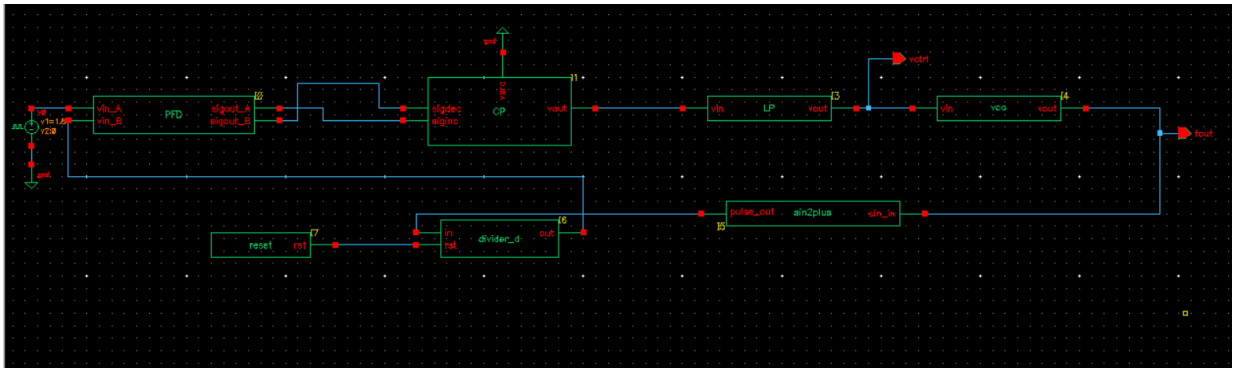


2.simulation waveform

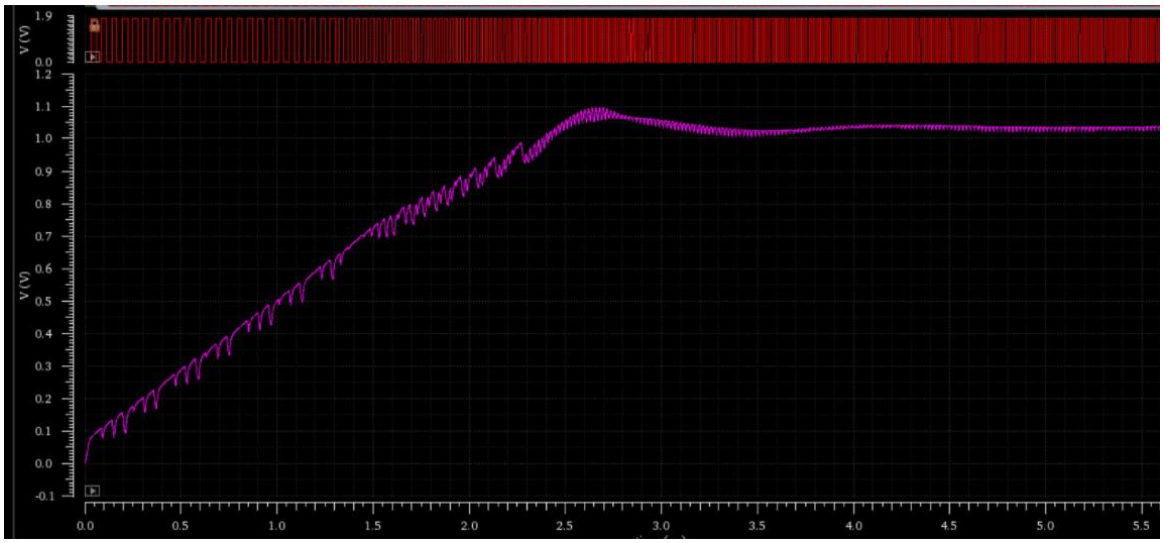


Lab2:

1.schematic

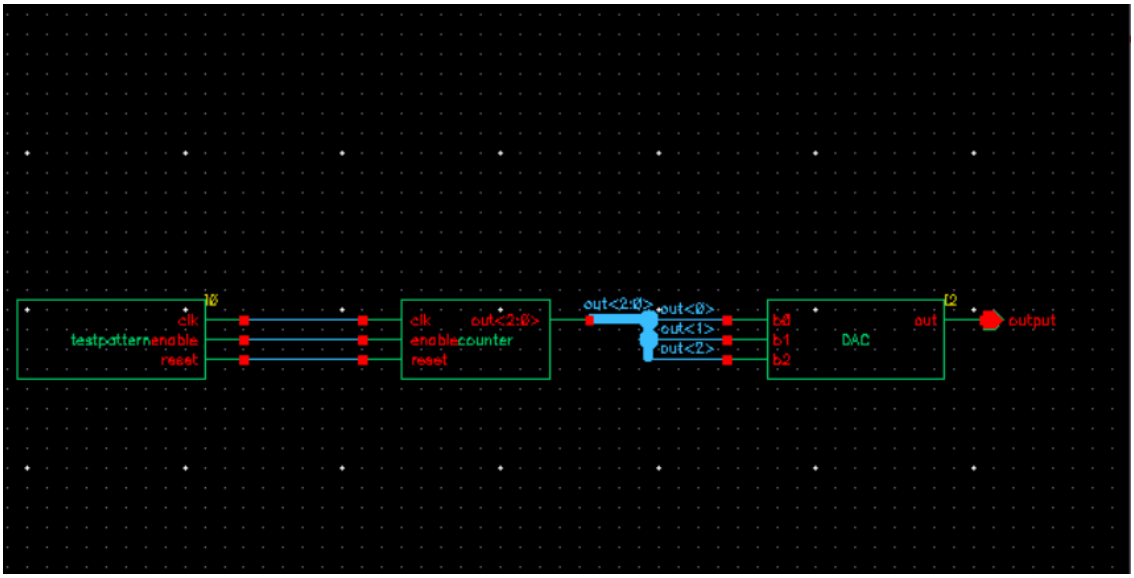


2.simulation waveform

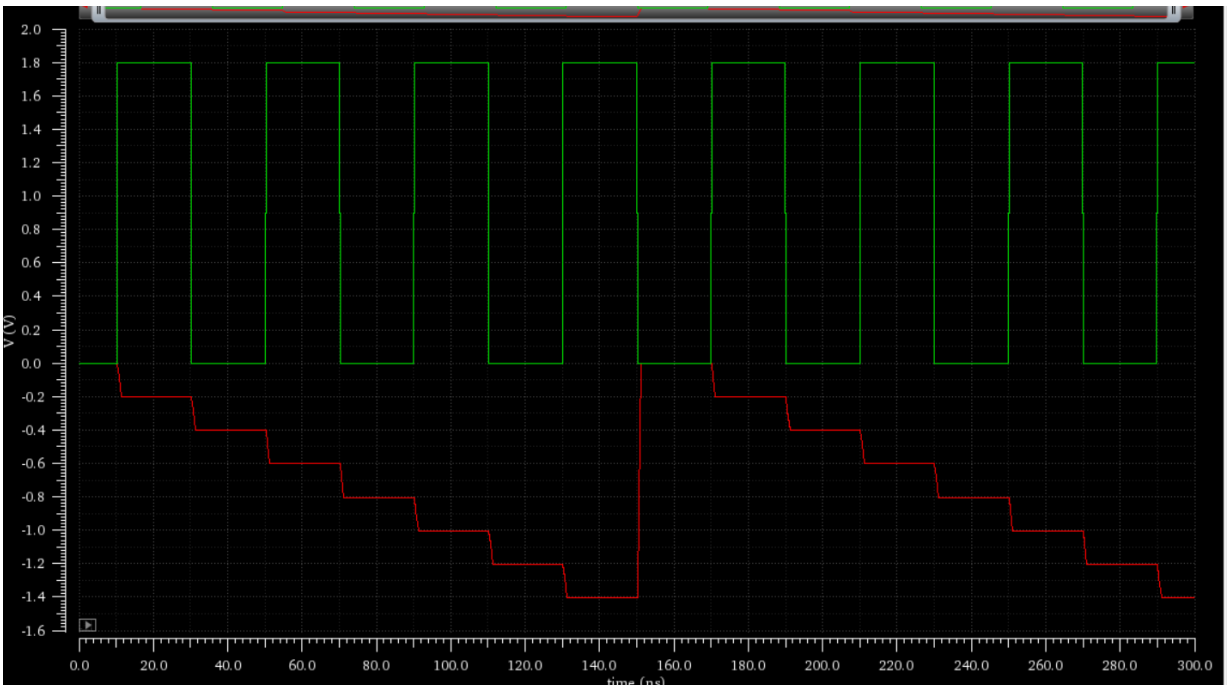


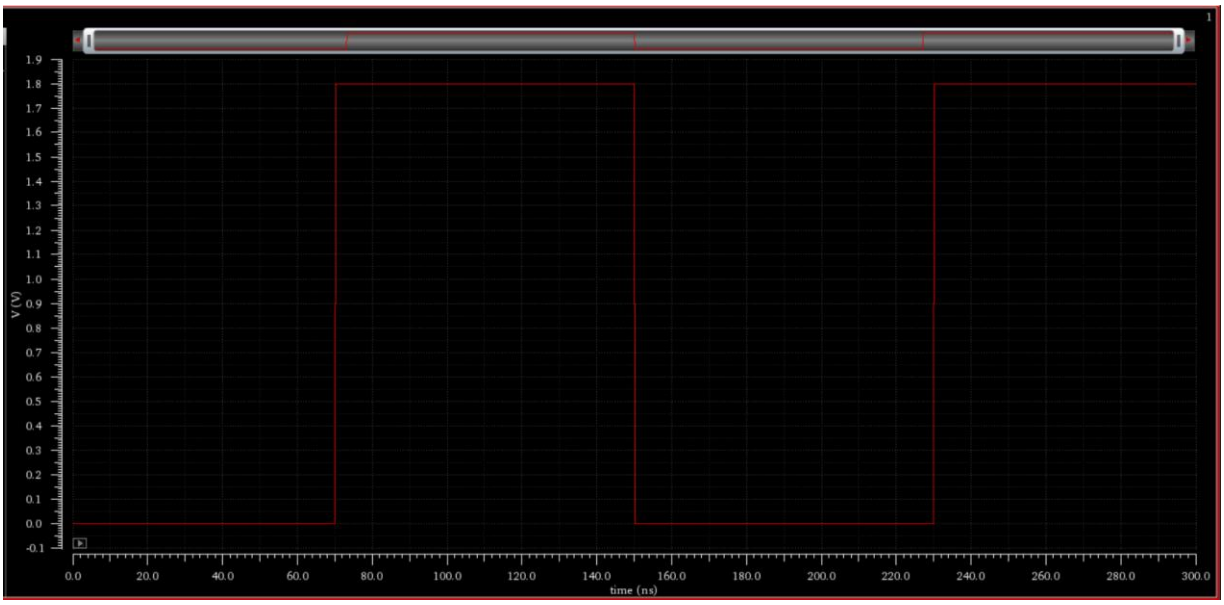
Lab3:

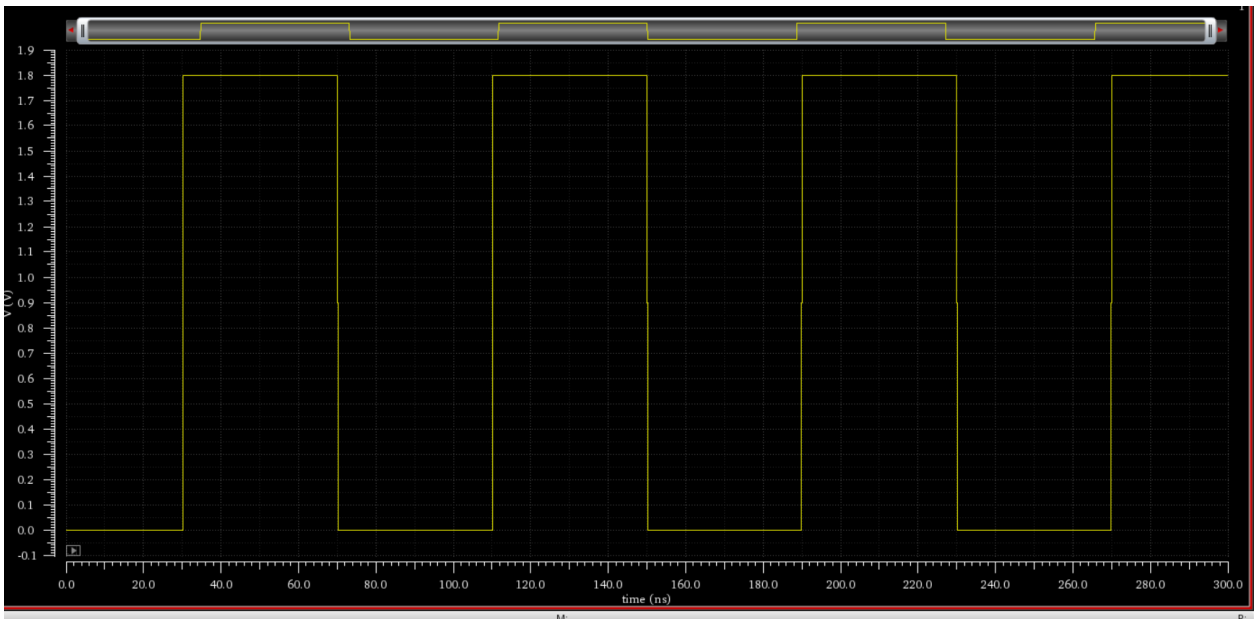
1.schematic



2.simulation waveform







本次作業學習心得：

透過本次 lab 我學習到 tool 操作，學習到基本 verilog A 之語法(雖然是參考講義撰寫)，學習到混合訊號數位類比轉換的 state 轉換情形，看到一堆波形有一種坐了時光機回到大二做電子實驗的感覺，不過也因為看到波形有了一些實感。

問題與討論：

1. tool 有時能用有時不能用:

   我發現當 tool 不正常中斷時會產生一個 cdclock 檔，把該檔案刪掉即可。

2. 波形大小不對:

   重新調整模擬時間調到剛好