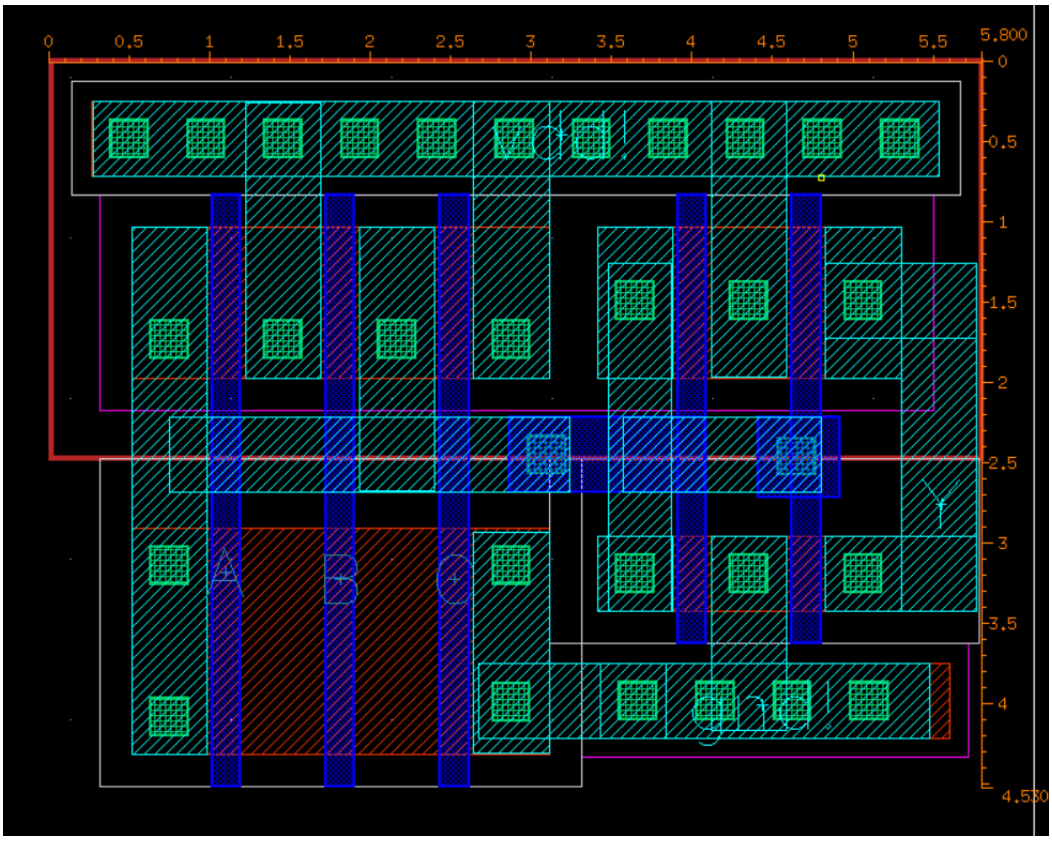
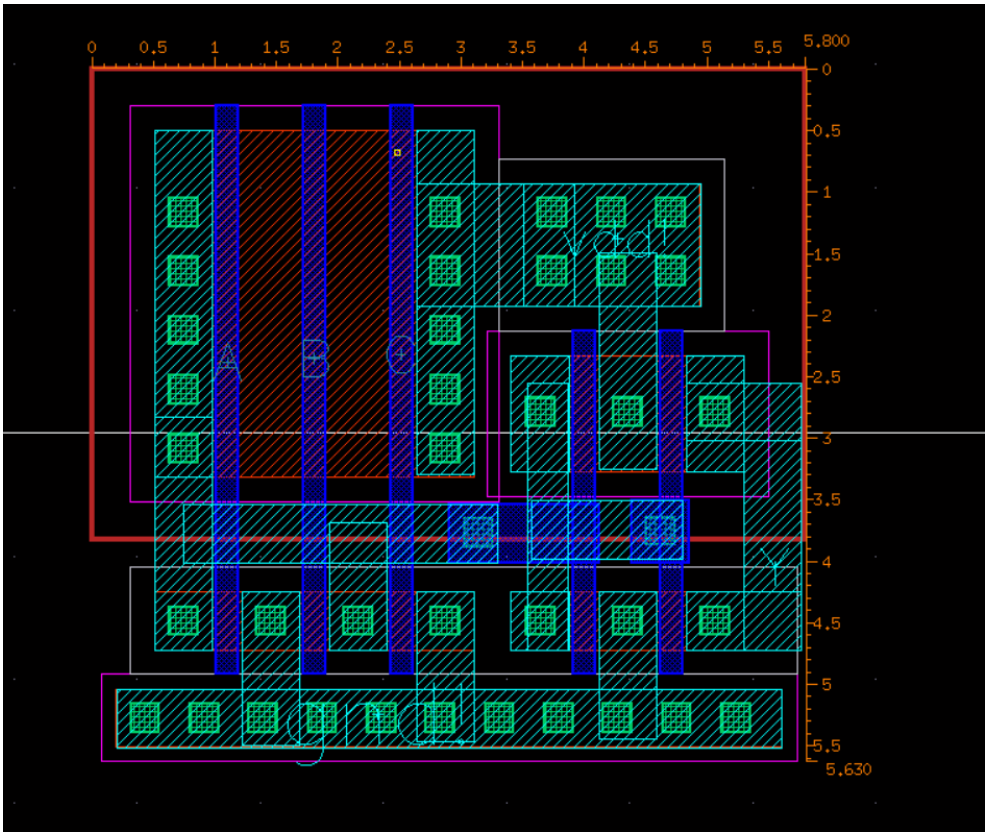
1.layout with ruler

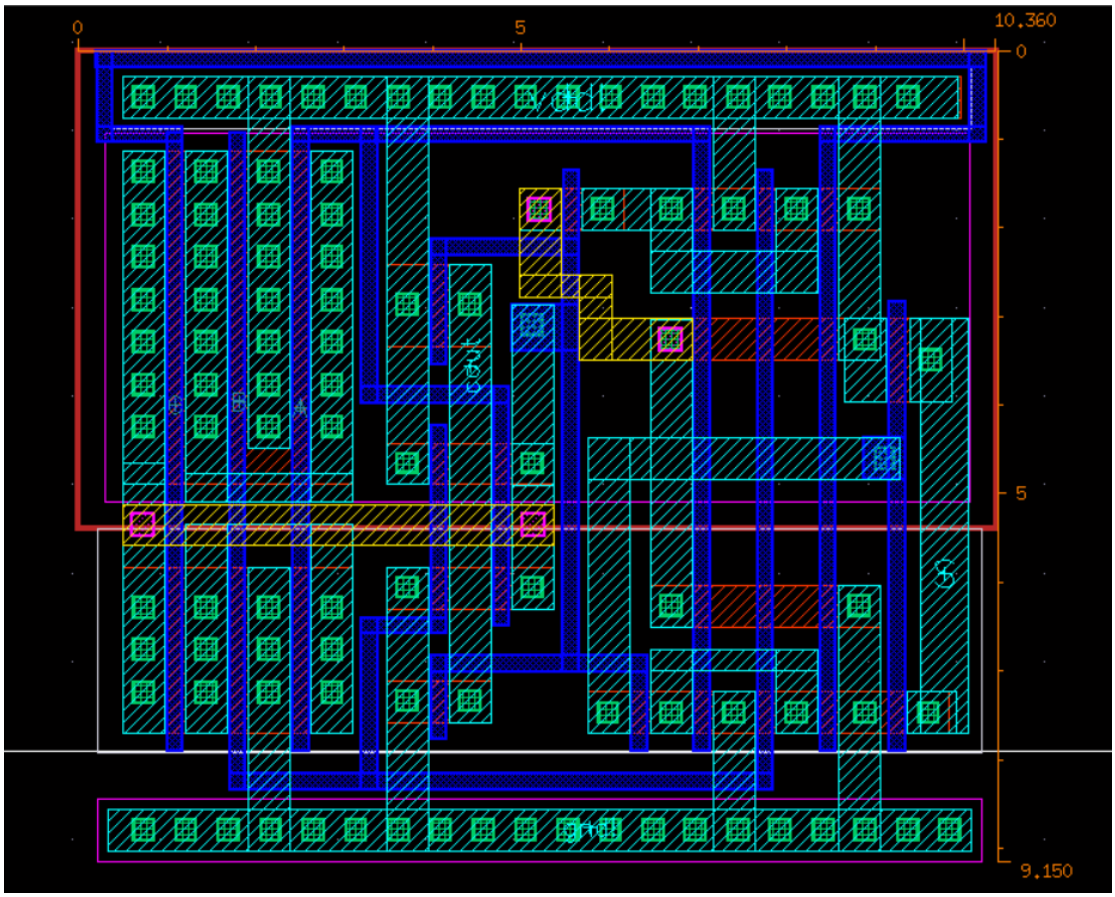
nand3 layout(5.8*4.53=26.274)



Nor3 layout(5.8*5.63=32.654)



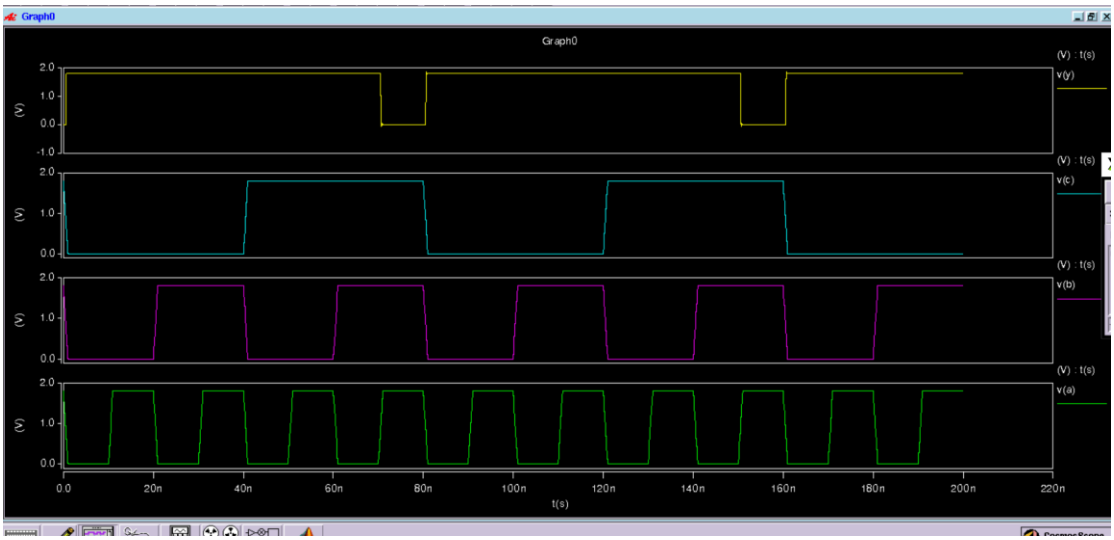
Fulladder layout(10.36*9.15=94.794)



2.Postsim wavefrom

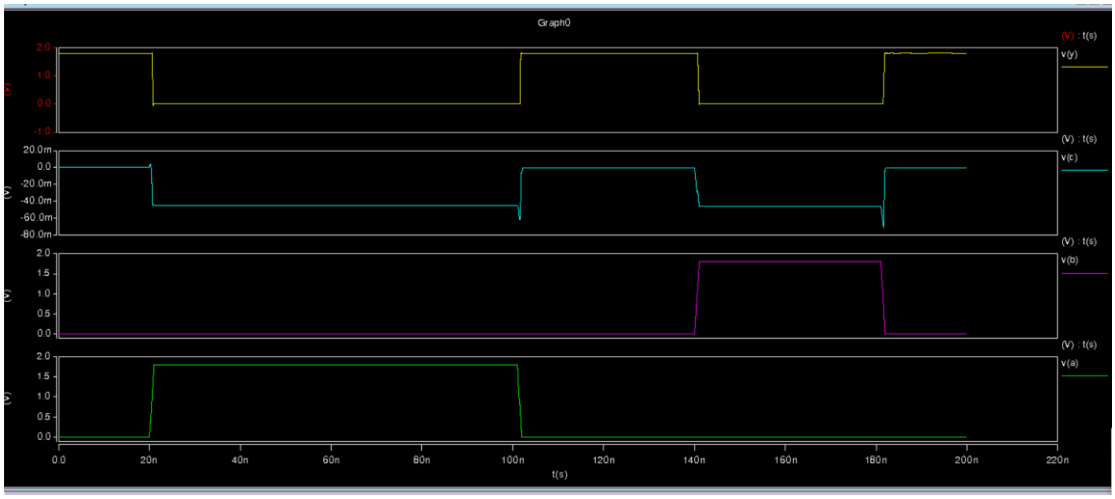
NAND3

Postsim:沒加任何東西



Nor3

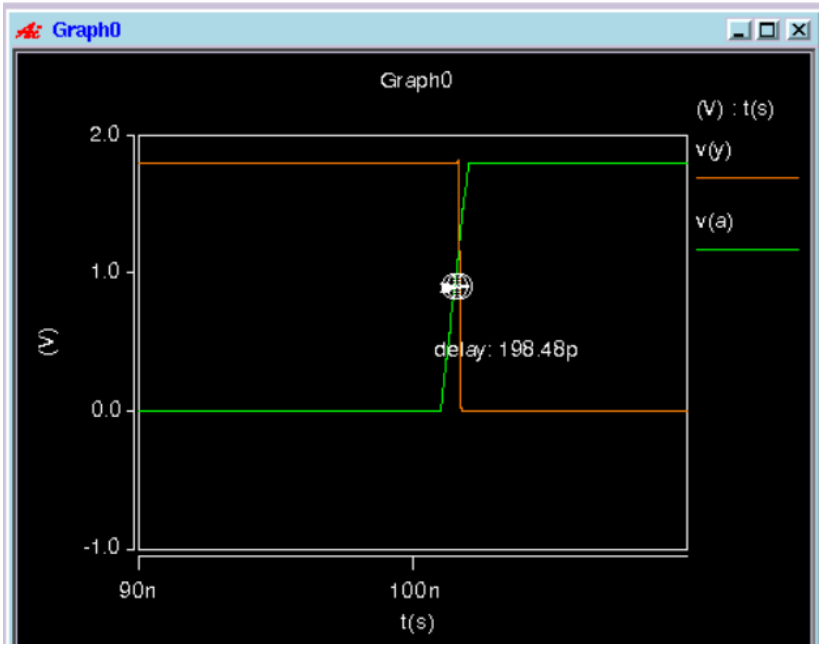
Postsim:沒加任何東西



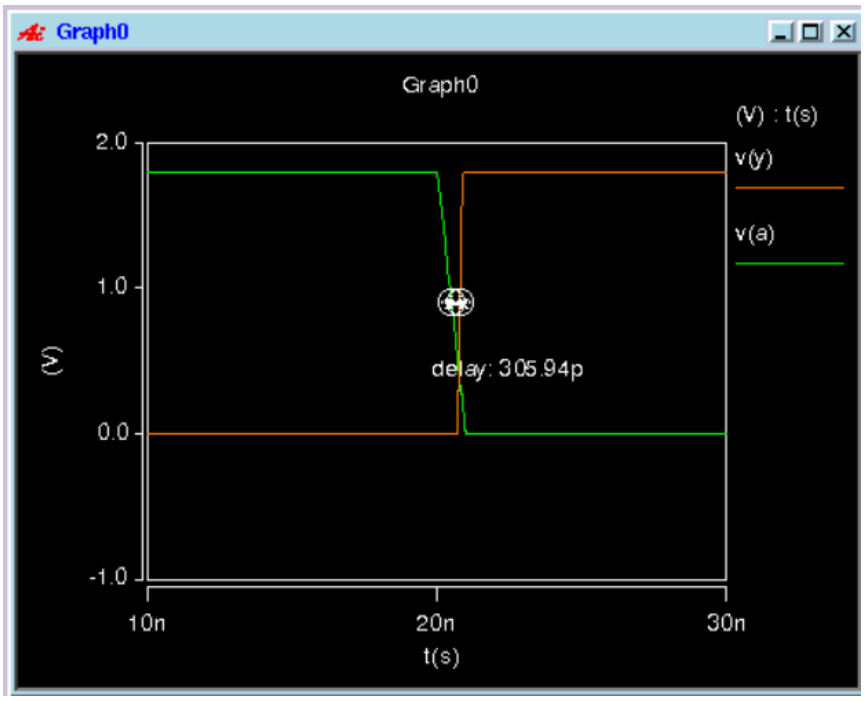
(1) NAND3 with inverter:

NAND3	Delay(an invertor)	Delay(FO4)
A up ($t_{pdr,A}$)	198.46p	220.87p
A down($t_{pdf,A}$)	305.94p	345.91p
B up($t_{pdr,B}$)	106.58p	102.77p
B down($T_{pdf,B}$)	315.51p	352.49p

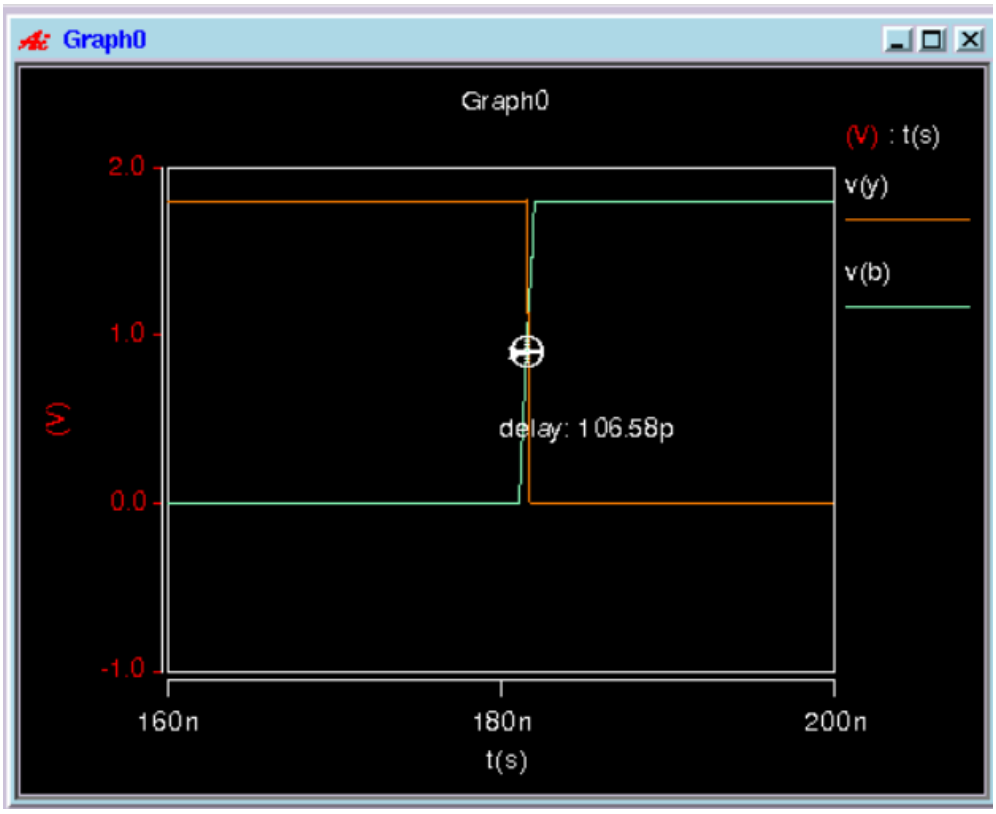
tdra:



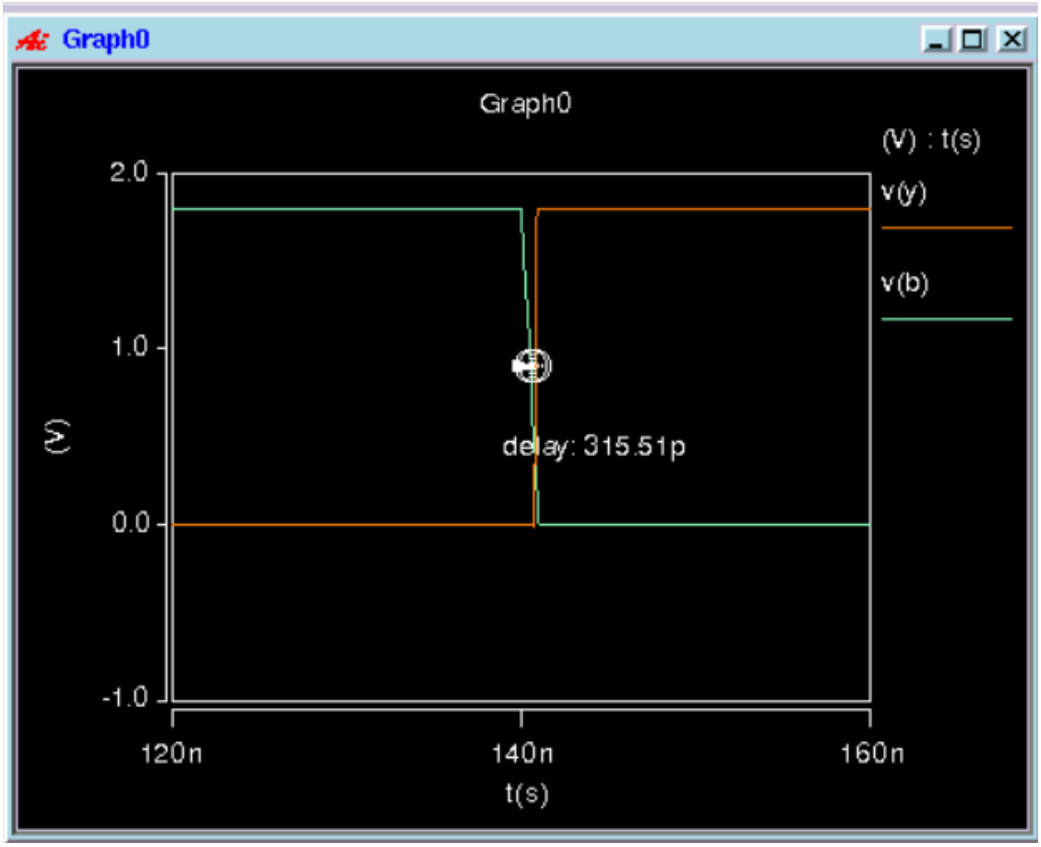
Tdfa:


Graph0
Graph0
(V) : t(s)
v(y)
v(a)
2.0
1.0
0.0
-1.0
(V)
delay: 305.94p
10n
20n
30n
t(s)

Tdrb:

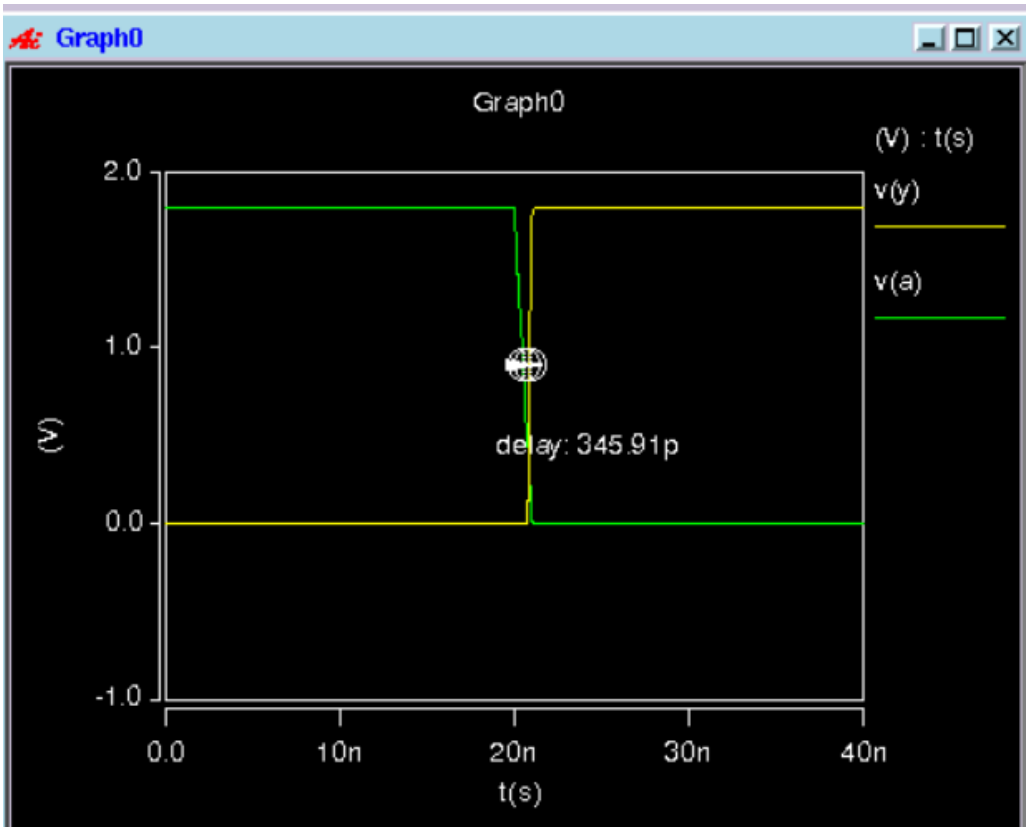

Graph0
Graph0
(V) : t(s)
v(y)
v(b)
2.0
1.0
0.0
-1.0
(V)
delay: 106.58p
160n
180n
200n
t(s)

Tdfb:

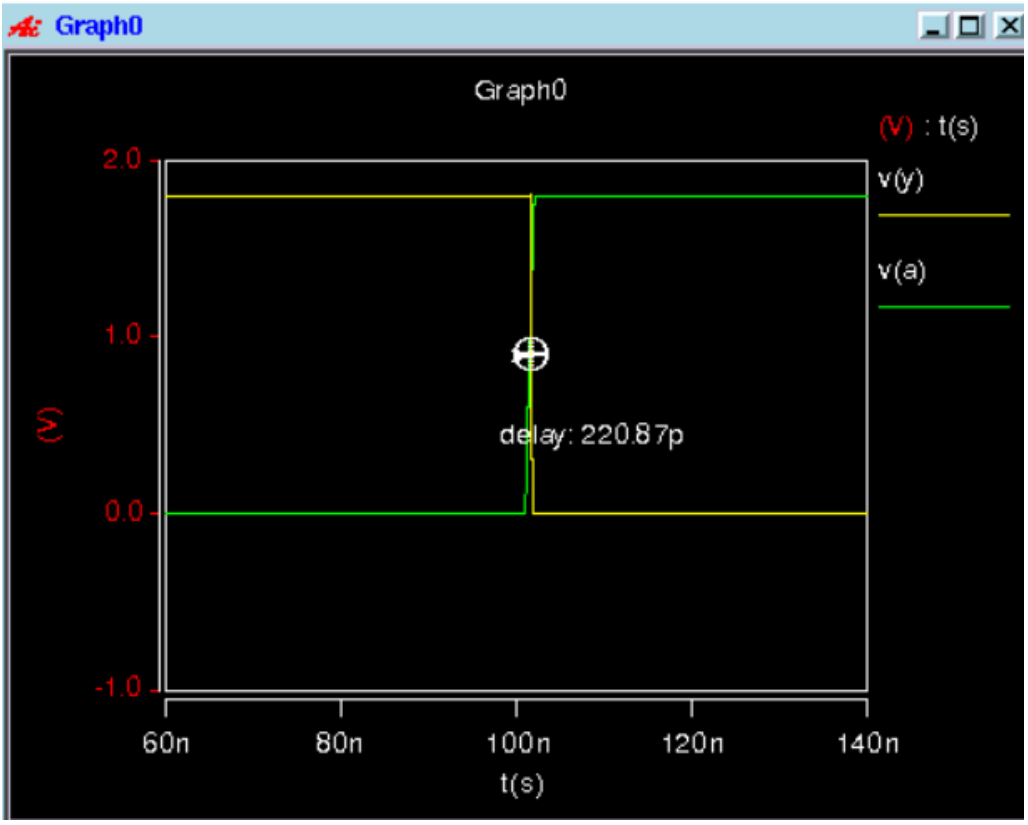


(2) NAND3 with fo4:

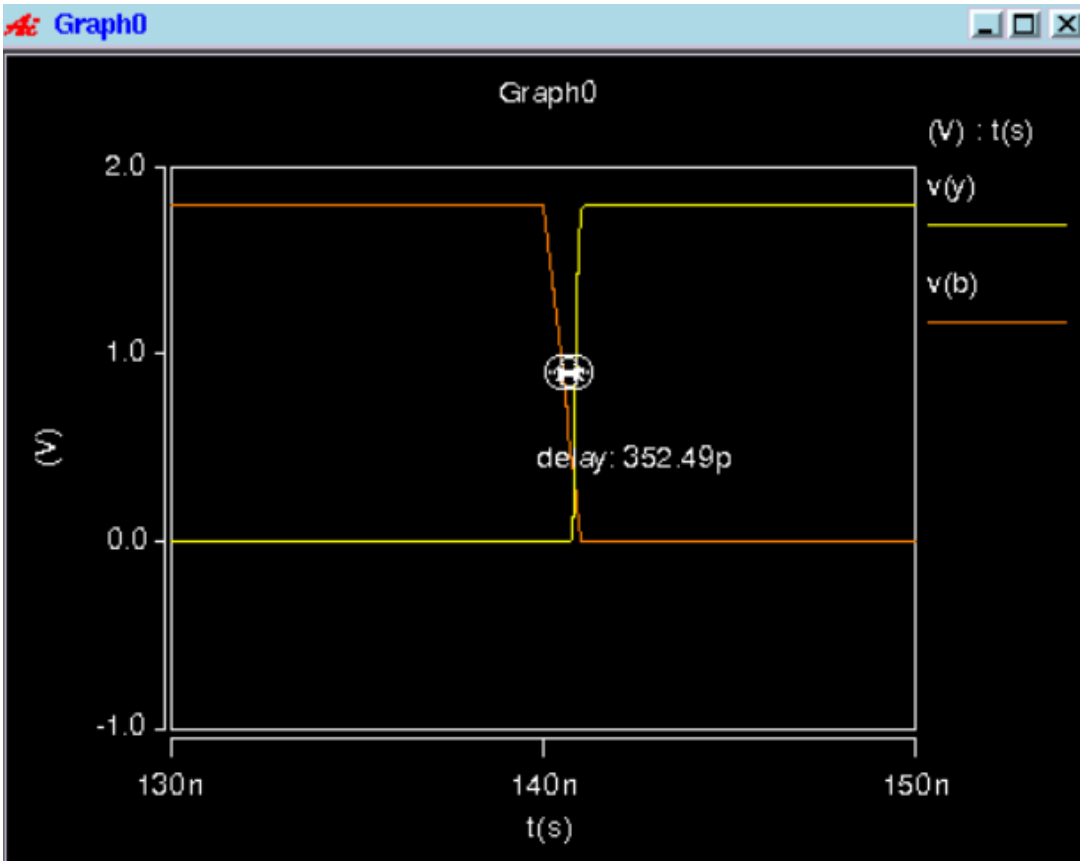
Tdfa:



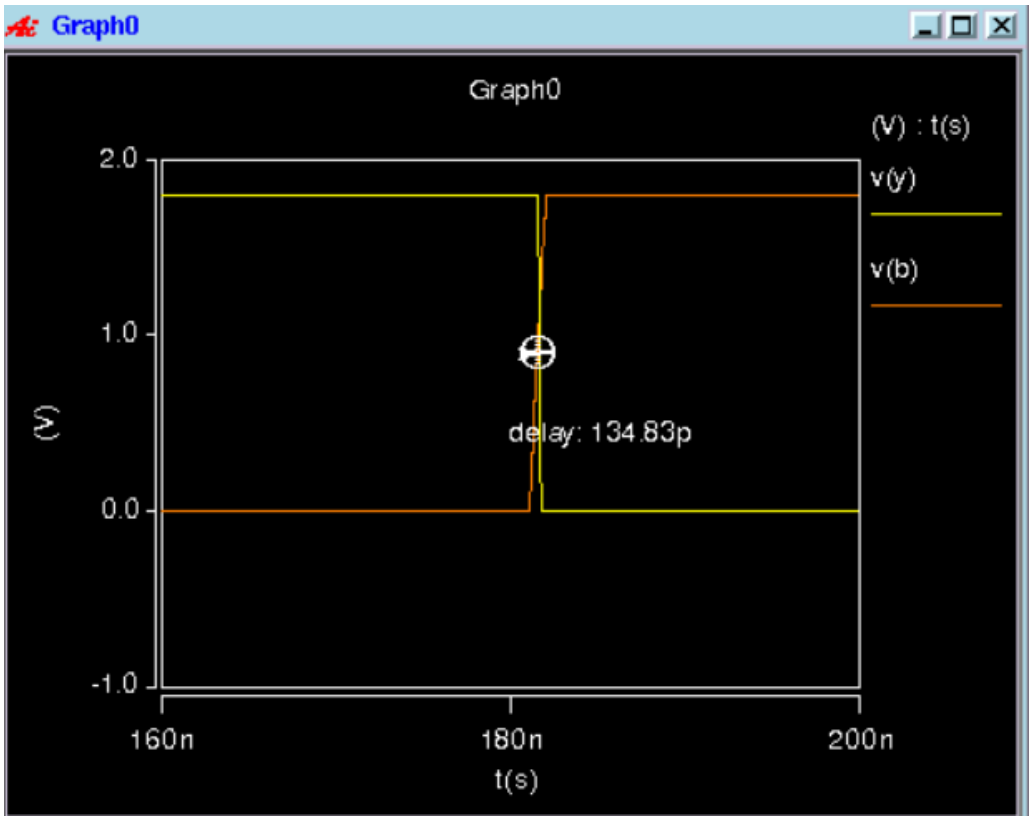
Tdra:


Graph0
Graph0
(V) : t(s)
v(y)
v(a)
2.0
1.0
0.0
-1.0
(V)
delay: 220.87p
60n
80n
100n
120n
140n
t(s)

Tdfb:


Graph0
Graph0
(V) : t(s)
v(y)
v(b)
2.0
1.0
0.0
-1.0
(V)
delay: 352.49p
130n
140n
150n
t(s)

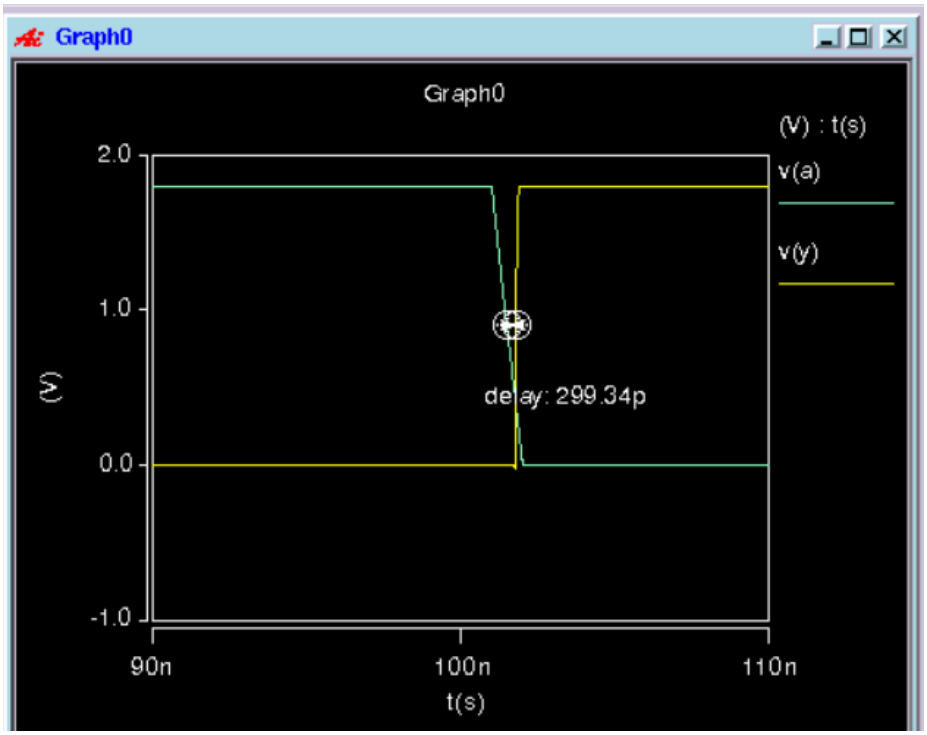
Tdrb:



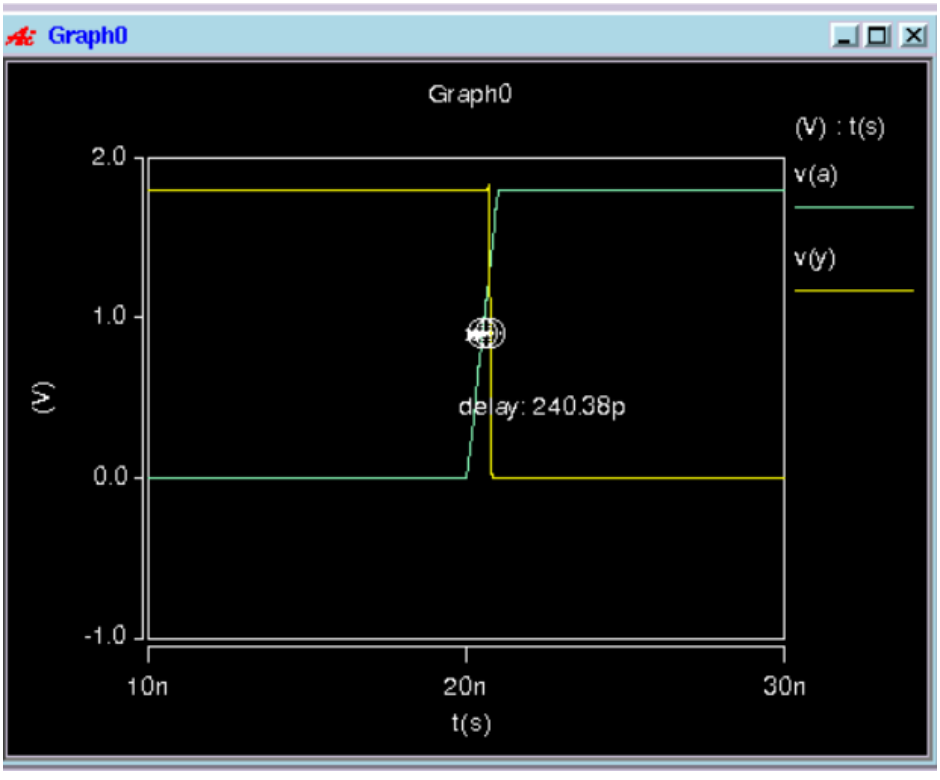
NOR	Delay(an invertor)	Delay(FO4)
A down($t_{pdf,A}$)	299.34p	327.36p
A up ($t_{pdr,A}$)	240.38p	267.51p
B down($T_{pdf,B}$)	215.33p	266p
B up($t_{pdr,B}$)	326.1p	280.69p

(3) NOR3 with inverter:

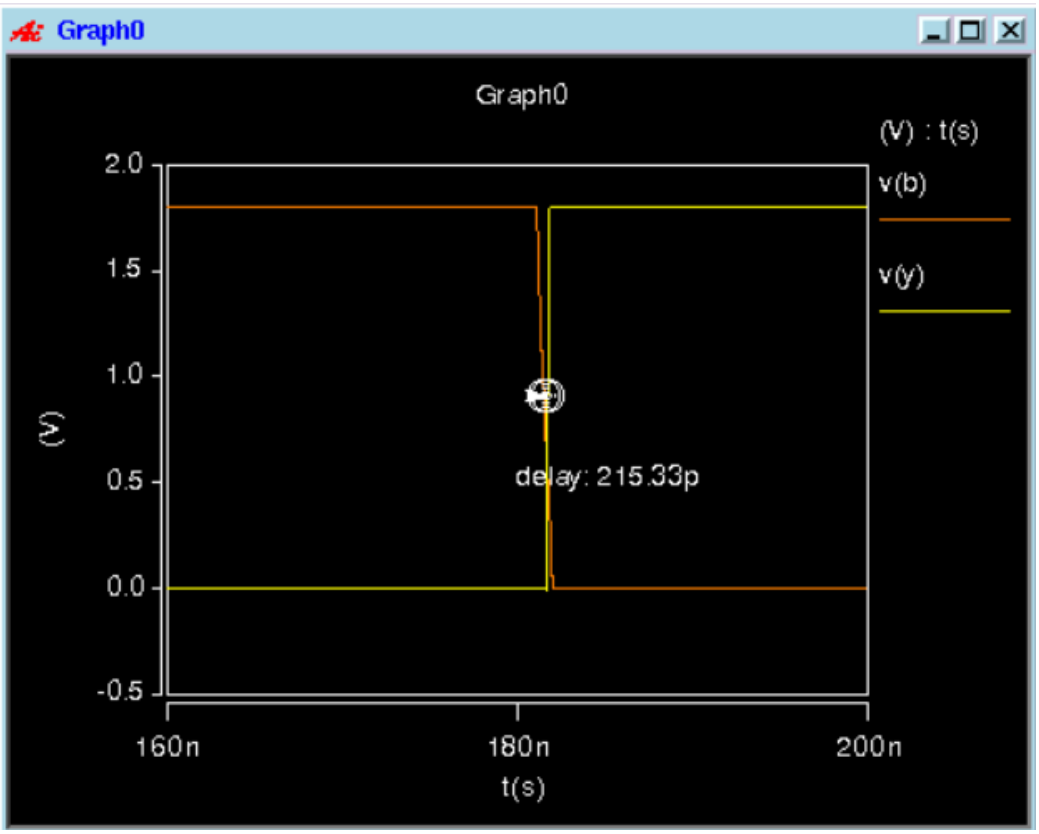
TdfA:


Graph0
Graph0
(V) : t(s)
v(a)
v(y)
2.0
1.0
0.0
-1.0
(V)
delay: 299.34p
90n
100n
110n
t(s)

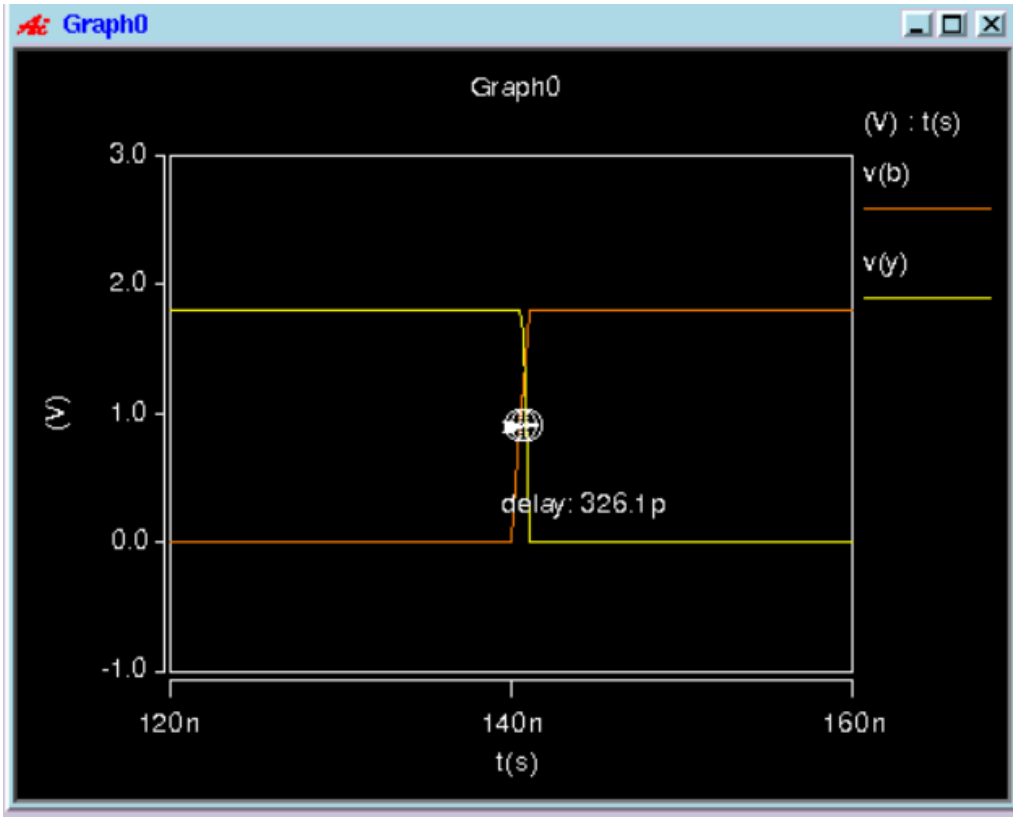
Tdra:


Graph0
Graph0
(V) : t(s)
v(a)
v(y)
2.0
1.0
0.0
-1.0
(V)
delay: 240.38p
10n
20n
30n
t(s)

Tdfb:

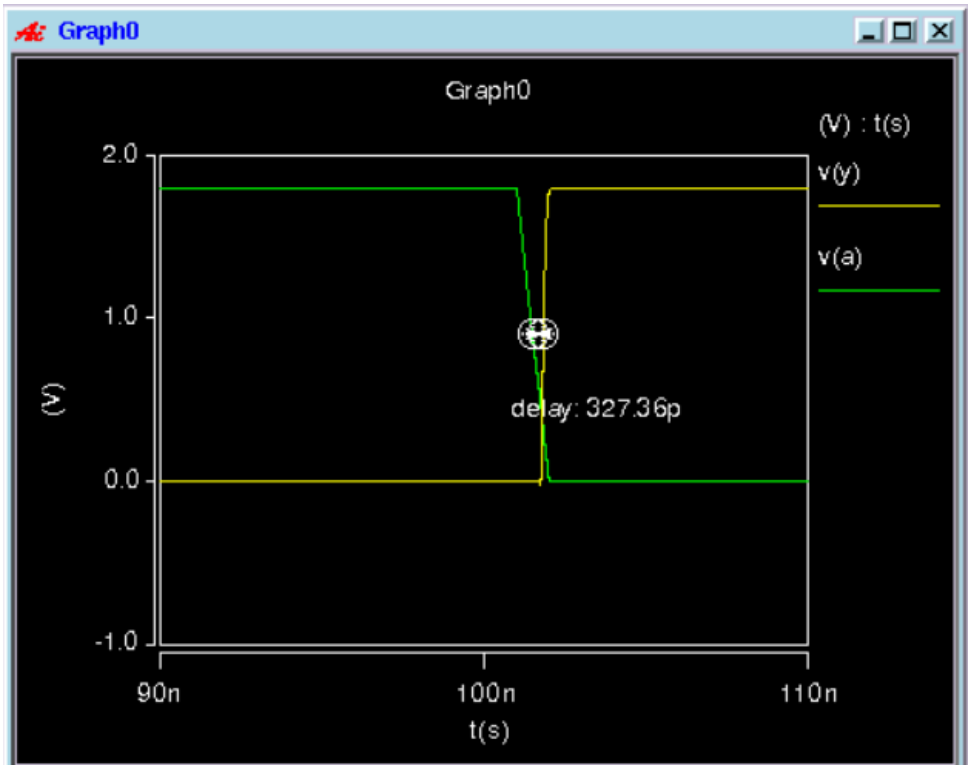


Tdrb:

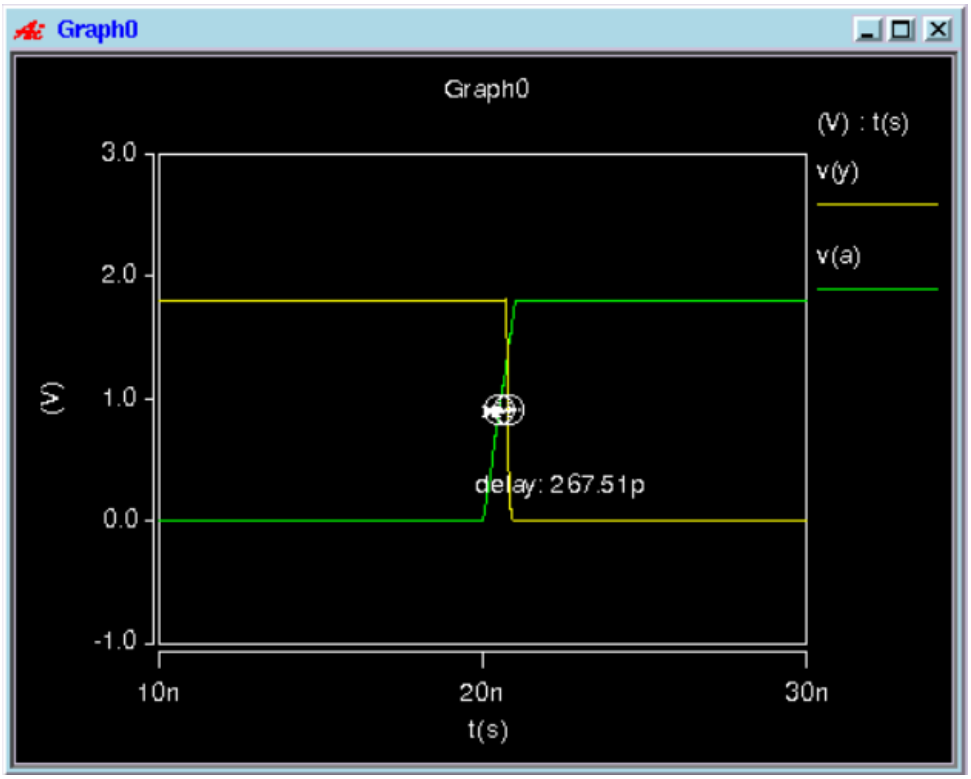


(4) Nor3 with fo4:

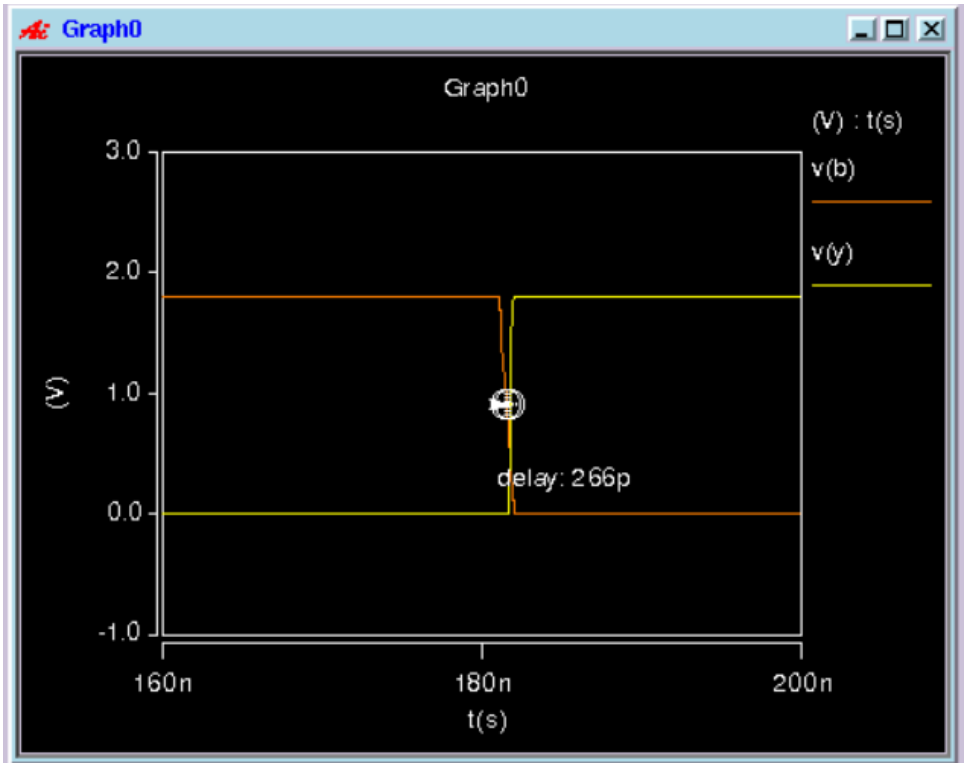
tdfa



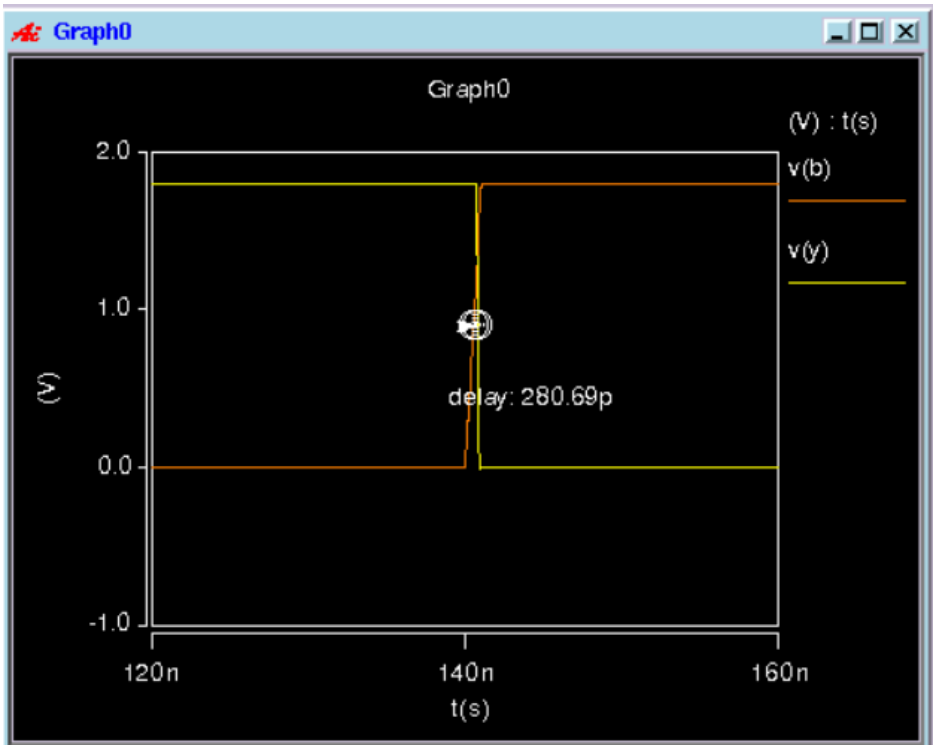
tdra



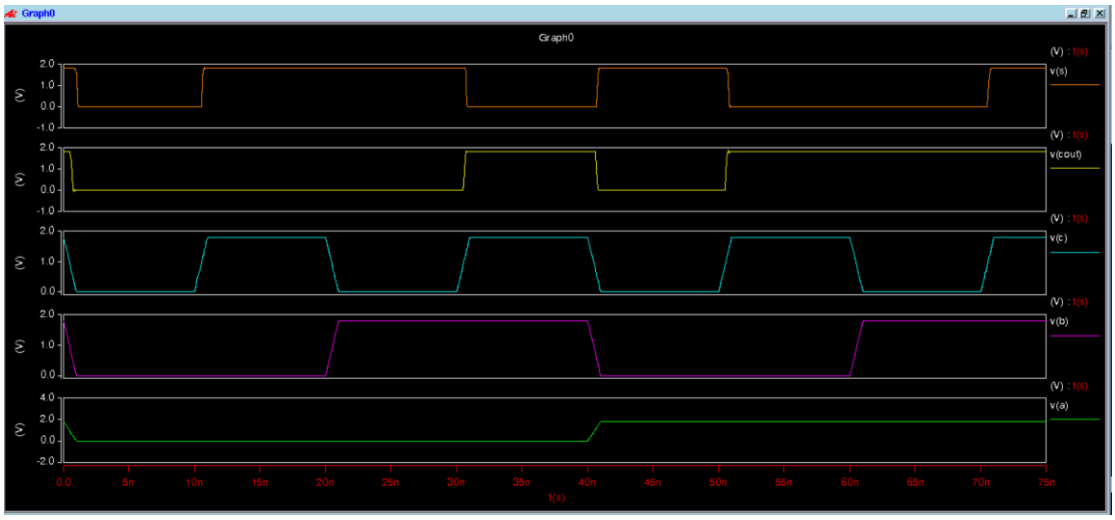
tdfb


Graph0
Graph0
(V) : t(s)
v(b)
v(y)
3.0
2.0
1.0
0.0
-1.0
(V)
delay: 266p
160n
180n
200n
t(s)

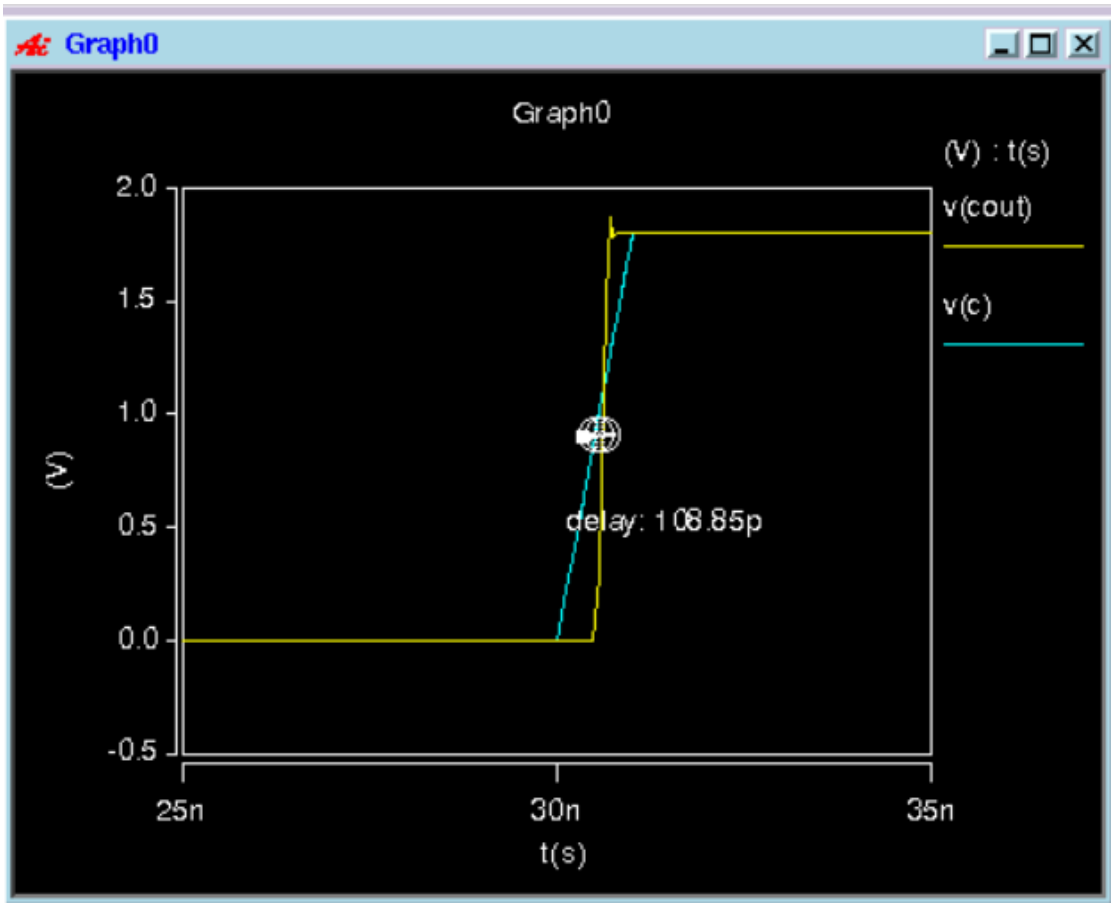
tdrb:

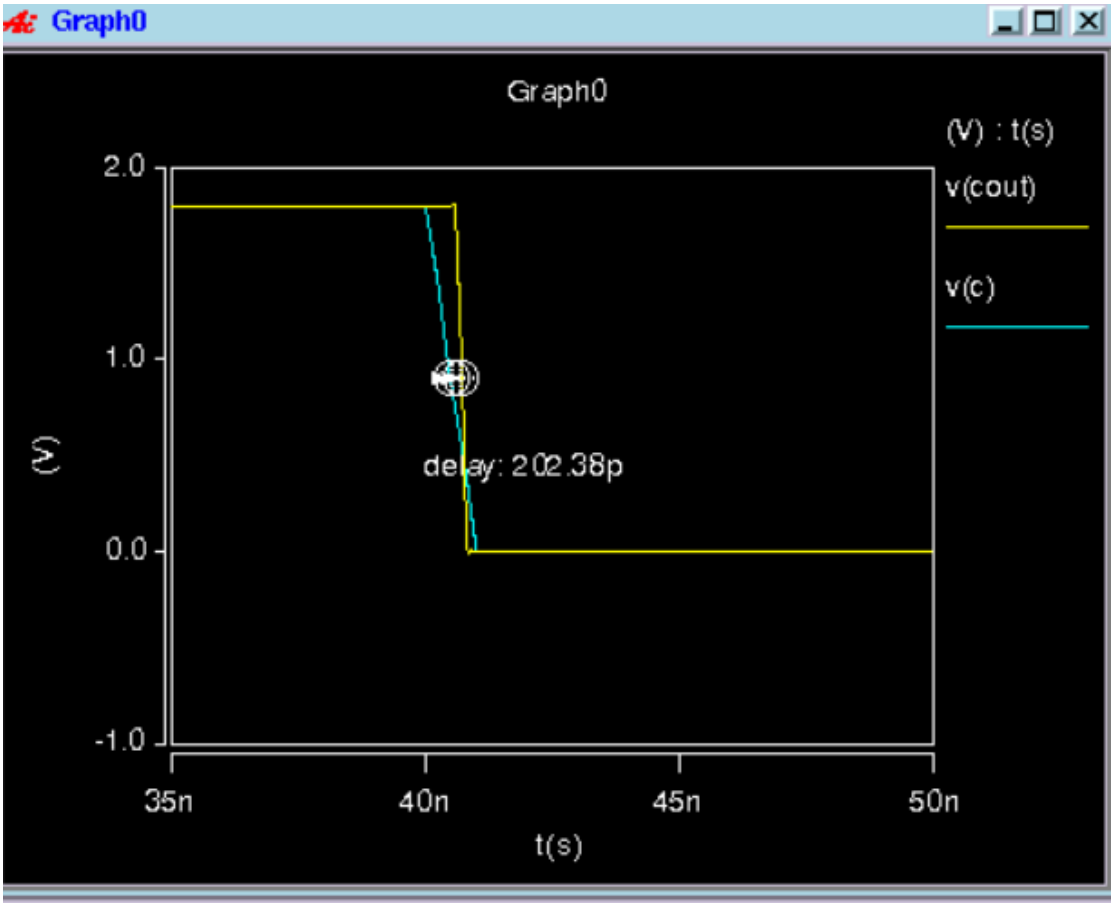

Graph0
Graph0
(V) : t(s)
v(b)
v(y)
2.0
1.0
0.0
-1.0
(V)
delay: 280.69p
120n
140n
160n
t(s)

Full-adder postsim:



Cin to cout delay:rising 108.85p falling:202.38p





3.NAND+NOR table

NAND3	Delay(an invertor)	Delay(FO4)
A up ($t_{pdr,A}$)	198.46p	220.87p
A down($t_{pdf,A}$)	305.94p	345.91p
B up($t_{pdr,B}$)	106.58p	102.77p
B down($T_{pdf,B}$)	315.51p	352.49p

NOR	Delay(an invertor)	Delay(FO4)
A down($t_{pdf,A}$)	299.34p	327.36p
A up ($t_{pdr,A}$)	240.38p	267.51p
B down($T_{pdf,B}$)	215.33p	266p
B up($t_{pdr,B}$)	326.1p	280.69p

power

Nand3 power:

```
******
**sim_nand3

 ******  transient analysis tnom=  25.000 temp=  25.000 *****
total_cur= 266.0303f  from=   0.          to= 200.0000n
total_pwr= 478.8546f
```

Nor3 power:

```
******
**sim_nor3

 ******  transient analysis tnom=  25.000 temp=  25.000 *****
total_cur= 313.7698f  from=   0.          to= 200.0000n
total_pwr= 564.7857f
```

Fulladder power:

```
******
**sim_fadd3

 ******  transient analysis tnom=  25.000 temp=  25.000 *****
total_cur=   1.0113p  from=   0.          to= 200.0000n
total_pwr=   1.8203p
```

4.question of the lab:

加了兩個反向器的電路相比於加了 FO4 的有較少的 delay time，因為 FO4 有著多四倍的電容，所以較費時。