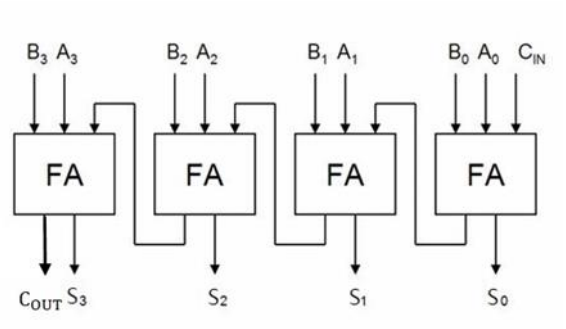
VLSI Lab4

I. Design a 4-bit carry-ripple adder.

A. You can use your 1-bit full adder in Lab2 to realize a 4-bit carry-ripple adder. (You need to add inverter as loading.)



B. Show a waveform to verify your design (set the input as below).

Measure $Delay_{CinToCout}$

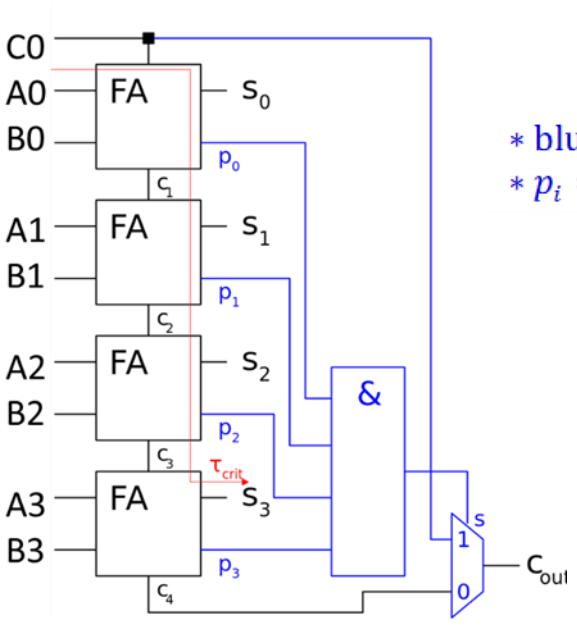
Pattern	C_{IN}	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
1	0	0	1	0	1	1	0	0	1
2	1	0	0	0	0	1	1	1	1

Rise time = 1ns
Fall time = 1ns

C. Measure Area, $Delay_{Cin\ to\ Cout}$ of the circuit.

II. Design a 4-bit carry-skip adder.

A. Add skip logic to your 4-bit carry-ripple adder to realize a 4-bit carry skip adder. (You need to add inverter as loading.)



* blue part is skip logic
* $p_i = A_i \oplus B_i$

B. Show a waveform to verify your design (set the input as below).

Measure $Delay_{CinToCout}$

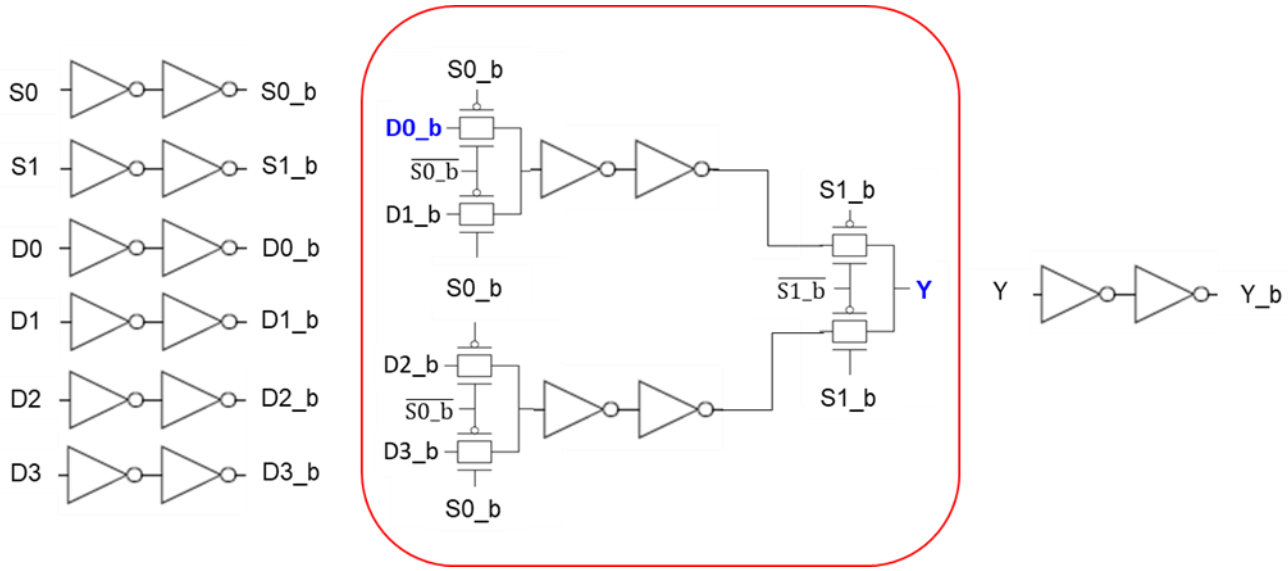
Pattern	C_{IN}	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
1	0	0	1	0	1	1	0	0	1
2	1	0	0	0	0	1	1	1	1

Rise time = 1ns
Fall time = 1ns

C. Measure Area, $Delay_{Cin\ to\ Cout}$ of the circuit.

III. Design a 4:1 MUX using transmission gates.

A. Use transmission gates to realize a 4:1 MUX as figure below. (You need to add inverter as loading.)

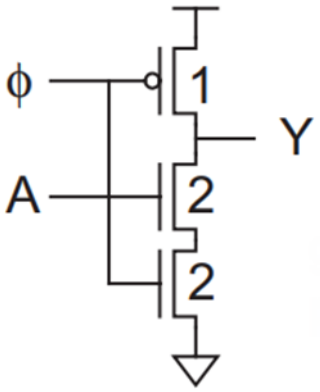


B. Show a waveform to verify your design

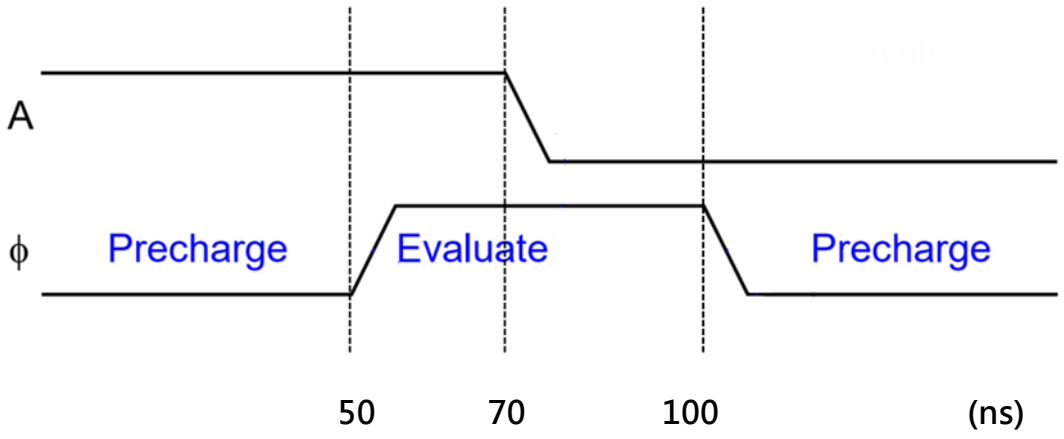
C. Measure Area, Delay$_{D0_b\ to\ Y}$ of the circuit.

IV. Design a dynamic inverter

A. Design a dynamic footed inverter. (You need to add inverter as loading.)

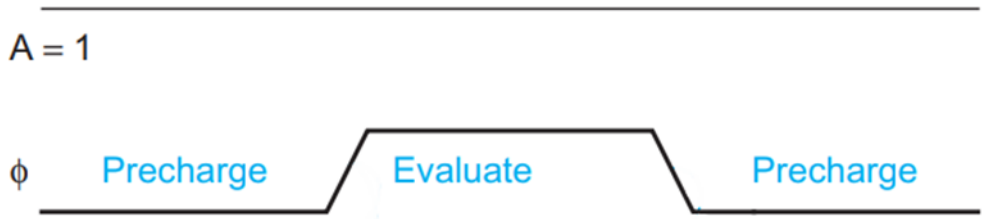


B. Show a waveform to verify your design (set the input as below)



C. Measure Area, $Delay_{\Phi \text{ to } Y}$ of the circuit.

- Φ toggle every 50 ns
- Rise time and fall time are 1 ns
- Set A to 1.8V



V. Questions of the lab

A. Compare the $Delay_{Cin\ To\ Cout}$ between 4-bit carry-ripple adder and 4-bit carry-skip adder, and explain the reason of the difference.

B. Discuss what are the benefits using transmission gates to realize a 4:1 MUX, and explain the reasons.

C. What is “Monotonicity Problem” and how can we resolve this problem?

VI. Grading policy

A. Pre-sim waveform: 16%

i. 4-bit carry-ripple adder 4%
ii. 4-bit carry-skip adder 4%
iii. 4:1 MUX 4%
iv. Dynamic inverter 4%

B. DRC & LVS: 32%

i. 4-bit carry-ripple adder 8%
ii. 4-bit carry-skip adder 8%
iii. 4:1 MUX 8%
iv. Dynamic inverter 8%

C. Post-sim waveform: 16%

i. 4-bit carry-ripple adder 4%
ii. 4-bit carry-skip adder 4%
iii. 4:1 MUX 4%
iv. Dynamic inverter 4%

D. Performance: 16%

i. 4-bit carry-ripple adder 5%

$$\boldsymbol{Figure\ of\ Merit\ (FoM) = Delay_{CinToCout} \times Area}$$

ii. 4-bit carry-skip adder 5%

$$\boldsymbol{Figure\ of\ Merit\ (FoM) = Delay_{CinToCout} \times Area}$$

iii. 4:1 MUX 3%

$$\boldsymbol{Figure\ of\ Merit\ (FoM) = Delay_{D0\_bToY} \times Area}$$

iv. Dynamic inverter 3%

$$Figure\ of\ Merit\ (FoM) = t_{\Phi \to Y} \times Area$$

E. Report: 20%

i. Layout screenshot with ruler: 4%
   1. 4-bit carry-ripple adder 1%
   2. 4-bit carry-skip adder 1%
   3. 4:1 MUX 1%
   4. Dynamic inverter 1%

ii. Post-sim waveform: 4%
   1. 4-bit carry-ripple adder 1%
   2. 4-bit carry-skip adder 1%
   3. 4:1 MUX 1%
   4. Dynamic inverter 1%

iii. Questions of the lab: 12%

VII. Demo time

12/9 (Wed.) 15:30 ~ 18:30

You only have “one” chance to demo!

After deadline, any requests for demo are denied.

VIII. Report hand-in deadline

12/9 (Wed.) 23:59 on New E3

After deadline, any requests for handing in report are denied.

IX. Appendix

Power measurement by Hspice

```
.tran 0.1n 200n
.meas tran total_cur integ par('-i(vvdd)')
.meas tran total_pwr param='1.8*total_cur'
```