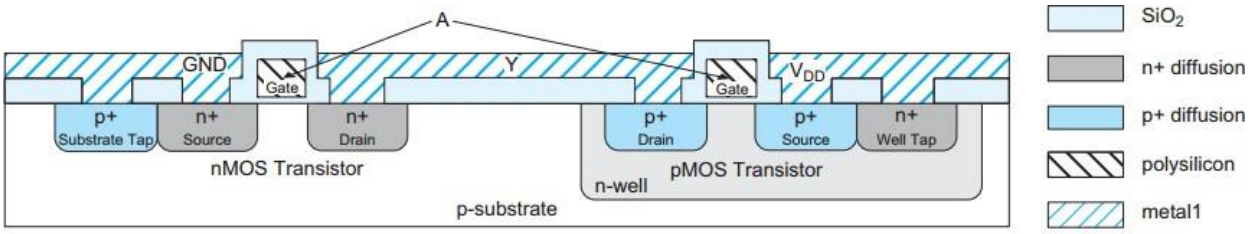
VLSI Lab1

I. Design an inverter with constraints given blow

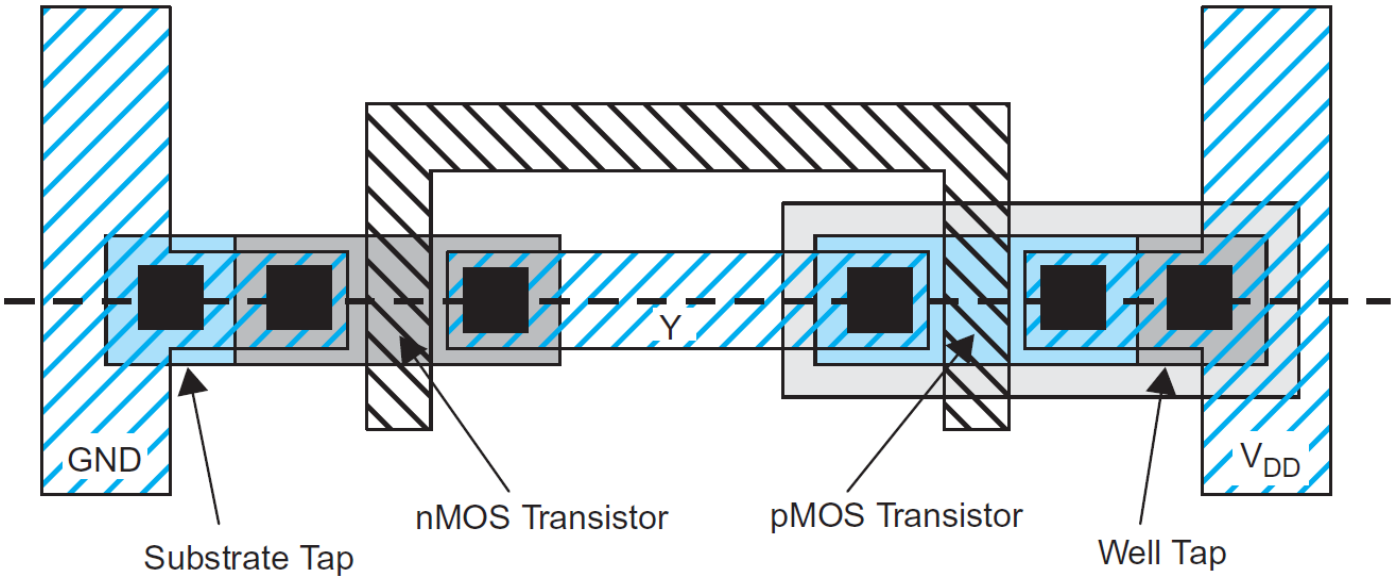
Use PMOS W/L = 0.94um / 0.18um, NMOS W/L = 0.47um / 0.18um as the size of inverter.

A. Layout architecture of inverter

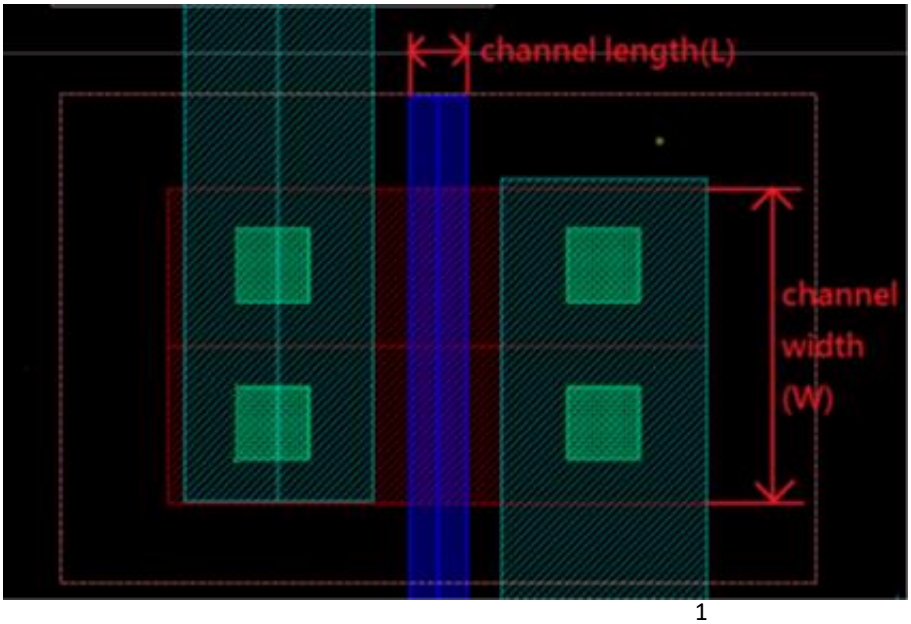
The Layout is based on the following architecture:

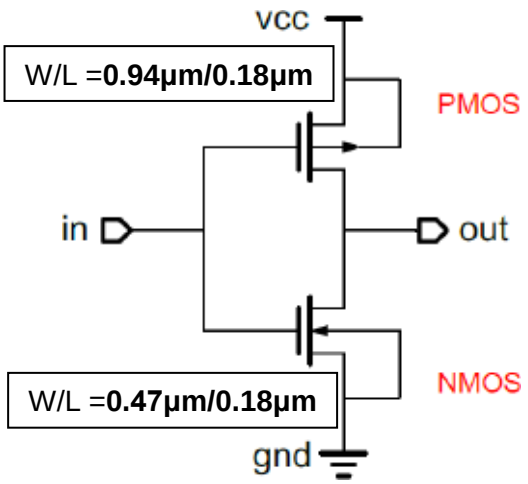


↑ Inverter cross-section with well and substrate contacts [from Fig.1.34 on P.20]



↑ Inverter mask set [from Fig.1.35(a) on P.21]





Component of inverter:

NWELL is used to define the region of PMOS.

PIMP/NIMP is used to define whether the diffusion is P-type or N-type.

DIFF is used to define type of diffusion for Source/Drain, also define active/isolation (or field) regions

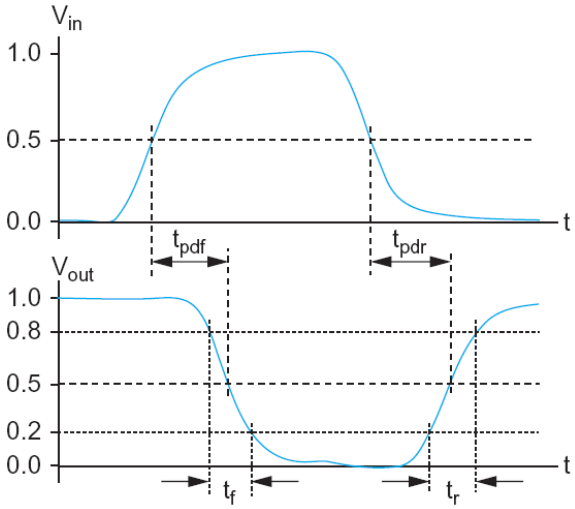
POLY is gate material over diff, defining W and L of transistor.

METAL is used to connect different components.

M1_TEXT is used to set the name of input, output and supply source.

CONT is used to define where the source, drain, gate, and tap are contacted to higher levels.

B. Waveform & Layout of inverter



t_{pdr}: rising propagation delay
- From input to rising output crossing VDD/2

t_{pdf}: falling propagation delay
- From input to falling output crossing VDD/2

t_r: rise time
- From output crossing 0.2 VDD to 0.8 VDD

t_f: fall time
- From output crossing 0.8 VDD to 0.2 VDD

Propagation delay and rise/fall times [from Fig. 3.1 on P.99]

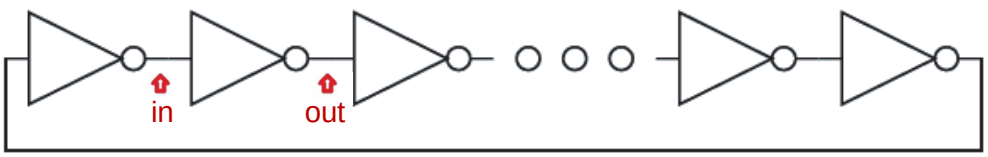
Assume that **rising time and falling time are both 1ns**, and delay time is 0ns.

Using **cscope** to **measure the propagation-delay time** of waveforms, the reason is that it will add extra resistance and capacitance when loading another inverter. Although the delay of loading part is larger, the waveform of that is more stable, almost no glitch exists in the waveform.

II. Design an N-inverter ring oscillator with the following constraints:

A. PMOS size: NMOS size = 2:1

B. N=31



Don't forget to set **initial condition** when simulating ring oscillator!
e.g.: .ic in = 1.8v

III. Questions of the lab

A. The pMOS transistor requires an n-type body region. However, we only have n-substrate wafers in fabrication process nowadays. How do we build pMOS on p-substrate wafers?

B. Why we set PMOS size: NMOS size = 2:1?

IV. Grading Policy

I. Pre-sim waveform: 10% (inverter 5% + ring oscillator 5%)

II. DRC pass: 20% (inverter 10% + ring oscillator 10%)

- Metal 3 ~ Metal 6 are **forbidden** to use in this lab.

III. LVS pass: 20% (inverter 10% + ring oscillator 10%)

IV. Post-sim waveform: 10% (inverter 5% + ring oscillator 5%)

V. Performance of Post-sim: 30% (inverter 15% + ring oscillator 15%)

Minimum power by itself is not an interesting objective because it is achieved as the delay for a computation approaches infinity and nothing is accomplished. The time for a computation must be factored into the analysis. Therefore, we use **power-delay product (PDP)** to evaluate performance of your layout.

1. Inverter:

$$Figure\ of\ Merit\ (FoM) = Power \times \frac{t_{pdr} + t_{pdf}}{2} \times Area$$

2. Ring oscillator:

$$Figure\ of\ Merit\ (FoM) = Power \times t_{period} \times Area$$

For both FoM, the lower FoM means the better performance.

VI. Report: 10%

1. Layout with **ruler** on it & Area: 4% (inverter 2% + ring oscillator 2%)
2. Questions: 6% (each question 3%)

V. Demo time: 10/07 (Wed.) 15:30 ~ 18:30

- After deadline, any requests for demo or turning in report are denied.

VI. Appendix

A. Input pattern for inverter

```
Vin in 0 pulse(0 1.8v 0 1n 1n 49n 100n)
```

1(node) should connect to input of 1st inverter.

B. Power measurement by HSpice in this lab

```
.tran 1n 1u
.meas tran total_cur integ par('-i(vvdd)')
.meas tran total_pwr param='1.8*total_cur'
```

'vvdd' is element name of power supply.