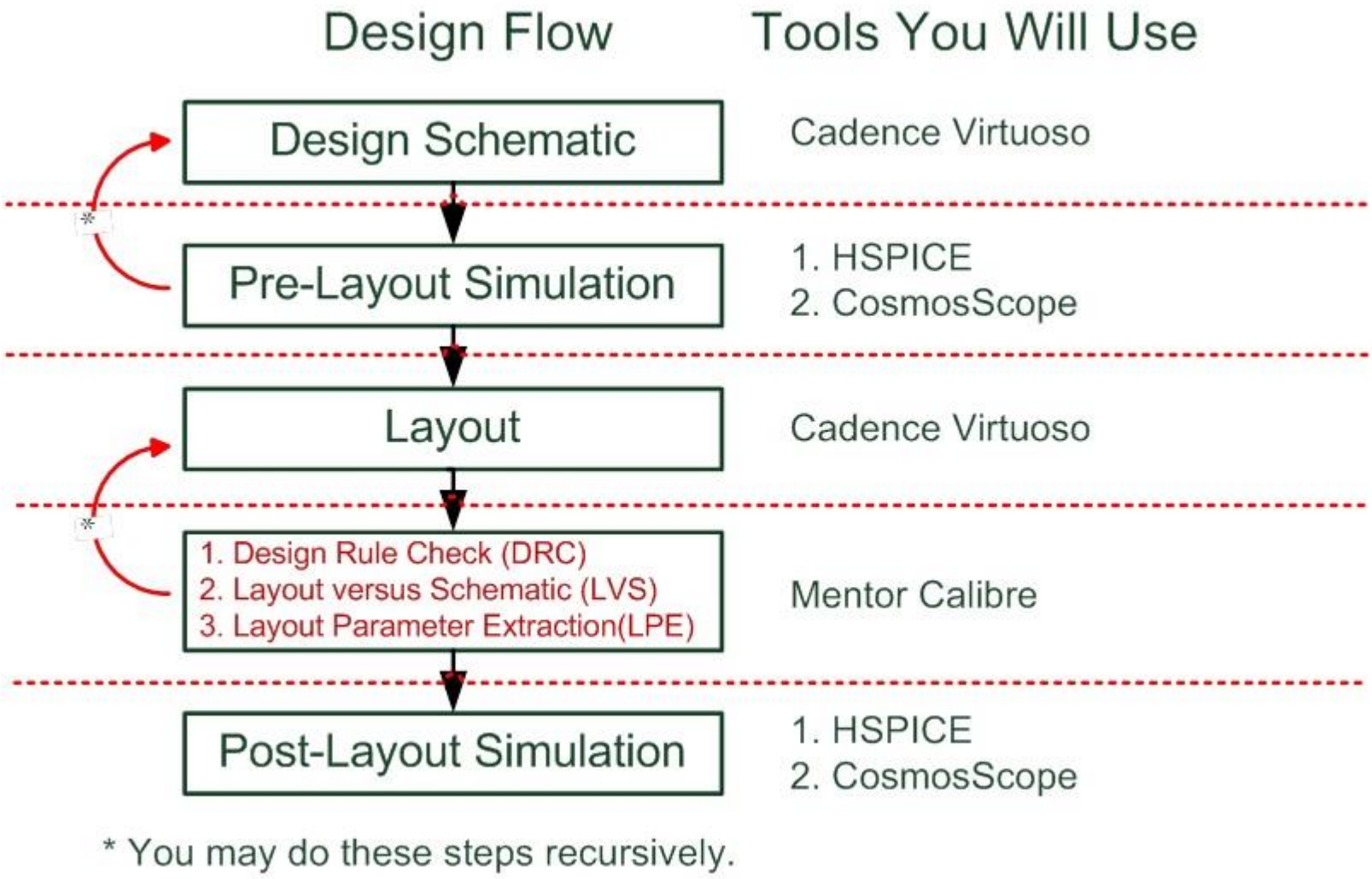
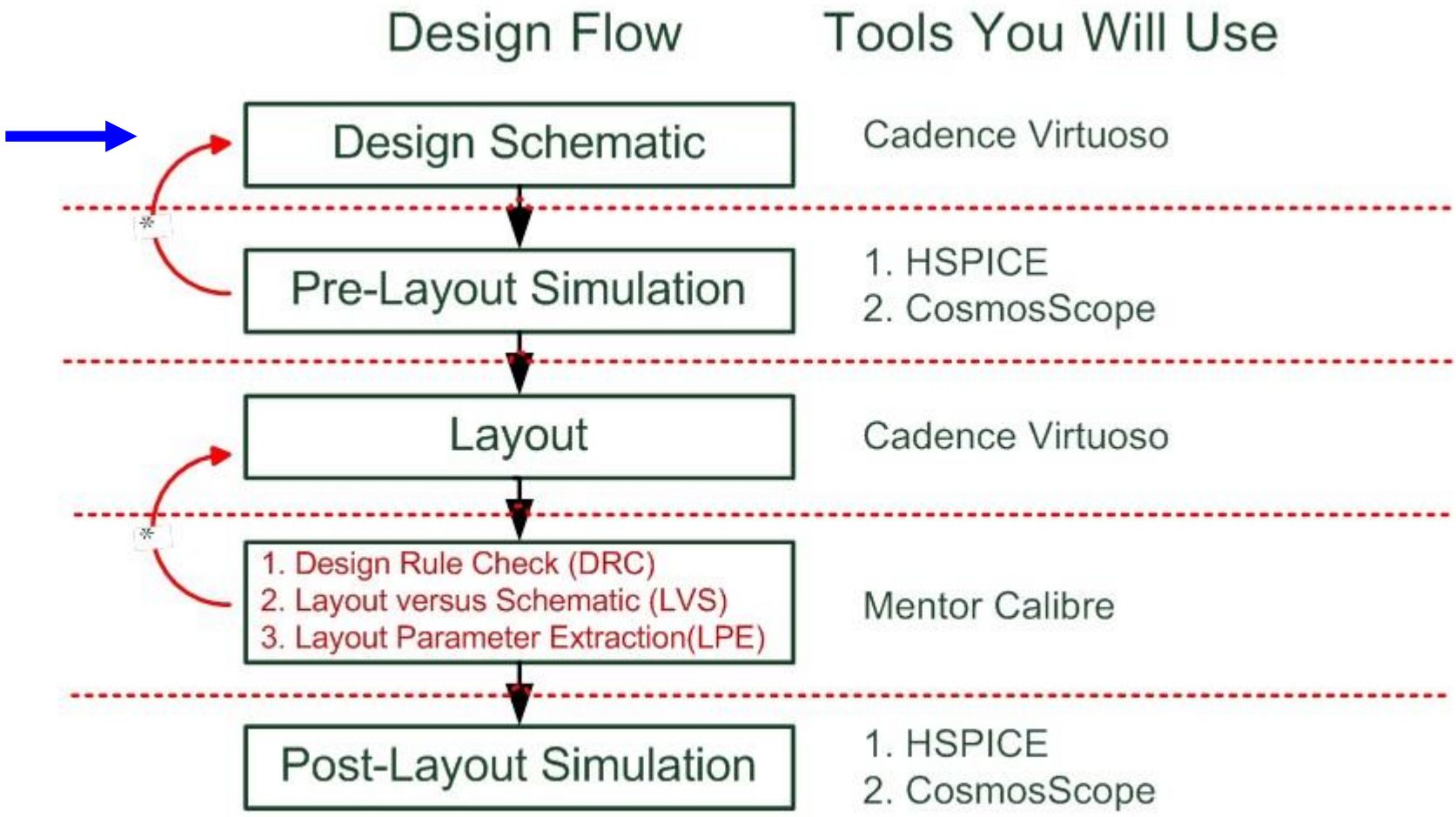
VLSI Lab Tutorial

Instructor: Prof. Herming Chiueh

Design Flow of Full-Custom Chip

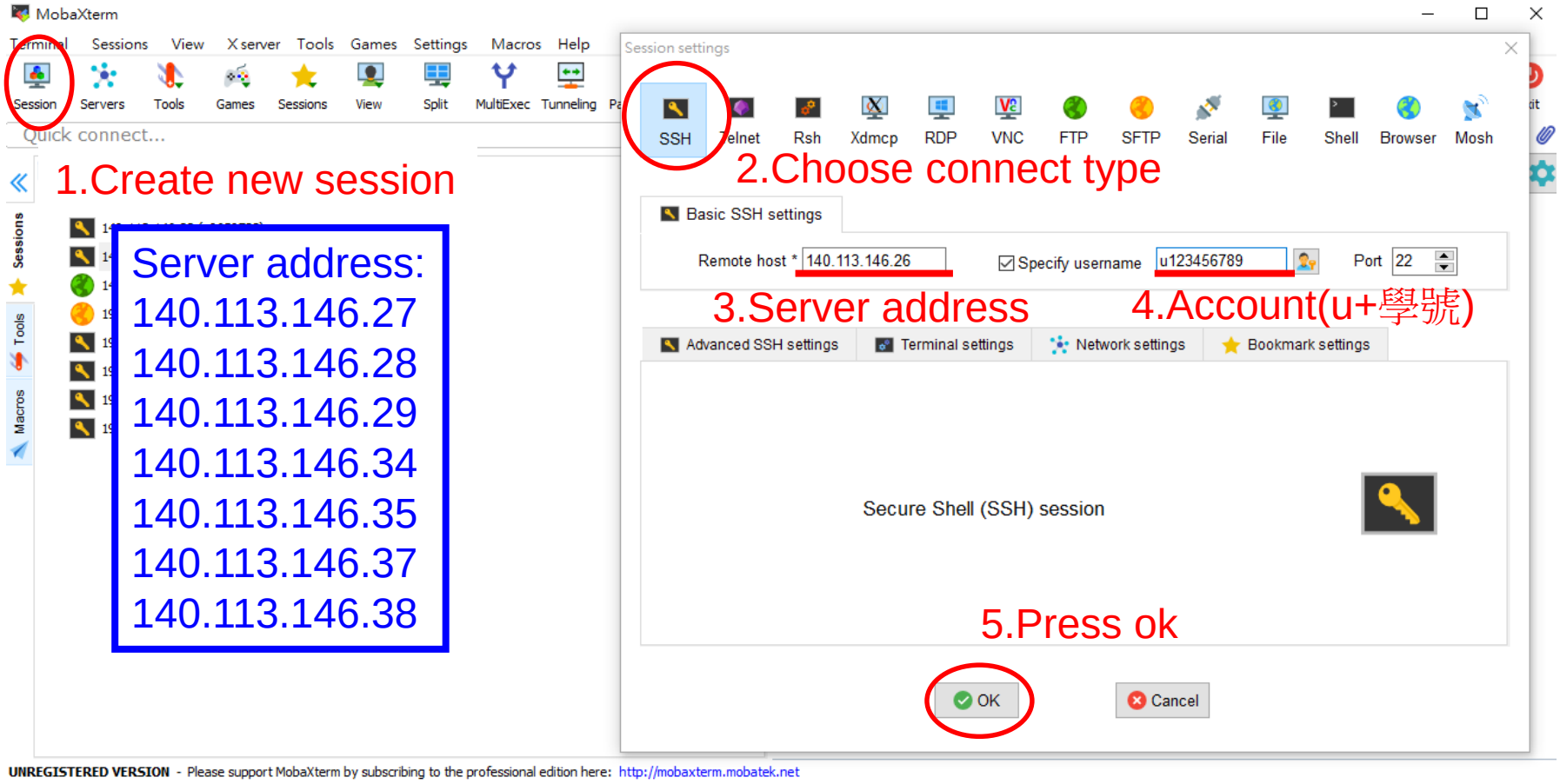


Design Flow of Full-Custom Chip



Setting Environment

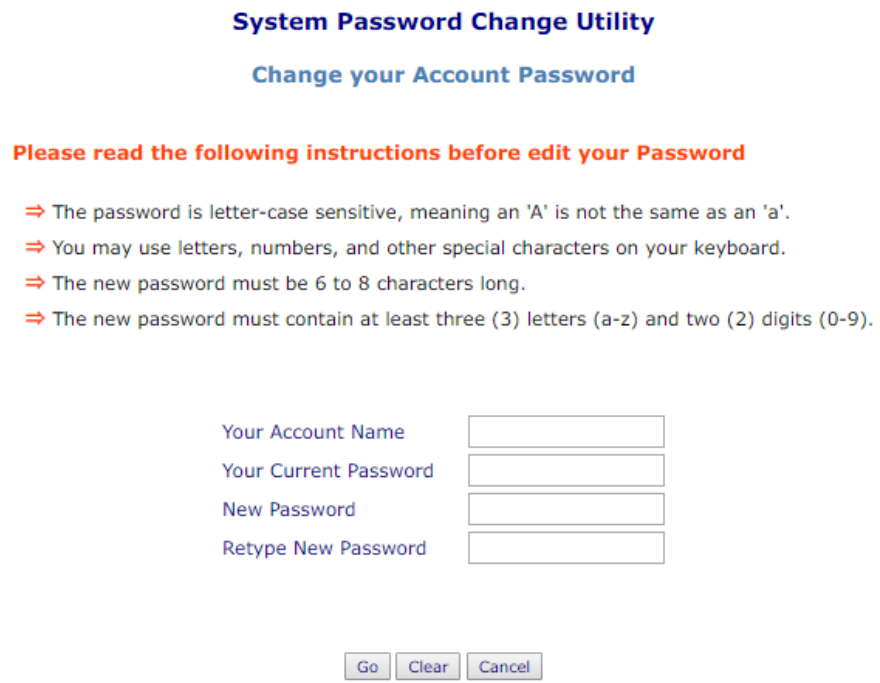
- 要連上工作站需要準備MobaXterm。
- 首先需要安裝MobaXterm ，設定session on MobaXterm。



MobaXterm 下載網址: https://mobaxterm.mobatek.net/download-home-edition.html

Your Default Account and Password

- Account : u+[YOUR STUDENT ID NUMBER]
  e.g. : u0250718
- Remember to change password by System Password Change Utility



Frequently Used Command in Unix

- Print working directory
- <terminal>pwd
- List the folders and files
- <terminal>ls
- Change a directory
- <terminal>cd ~ ; cd ..
- Make a directory
- <terminal>mkdir
- Remove a file
- <terminal>rm
- Remove a directory
- <terminal>rm -r

Before Designing a Circuit (1/2)

- Environment setup(first time you log in only)
  - <terminal>source ~u0850754/00_FirstTimeLogin
- Untar file
  - <terminal>tar –xvf ~u0850754/VLSI_LAB.tar
- Check successful untar file
  - <terminal>cd vlsilab
  - <terminal>ls –al

```
[ce26]/usr3/ce21/student/u0650722/% cd vlsilab/
[ce26]/usr3/ce21/student/u0650722/vlsilab/% ls -al
total 28
drwxr-xr-x  5 u0650722 student 4096 Sep 10 13:54 .
drwx------  6 u0650722 student 4096 Sep 10 13:59 ..
-rw-r--r--  1 u0650722 student  254 Sep 10 13:53 .cdsinit
-rw-r--r--  1 u0650722 student 1465 Sep 10 13:53 .tcshrc
drwxr-xr-x  5 u0650722 student 4096 Sep 25  2013 calibre
drwxr-xr-x  2 u0650722 student 4096 Sep 25  2013 model
drwxr-xr-x  2 u0650722 student 4096 Sep 25  2013 virtuoso
[ce26]/usr3/ce21/student/u0650722/vlsilab/%
```

Successful

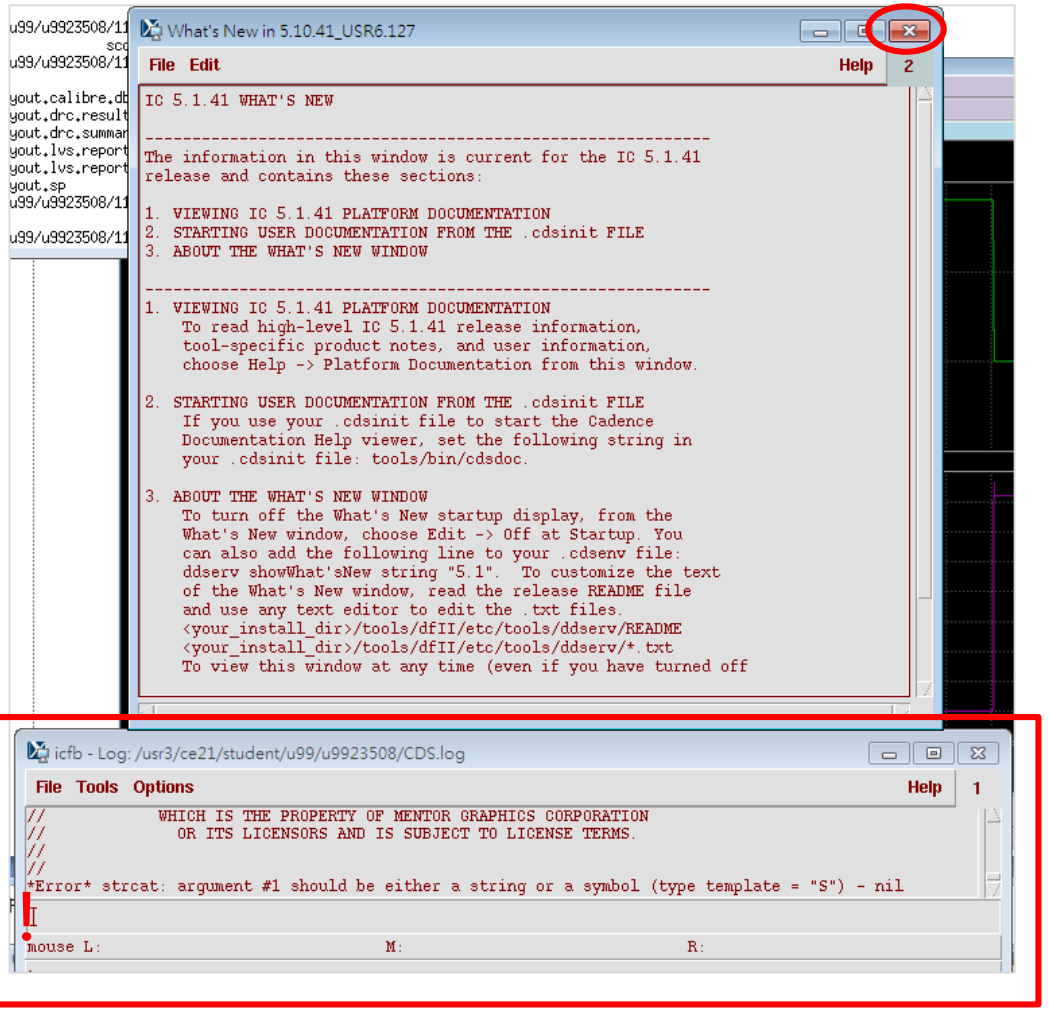
Before Designing a Circuit (2/2)

- Folder “model”
  - cic018.l: Library file for Hspice simulation
- Folder “virtuoso”
  - Technology file
  - Display file
- Folder “calibre”
  - Files for DRC、LVS and PEX

Launch Cadence Virtuoso

-[~/vlsilab]$ icfb &

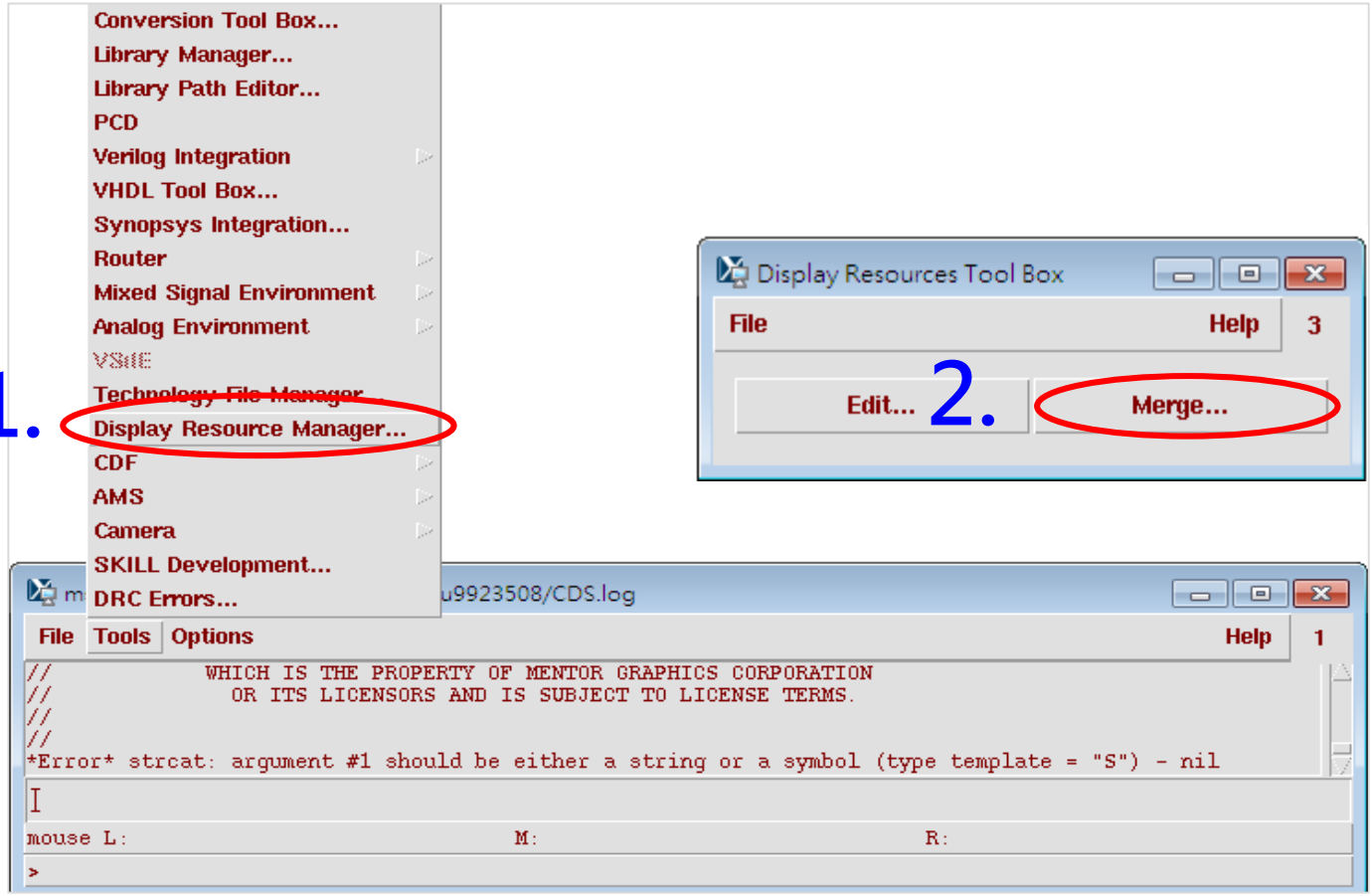
Close it



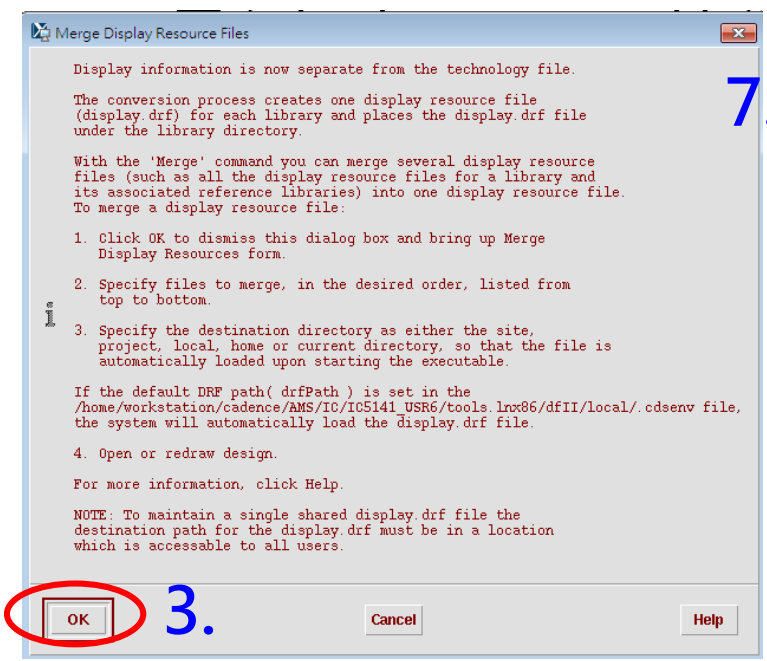
Succeed to Launch!

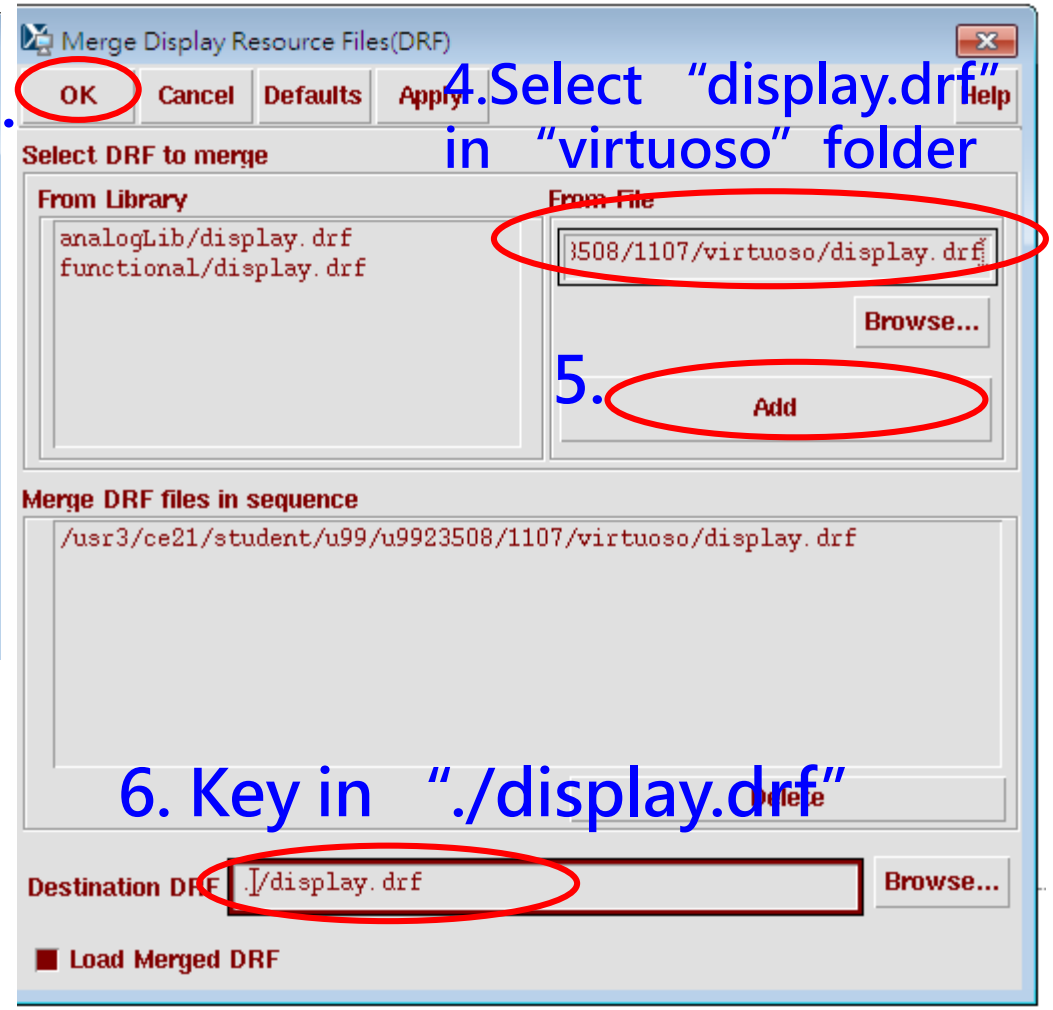
Load Display Resource File (1/2)

- Load the layer information into virtuoso (color, layer number ….)
- Just do it at the first time

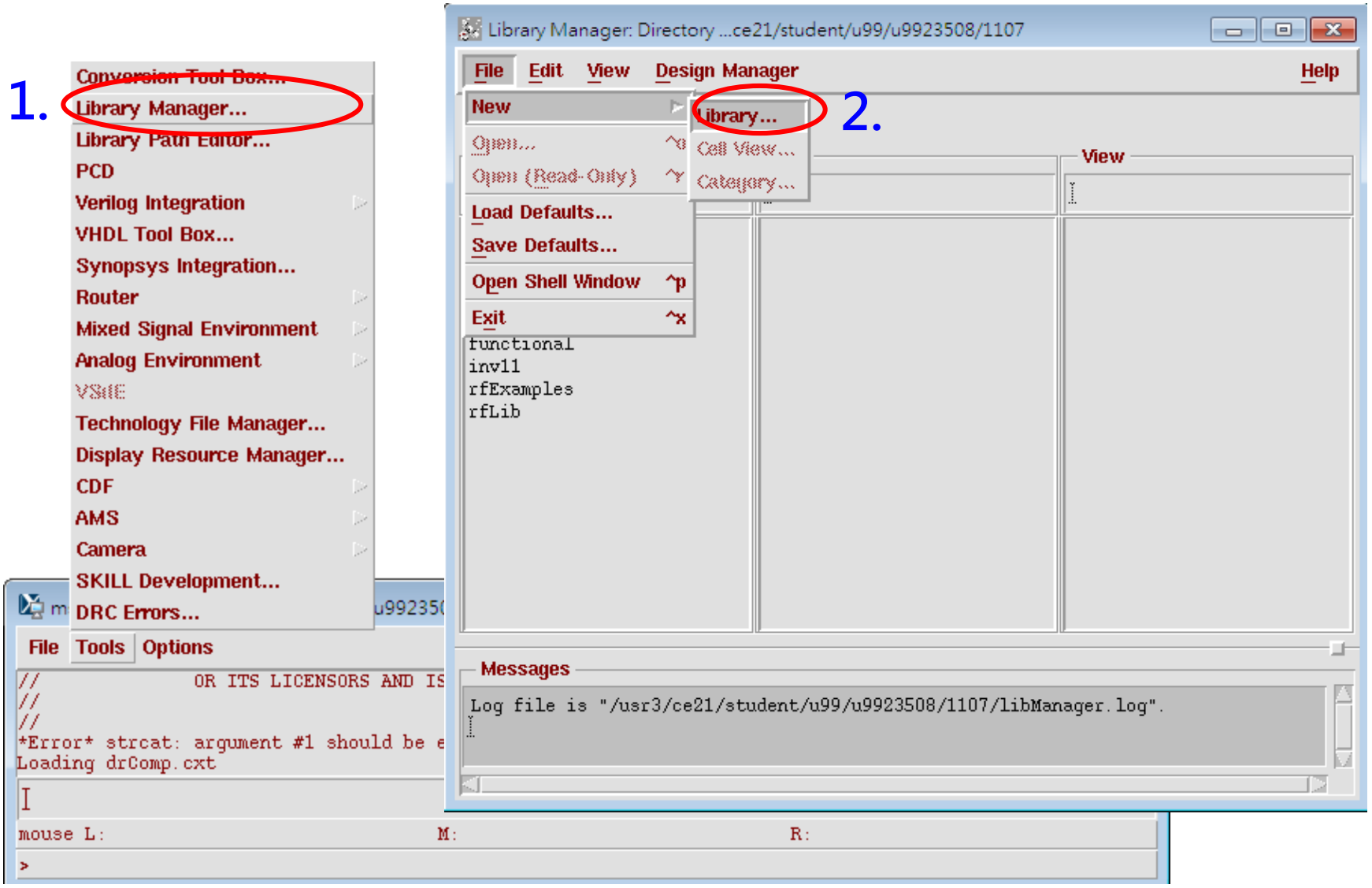


Load Display Resource File (2/2)

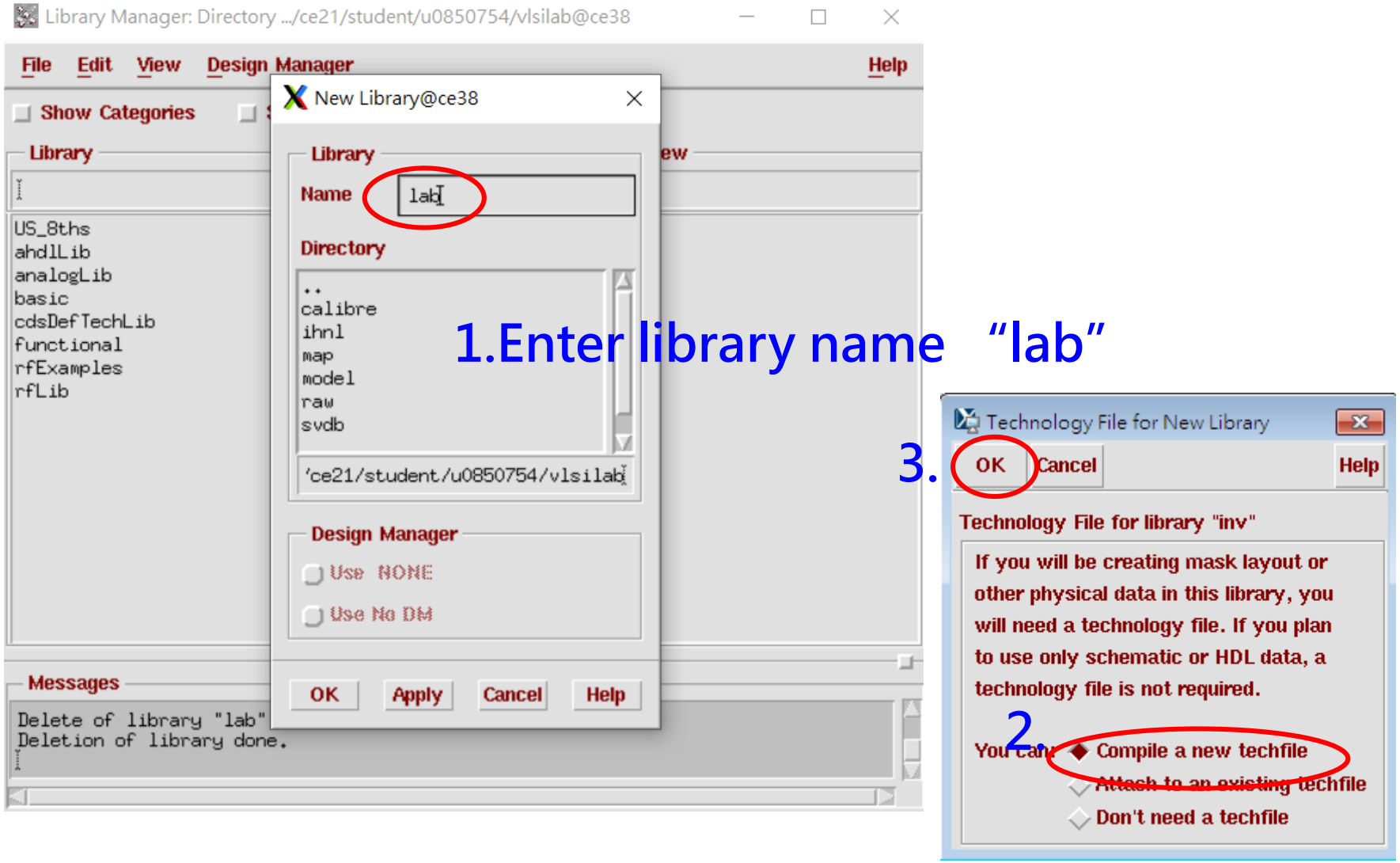




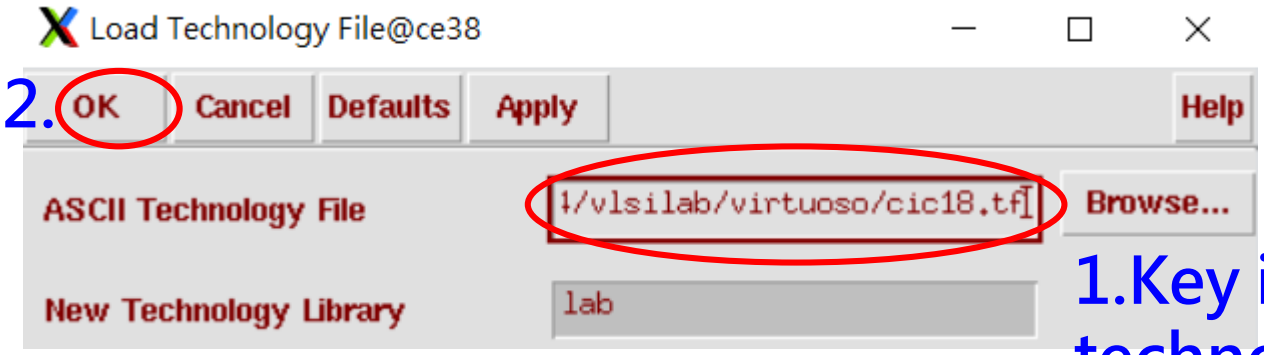
Create a New Library (1/3)



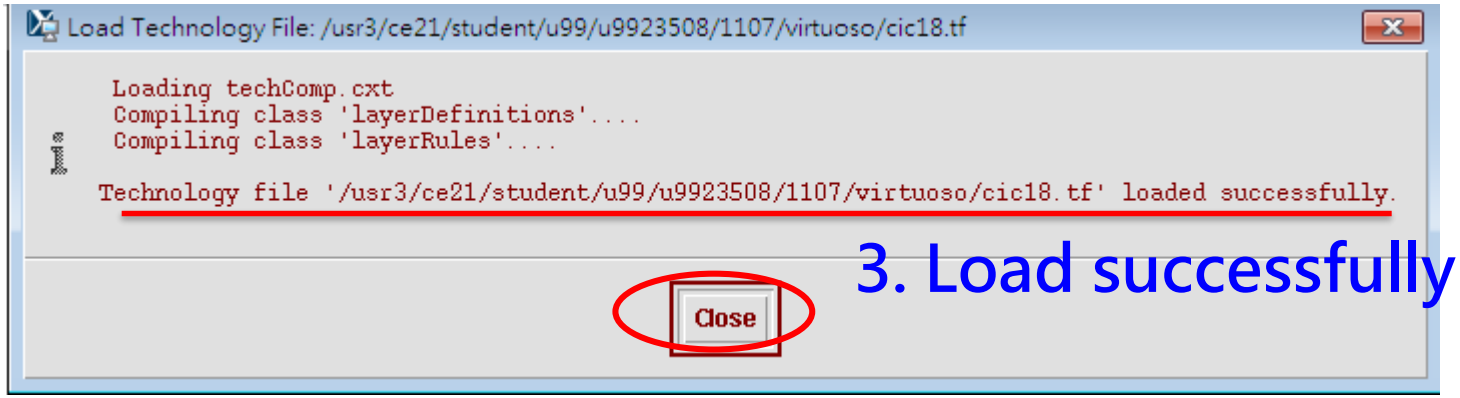
Create a New Library (2/3)



Create a New Library (3/3)

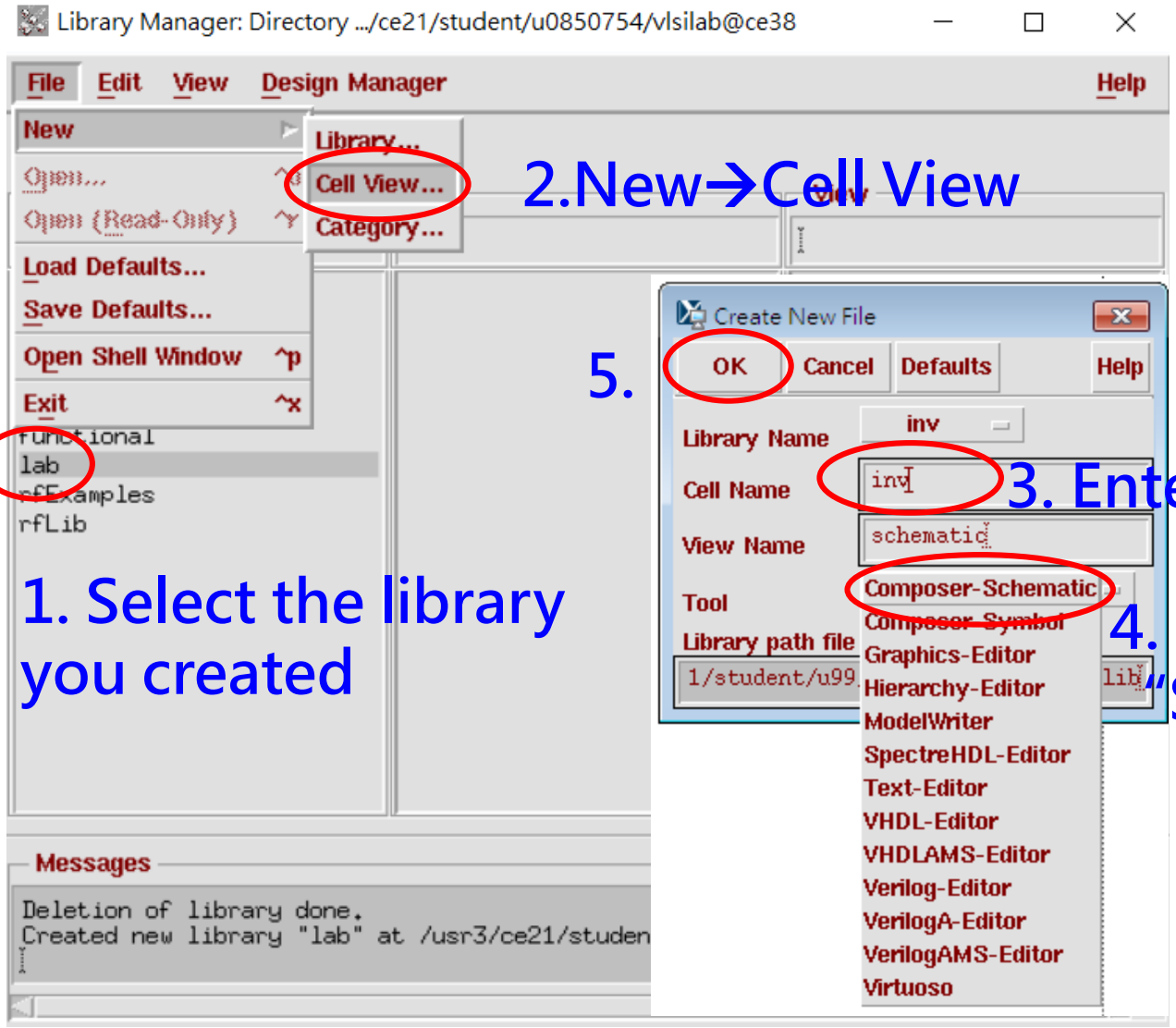


1.Key in path of technology file

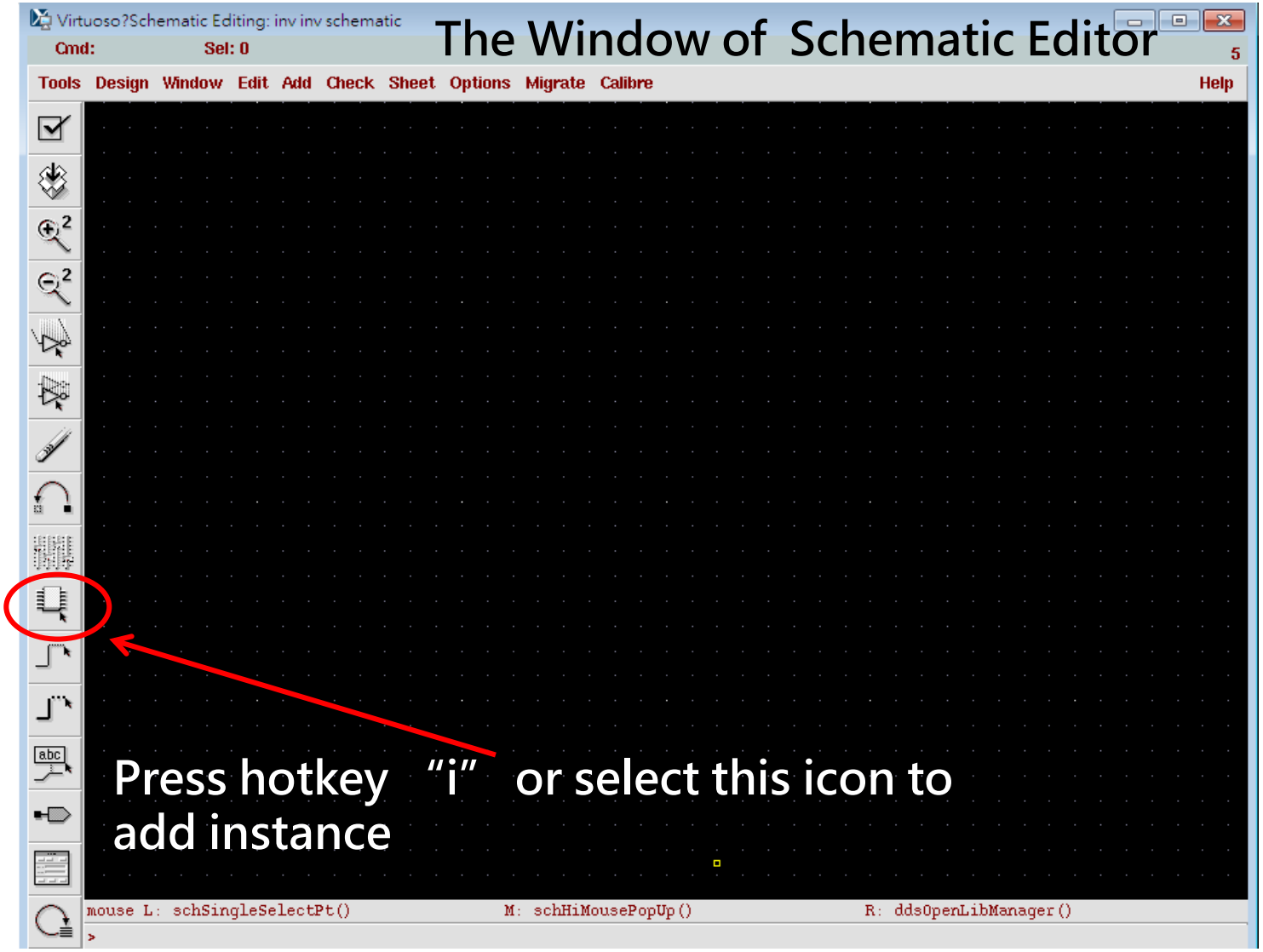


3. Load successfully

Create a New Cell – Schematic (1/6)



Create a New Cell – Schematic (2/6)

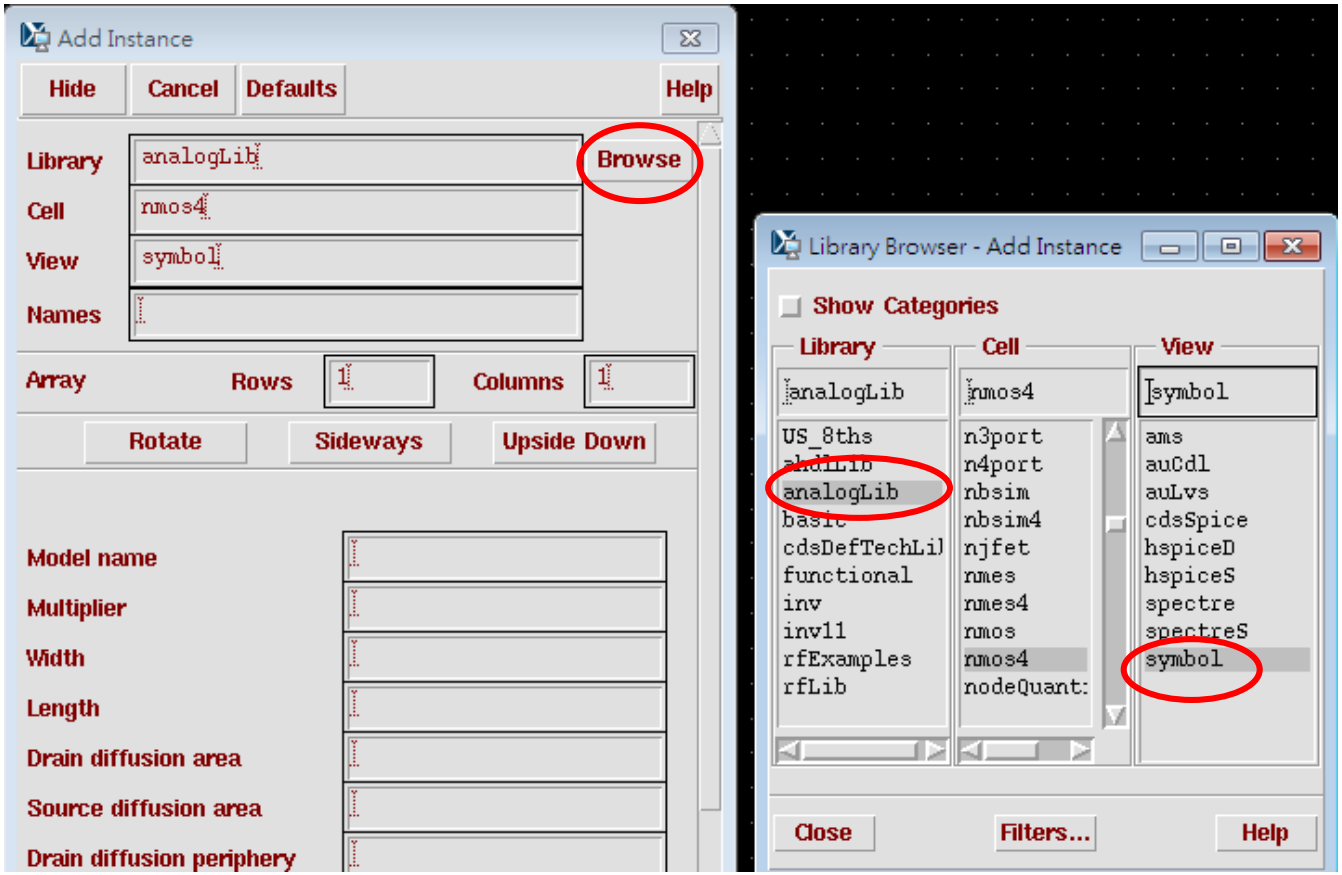


Create a New Cell – Schematic (3/6)

Press "Browse" button

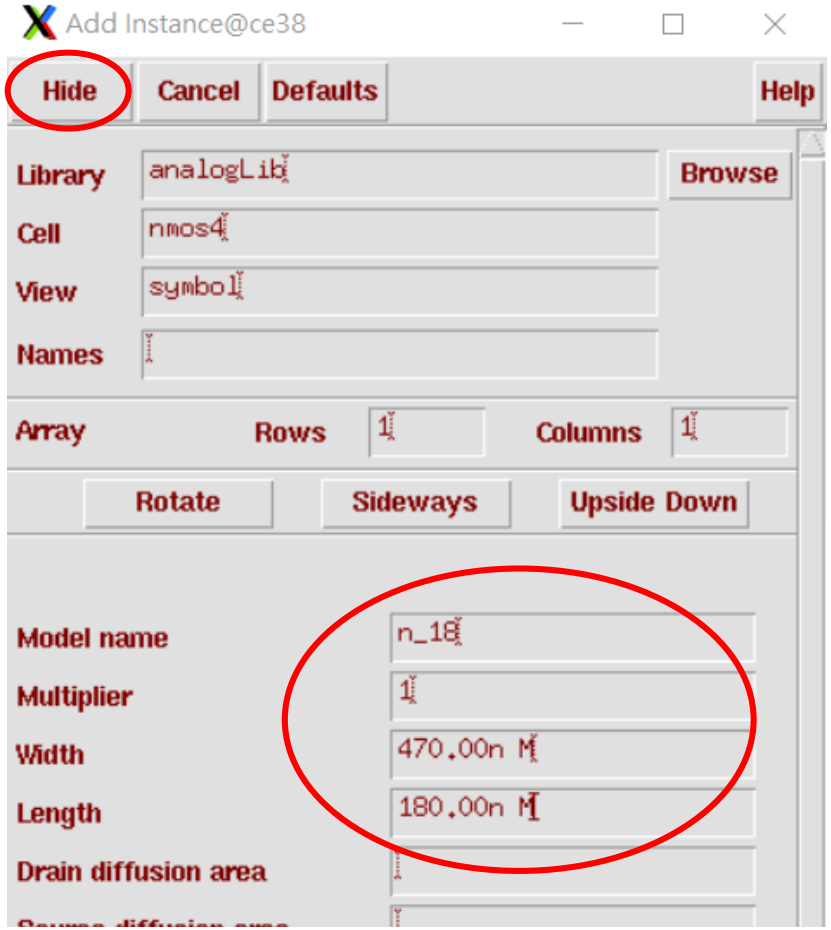
1. select analogLib

2. instance (pmos4, nmos4, vdd, gnd, …)



Create a New Cell – Schematic (4/6)

"Hide " to close this window



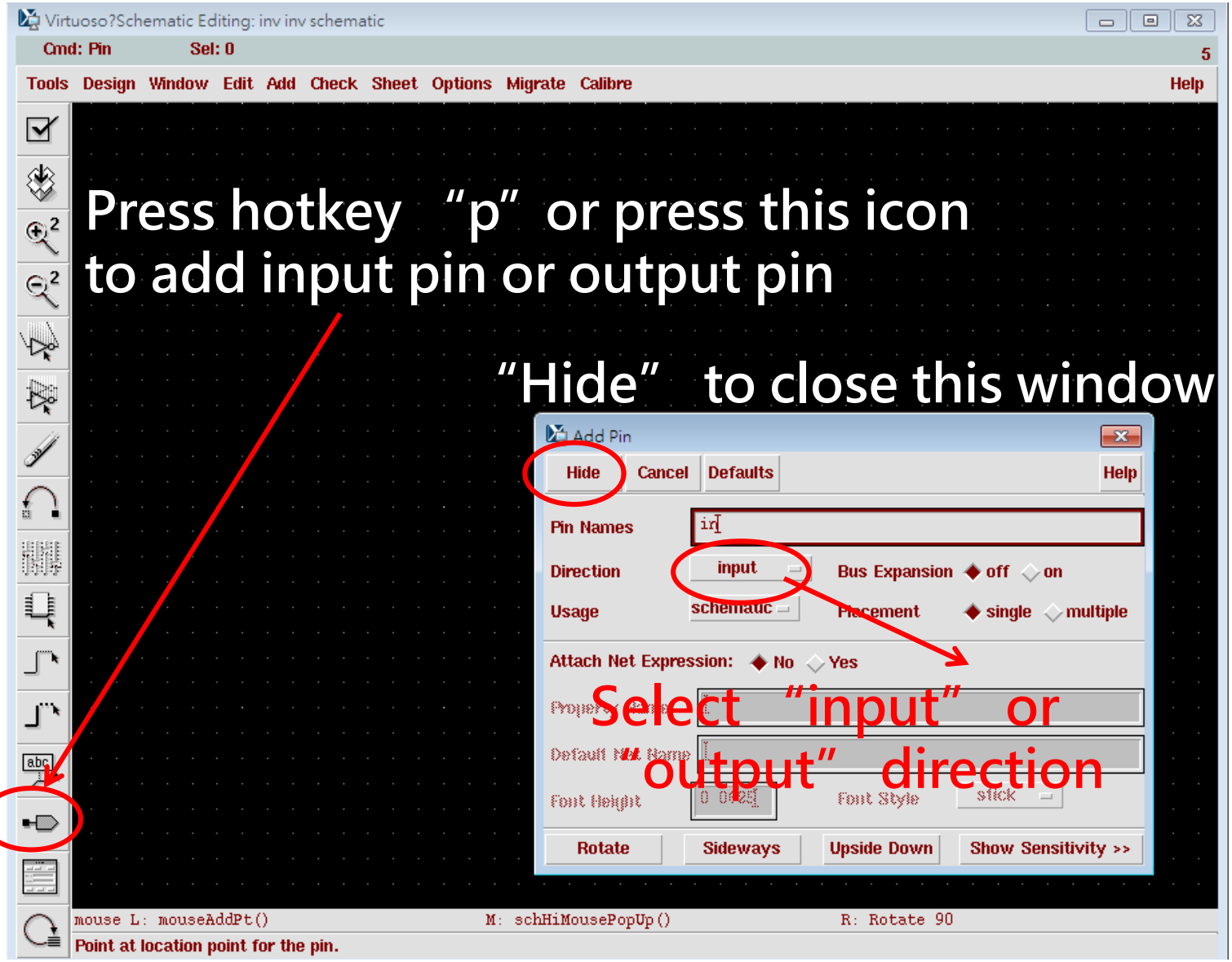
In this lab

1. (Width/Length)p=0.94um/0.18um
2. (Width/Length)n=0.47um/0.18um

For cell "nmos4"

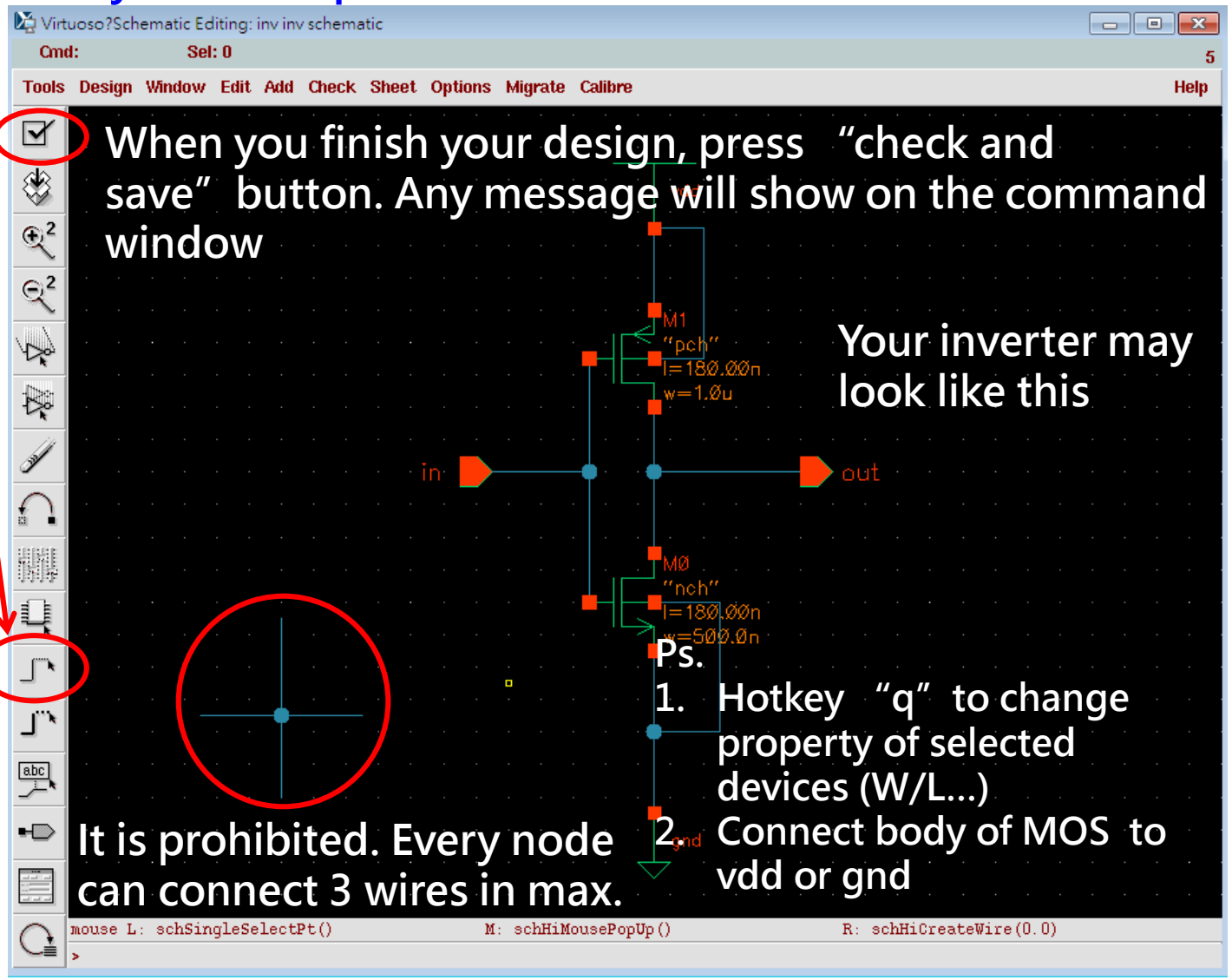
1. Model name: n_18
2. Multiplier: 1
3. Width: 0.47u
4. Length: 0.18u

Create a New Cell – Schematic (5/6)



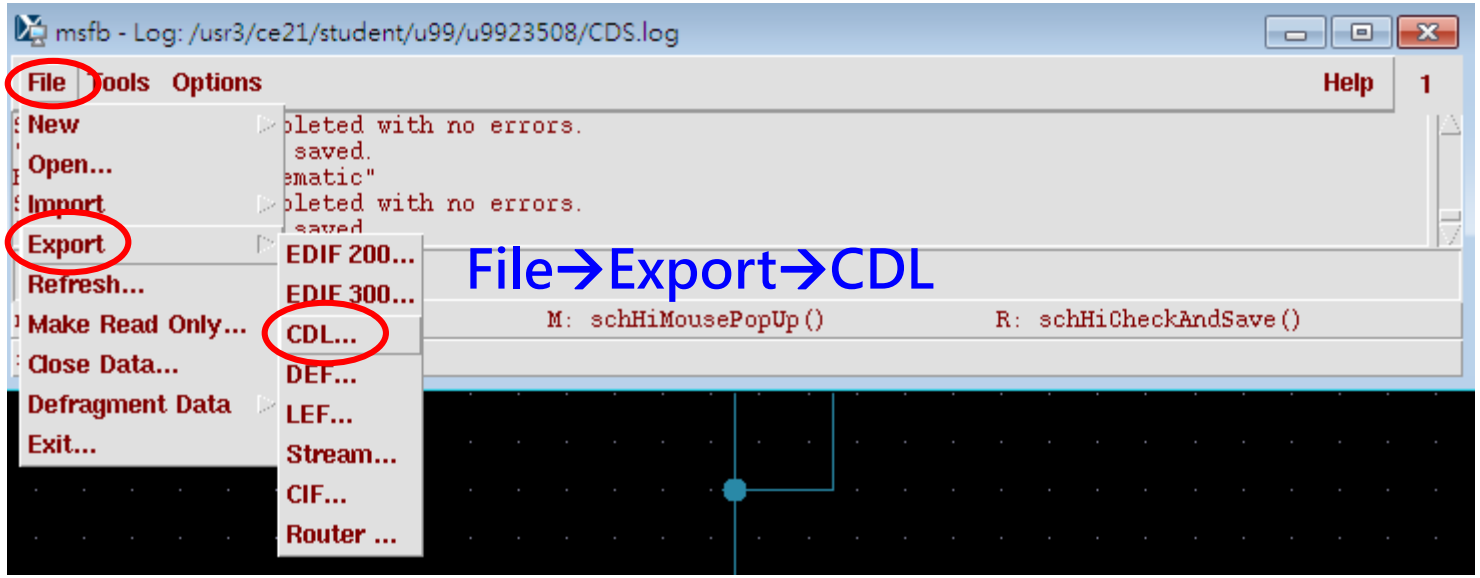
Create a New Cell – Schematic (6/6)

Press hotkey "w" or press this icon to make a connection

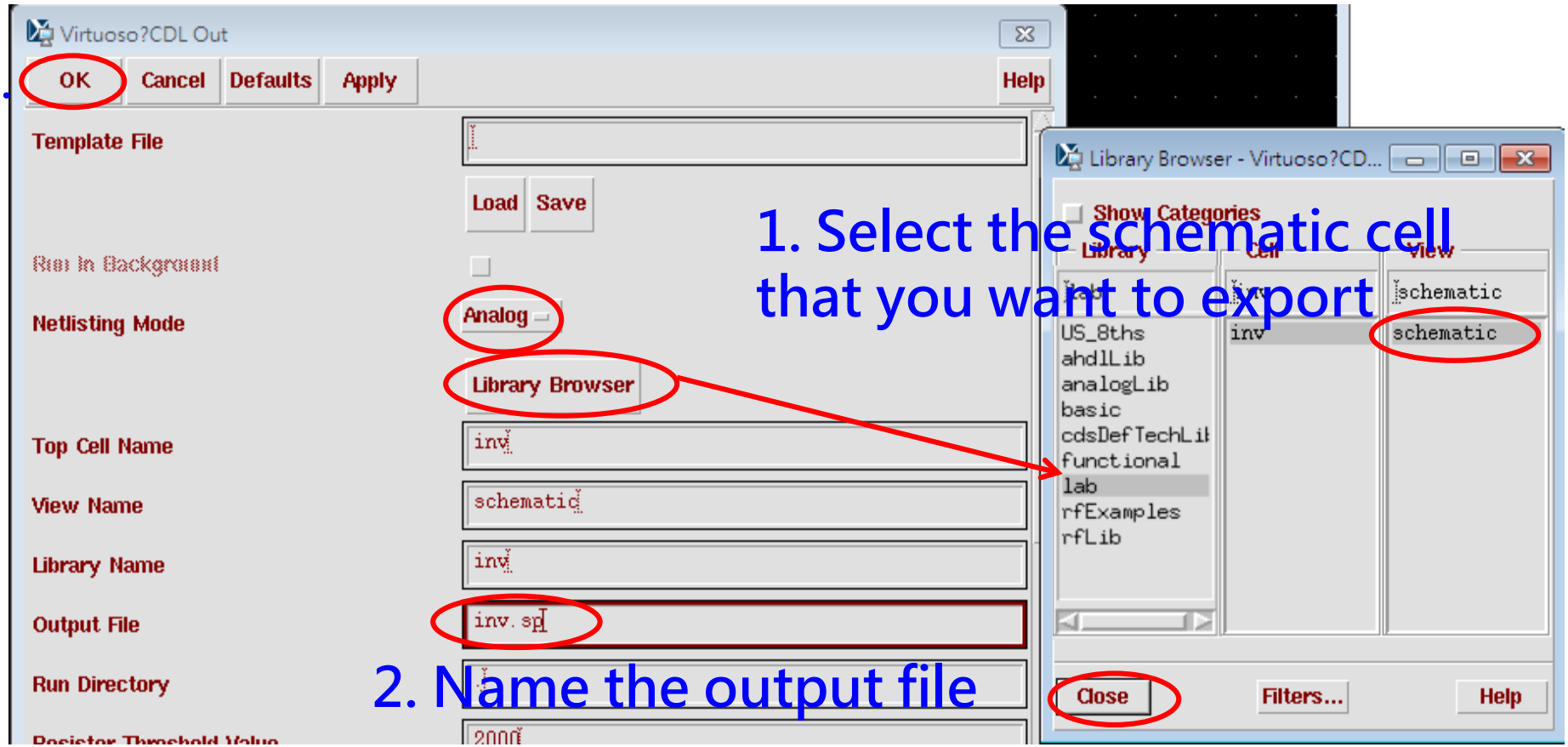


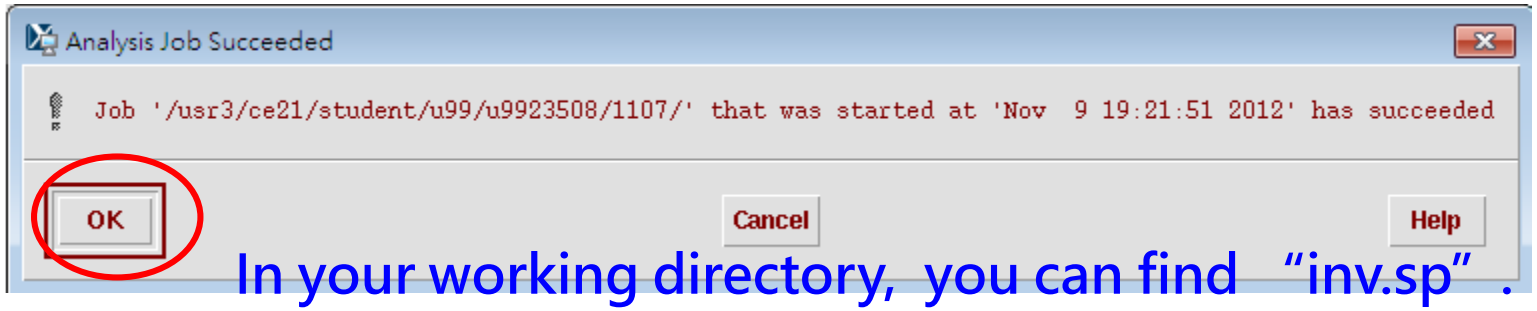
Export Spice Netlist (1/3)

- Back to icfb command window
- Export schematic to spice file



Export Spice Netlist (2/3)





In your working directory, you can find "inv.sp".

Export Spice Netlist (3/3)

Use gedit to revise inv.sp in server

```
********************************************************************************
* auCdl Netlist:
*
* Library Name:  inv
* Top Cell Name: inv
* View Name:     schematic
* Netlisted on:  Sep 10 12:15:10 2018
********************************************************************************

*.BIPOLAR
*.RESI = 2000
*.RESVAL
*.CAPVAL
*.DIOPERI
*.DIOAREA
*.EQUATION
*.SCALE METER
*.MEGA
*.PARAM

*.GLOBAL gnd!
+        vdd!

*.PIN gnd!
*+    vdd!

********************************************************************************
* Library Name: inv
* Cell Name:    inv
* View Name:    schematic
********************************************************************************

.SUBCKT inv vin vout vdd! gnd!
*.PININFO vin:I vout:O
MM1 vout vin vdd! vdd! P_18 W=1u L=180n m=1
MM0 vout vin gnd! gnd! N_18 W=500.0n L=180n m=1
.ENDS
```

Star symbol – "*" means start of comment

Hspice will not execute the first line.
Please don't write comment in the first line.

1. Comment ".PARAM"

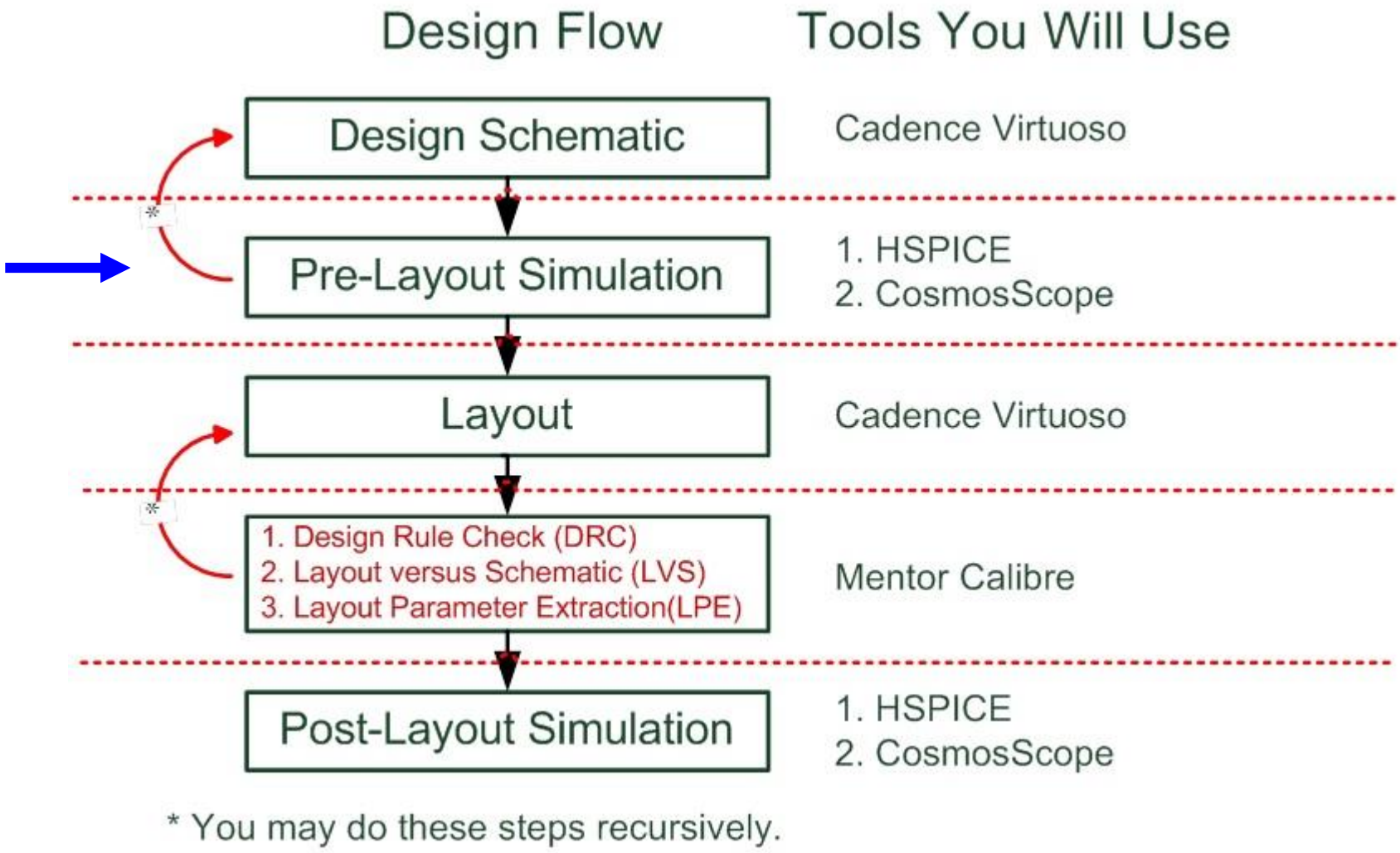
By default, the case of letters are insensitive in spice.

Description of inverter

2. Add "vdd! gnd!" manually

3. Replace "PM" and "NM" to "P_18" and "N_18" respectively.

Design Flow of Full-Custom Chip



Create Spice Netlist for simulation(1/2)

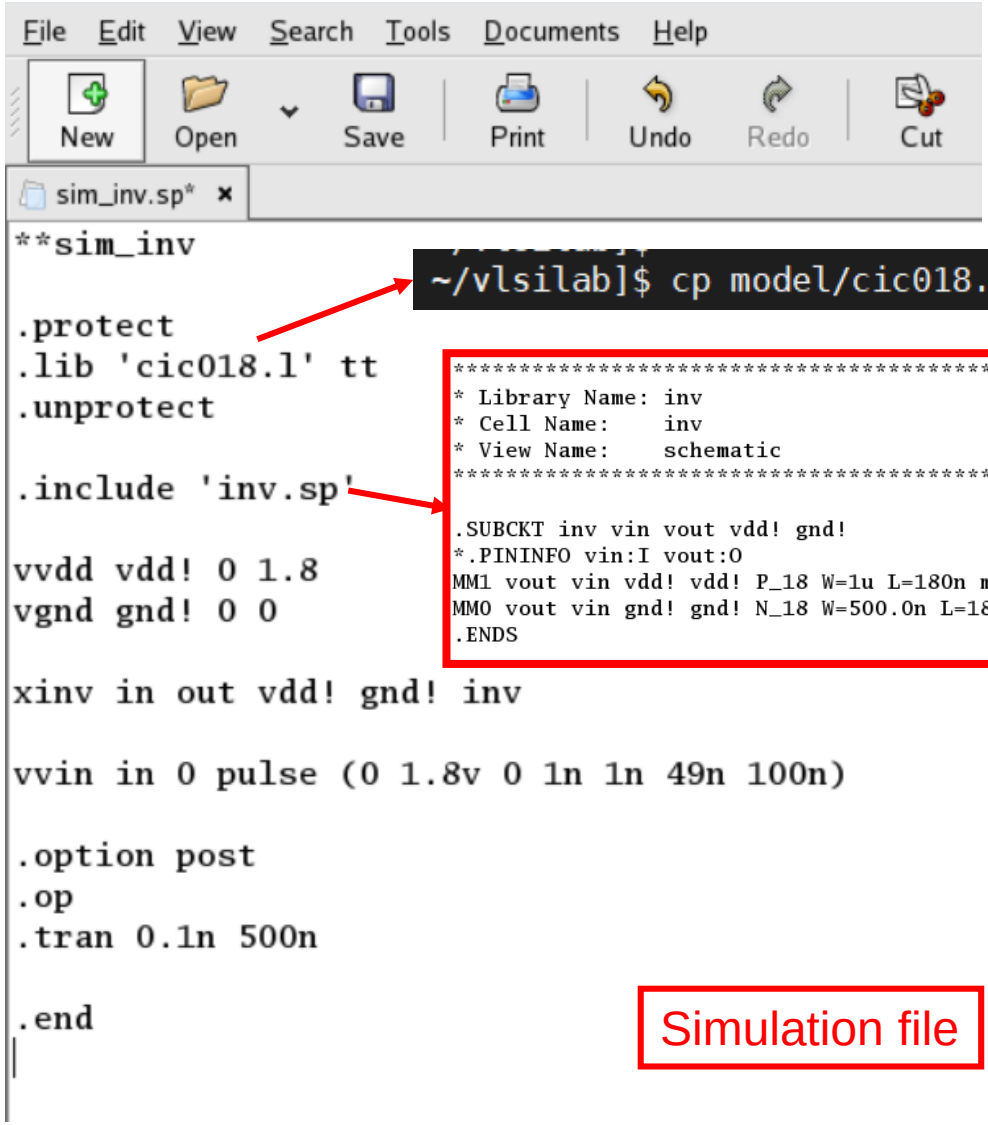
Title

include library

Define voltage

Call subcircuits

Define input waveform




```
~/vlsilab]$ cp model/cic018.l ~/vlsilab/
```

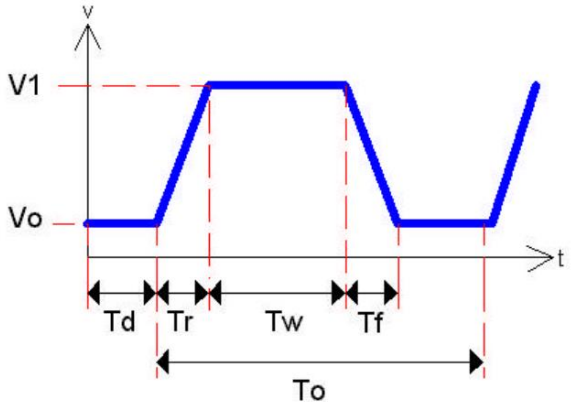
```
********************************************************************************
* Library Name: inv
* Cell Name:    inv
* View Name:    schematic
********************************************************************************

.SUBCKT inv vin vout vdd! gnd!
*.PININFO vin:I vout:O
MM1 vout vin vdd! vdd! P_18 W=1u L=180n m=1
MM0 vout vin gnd! gnd! N_18 W=500.0n L=180n m=1
.ENDS
```

Design file

Simulation file

Create Spice Netlist for simulation(2/2)

- DC signal: V<name> V+ V- DC
  - Ex : vdd vdd gnd 1.8
- Pulse signal: pulse (V0 V1 <Tdelay Trise Tfall Twidth Tperiod>)
  - Ex : Vin in gnd pulse(0v 1.8v 5ns 1ns 1ns 9ns 20ns)
- Piecewise linear signal: pwl (t1 v1, t2 v2, …)
  - Ex : Vin in gnd pwl (25n 0v, 25.1n 1.8v)
- Others:
  - .op (post the operation point)
  - .tran 10ns 1000ns
    (transient analysis, sample in period of 10ns and 1000ns of the total run time)
  - .end (Must add at the end of file)
  - * (comment)



Hspice Simulation

- <terminal> hspice sim_xxx.sp | tee xxx.log

```
[ce24]/usr3/ce21/student/u99/u9923508/1108/sim/% hspice sim_inv.sp
```

xterm

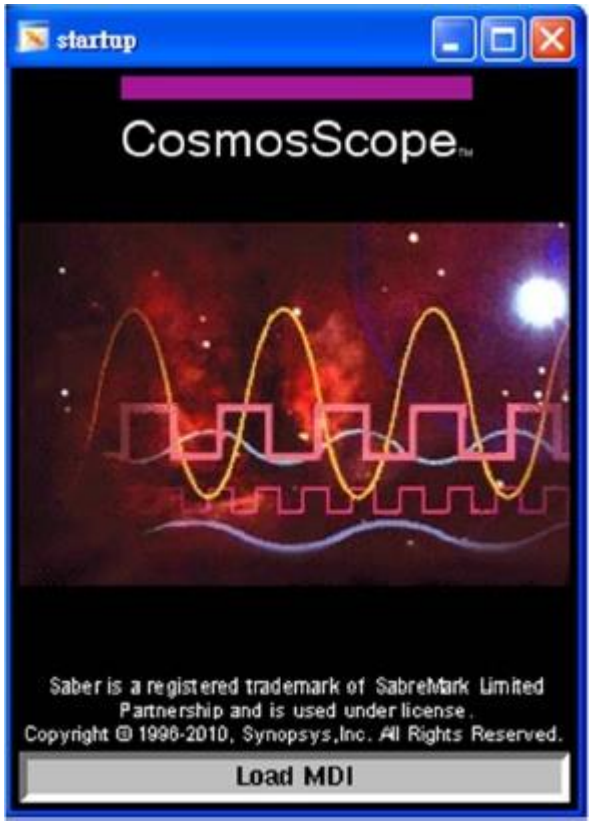
```
******  Runtime Statistics (seconds)  ******

analysis          time    # points   tot. iter  conv.iter
op point          0.00           1            7
transient         0.00        5001          429         166 rev=         1
readin            0.01
errchk            0.01
setup             0.00
output            0.00


          total memory used          193  kbytes
          total cpu time            0.02 seconds
          total elapsed time        0.16 seconds
          job started at     19:35:07 11/09/2012
          job ended   at     19:35:07 11/09/2012


>info:       ***** hspice job concluded
 lic: Release hspice token(s)
real 0.17
user 0.02
sys 0.01
[ce24]/usr3/ce21/student/u99/u9923508/1108/sim/%
```

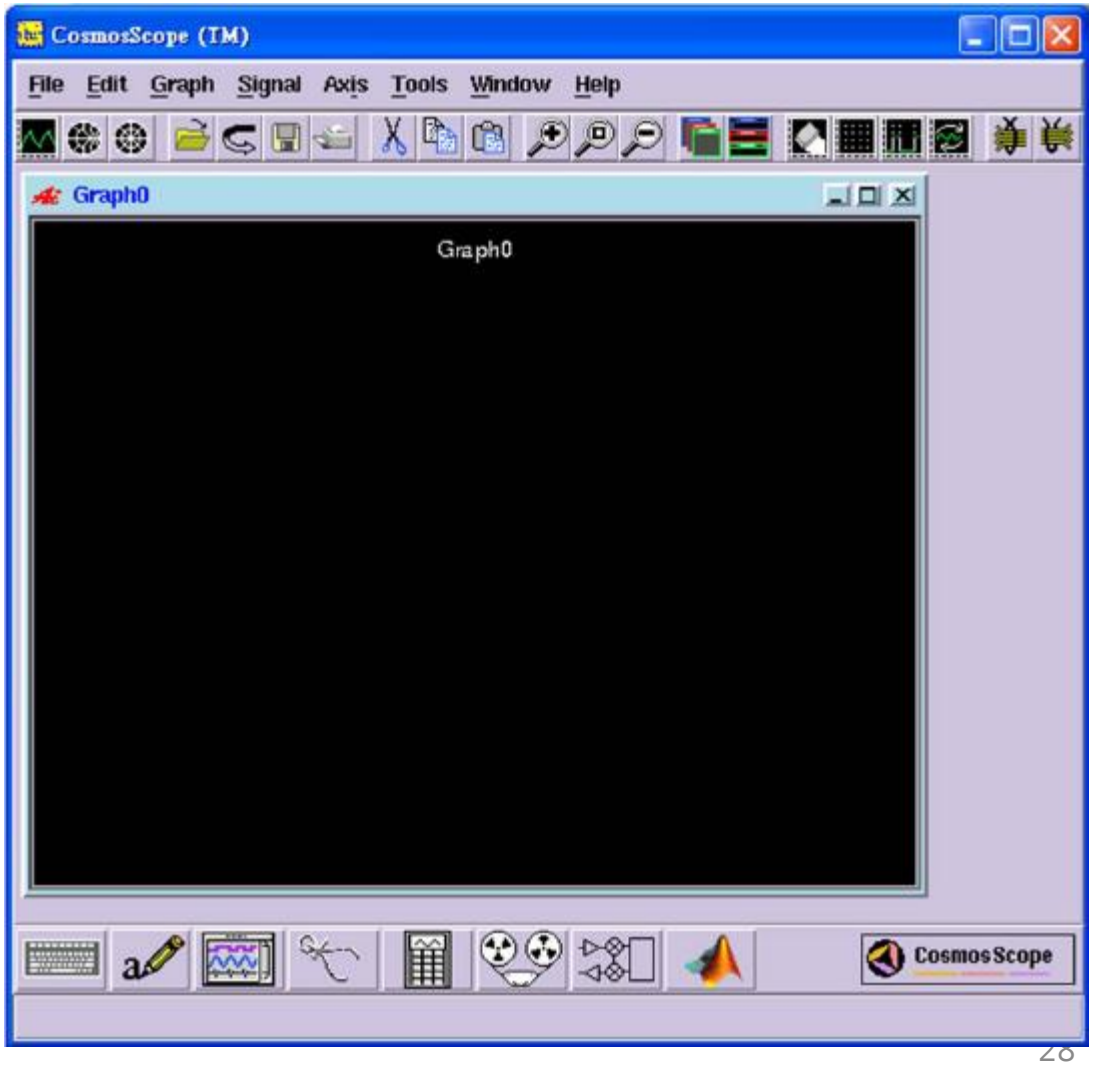
Simulate successfully

Otherwise, it shows: "hspice job aborted"

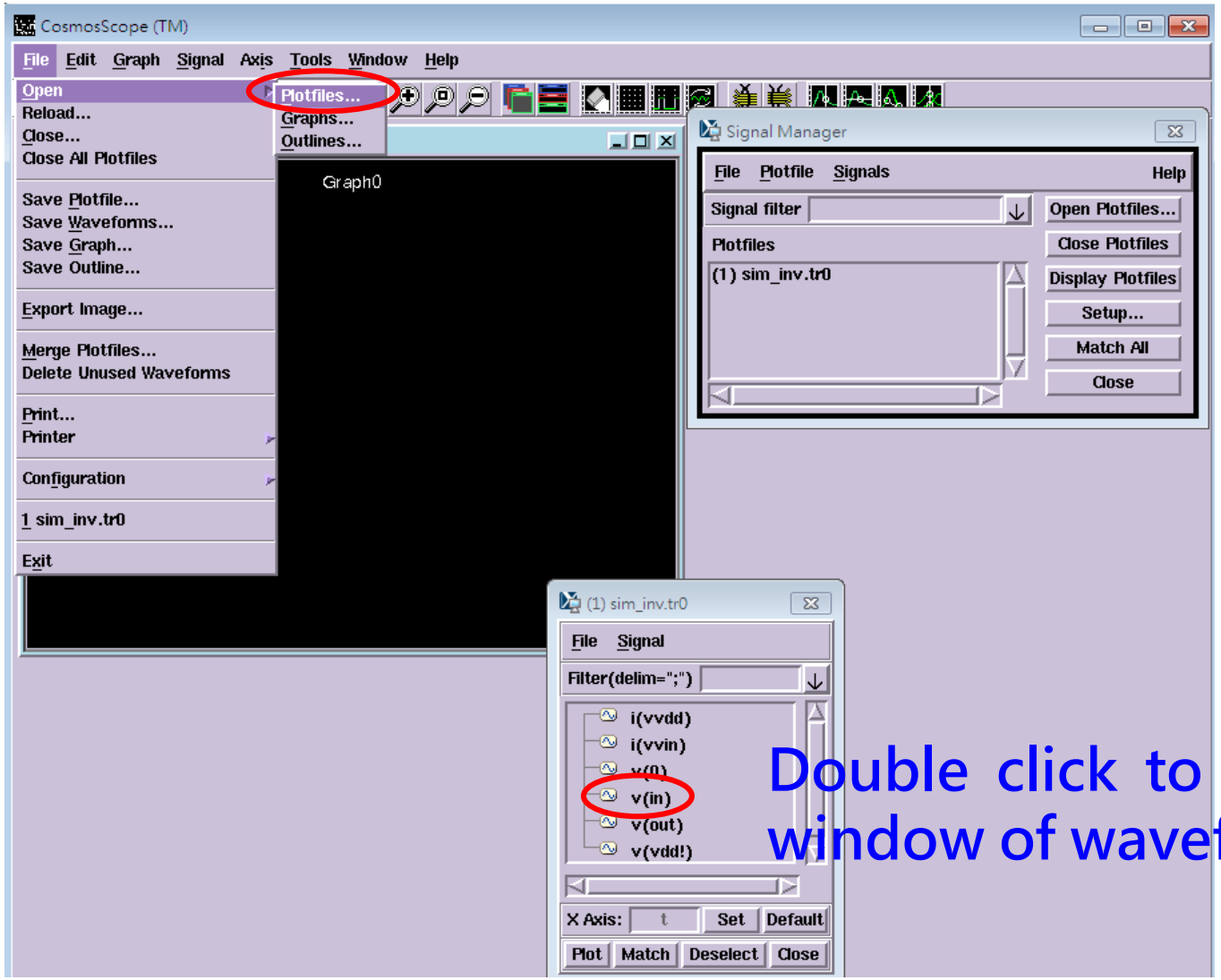
CosmosScope (1/5)

- <terminal>cscope &





CosmosScope (2/5)



Double click to open the window of waveform

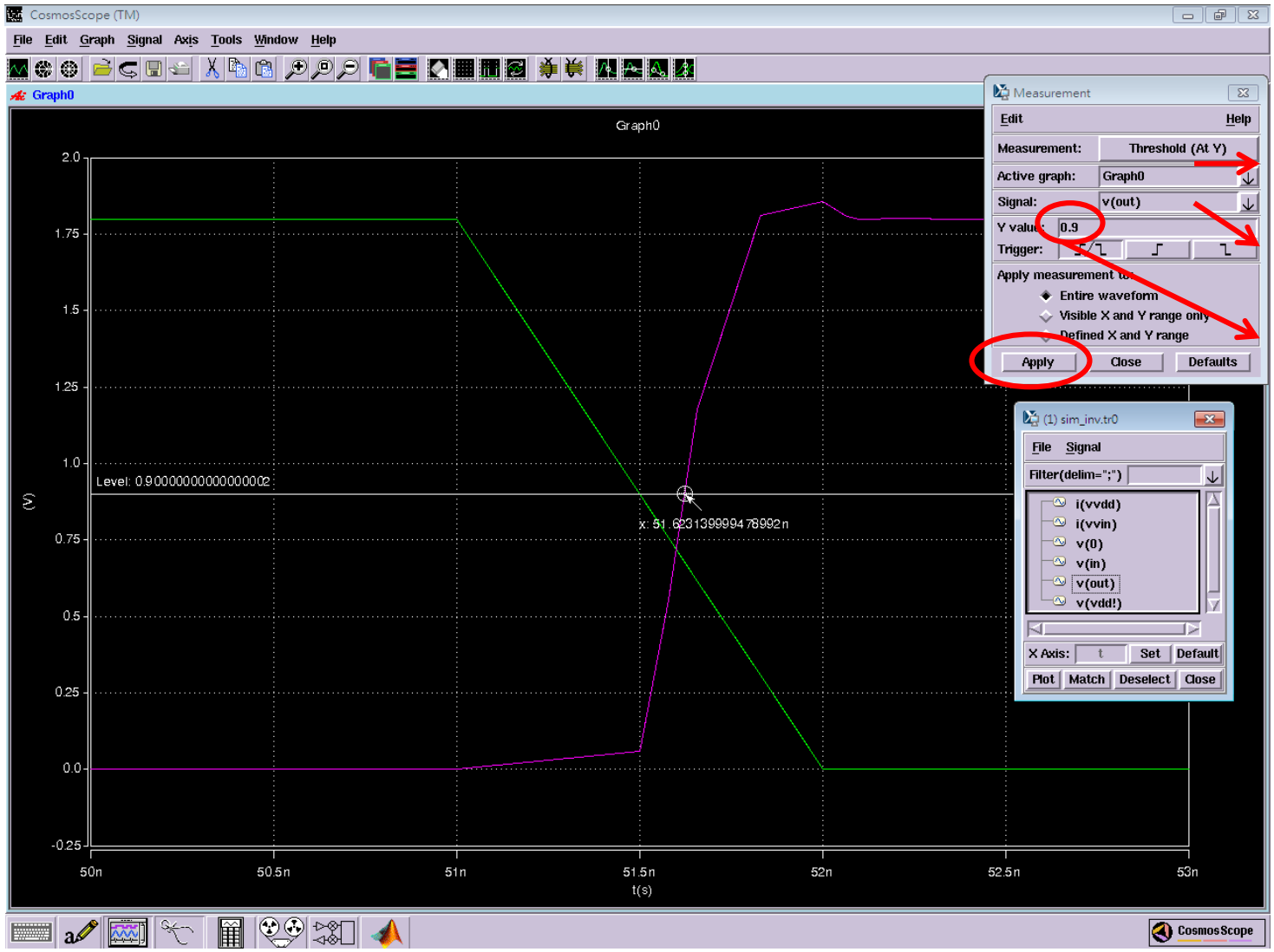
CosmosScope (3/5)

CosmosScope (4/5)

Tools → Measurement Tool

Adjust the resolution of waveform

CosmosScope (5/5)

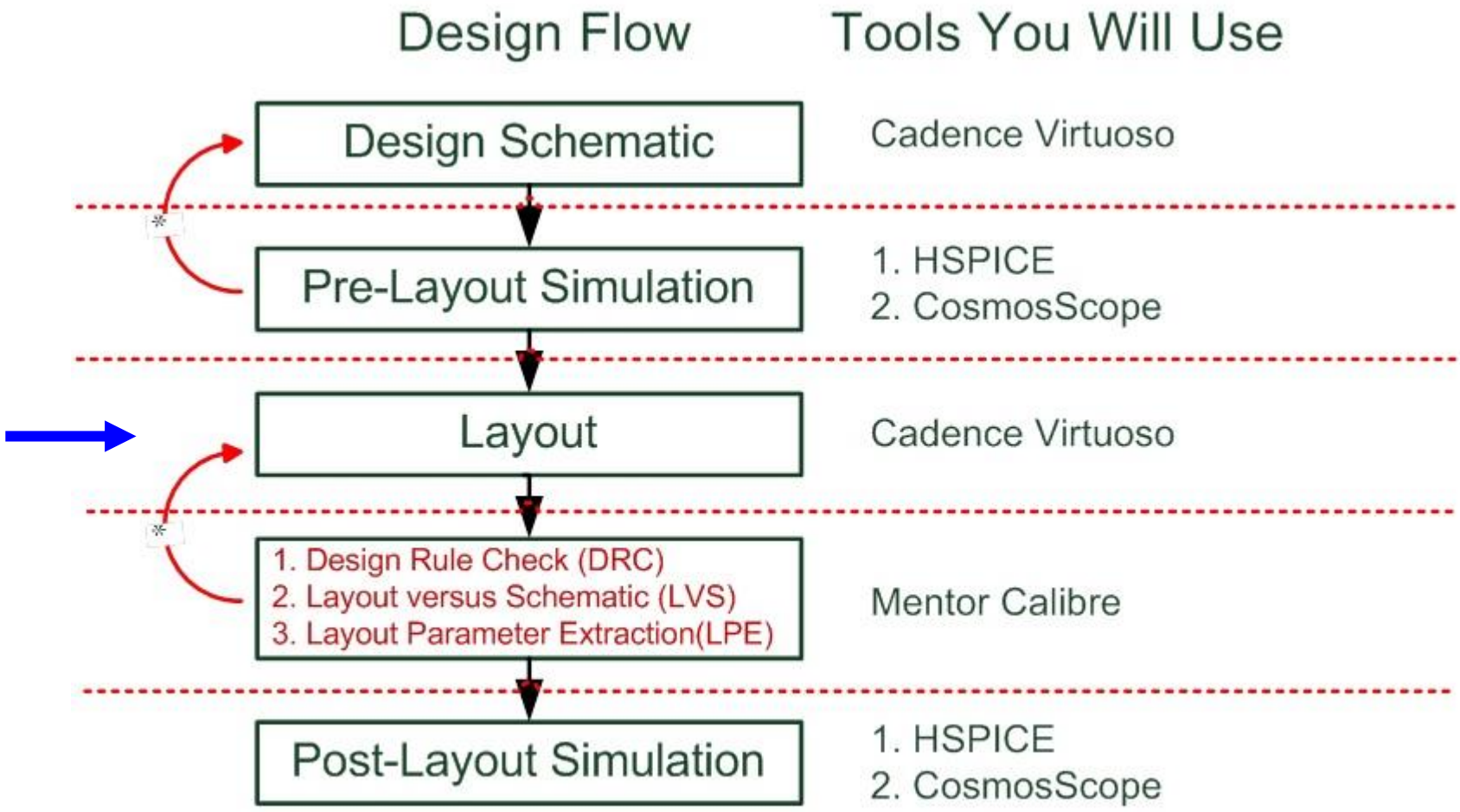


Measurement Options

Probe Signal

Fixed Value

Design Flow of Full-Custom Chip

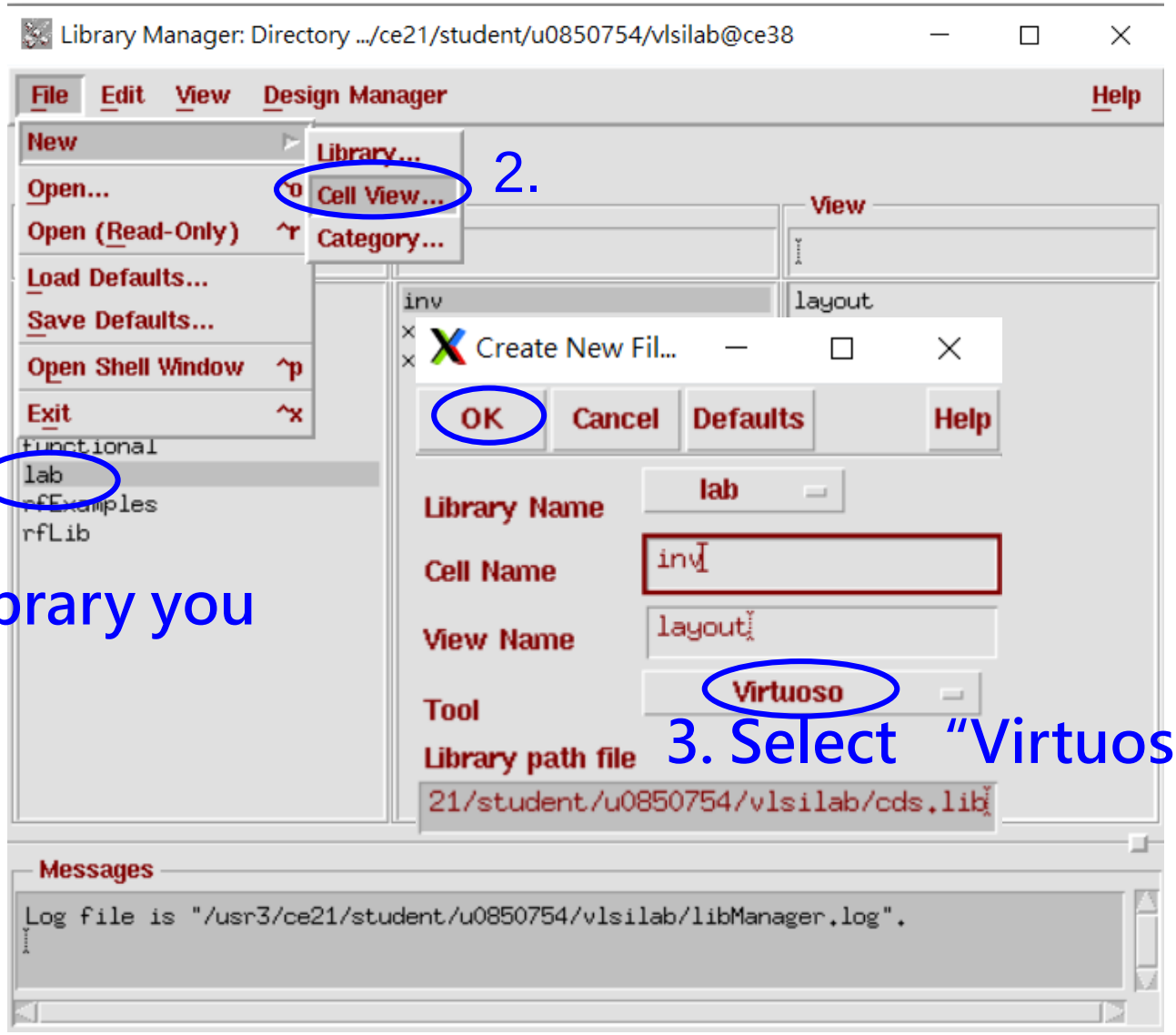


Layout

- When the behavior of circuit is verified, then you can draw the layout.

- Add layout cell view in library manager

Create a Layout Cell View

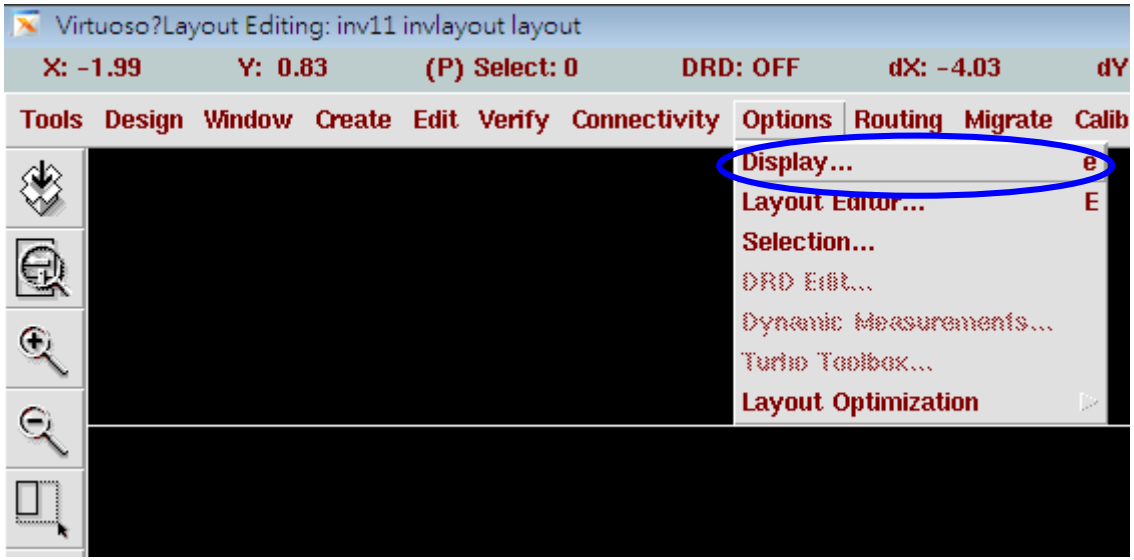


1. The Library you created

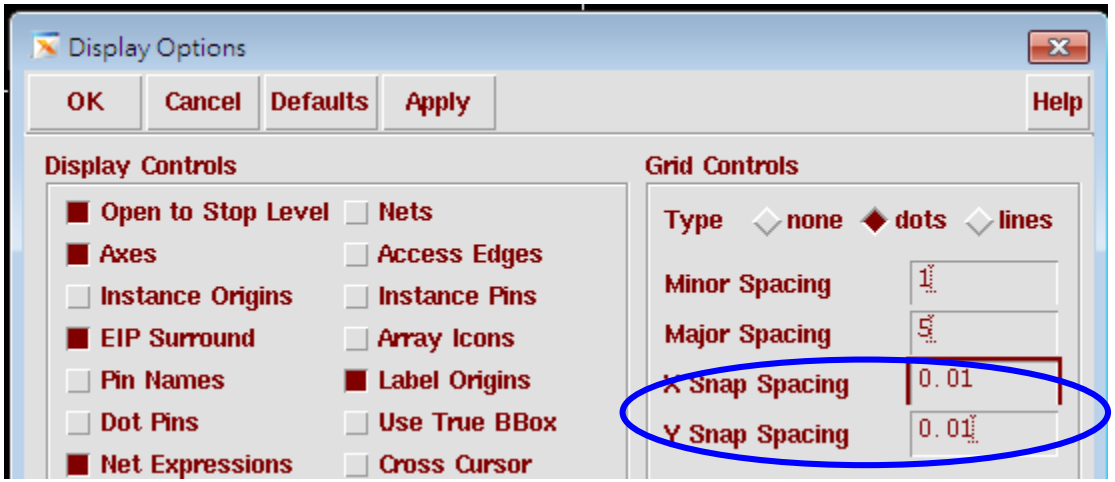
3. Select "Virtuoso" tool

Settings for Layout Environment

- **Set display options as you launch Virtuoso**



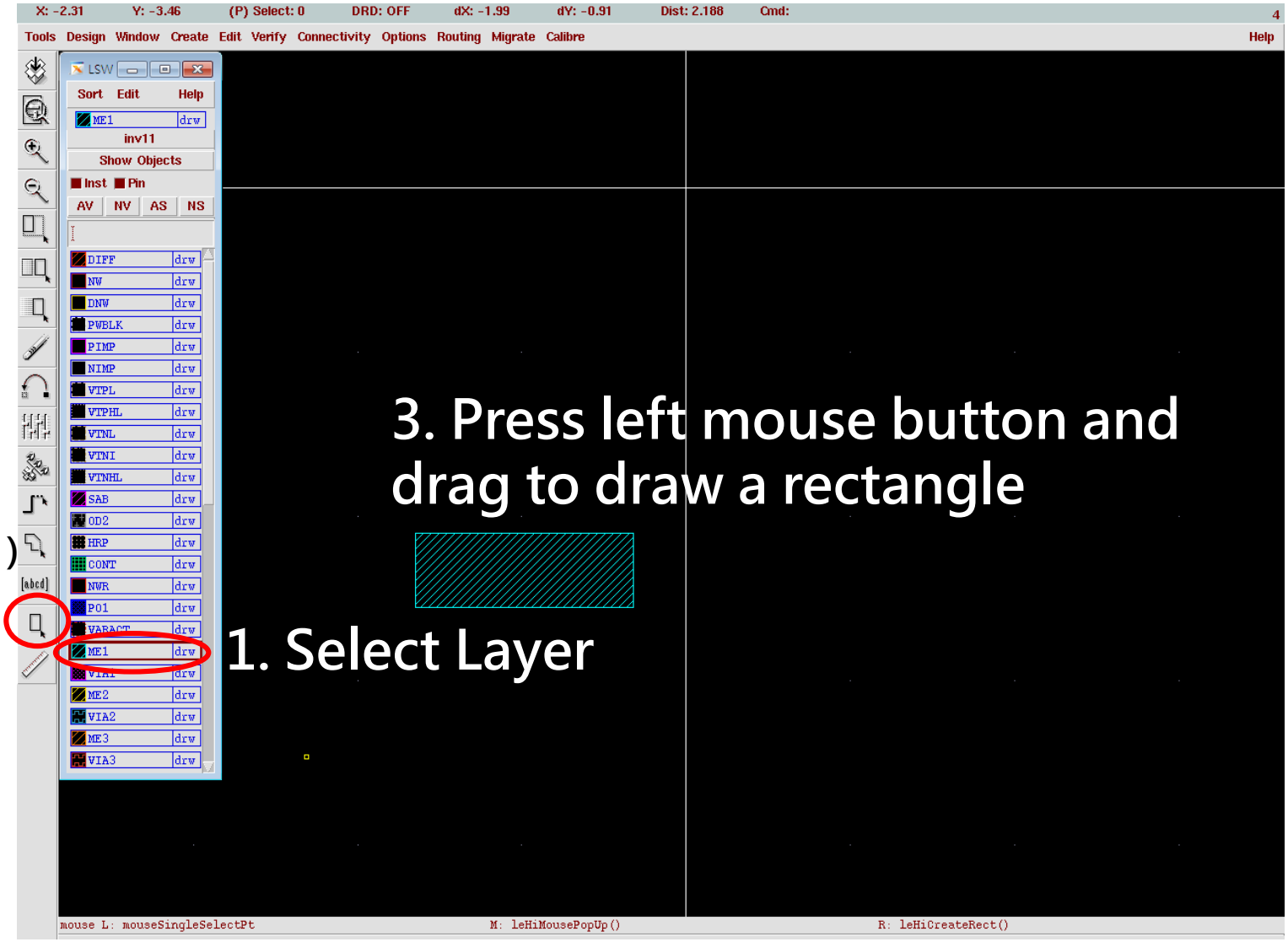
1. Options → Display



2. Snap Spacing: 0.01

Layout : Device

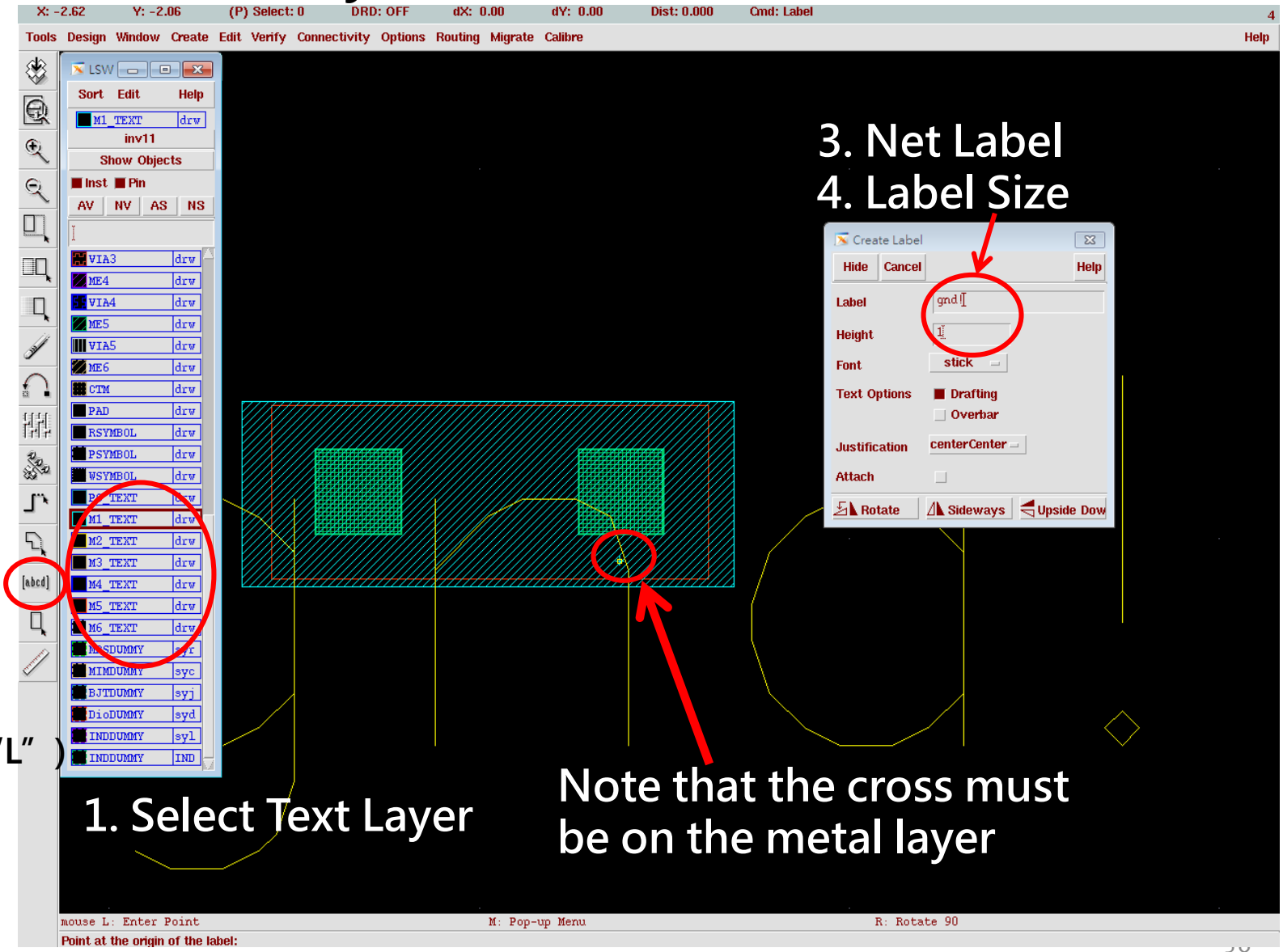
2. Select “Rectangle” Button (hotkey – “r”)



3. Press left mouse button and drag to draw a rectangle

1. Select Layer

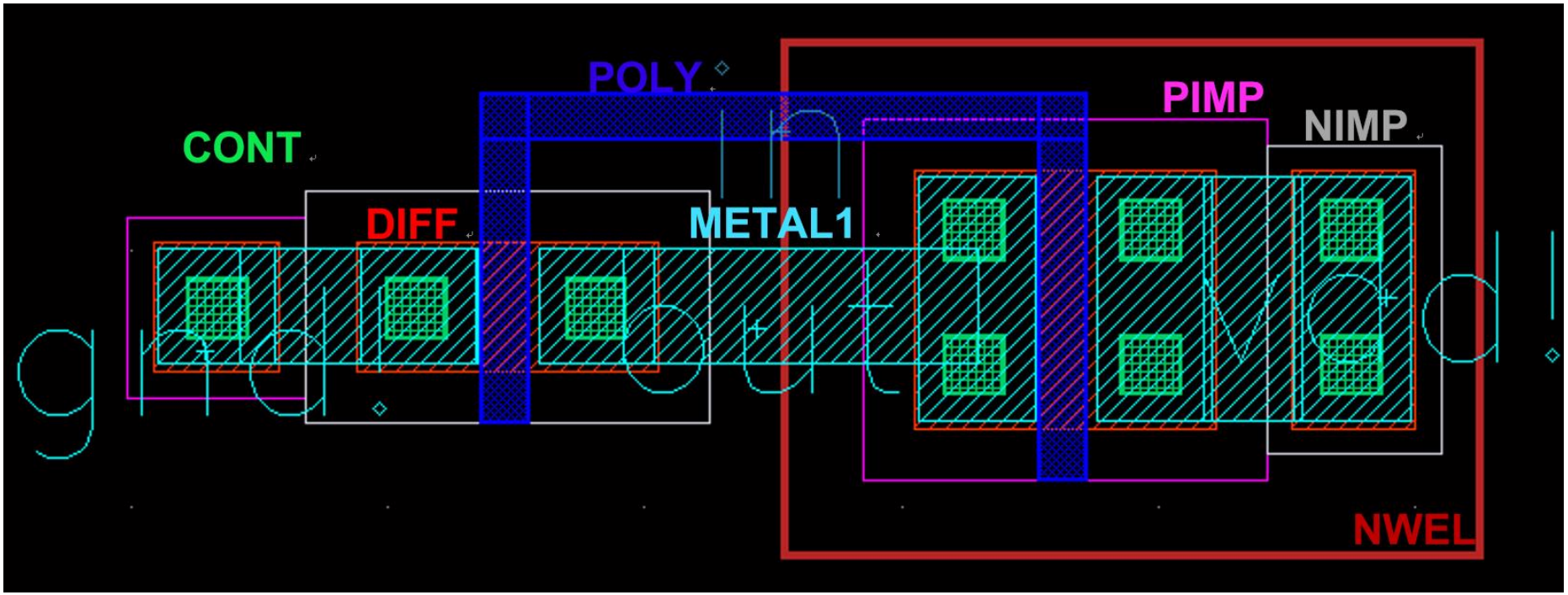
Layout : Add Label



Cadence Virtuoso – Hot Keys for Layout

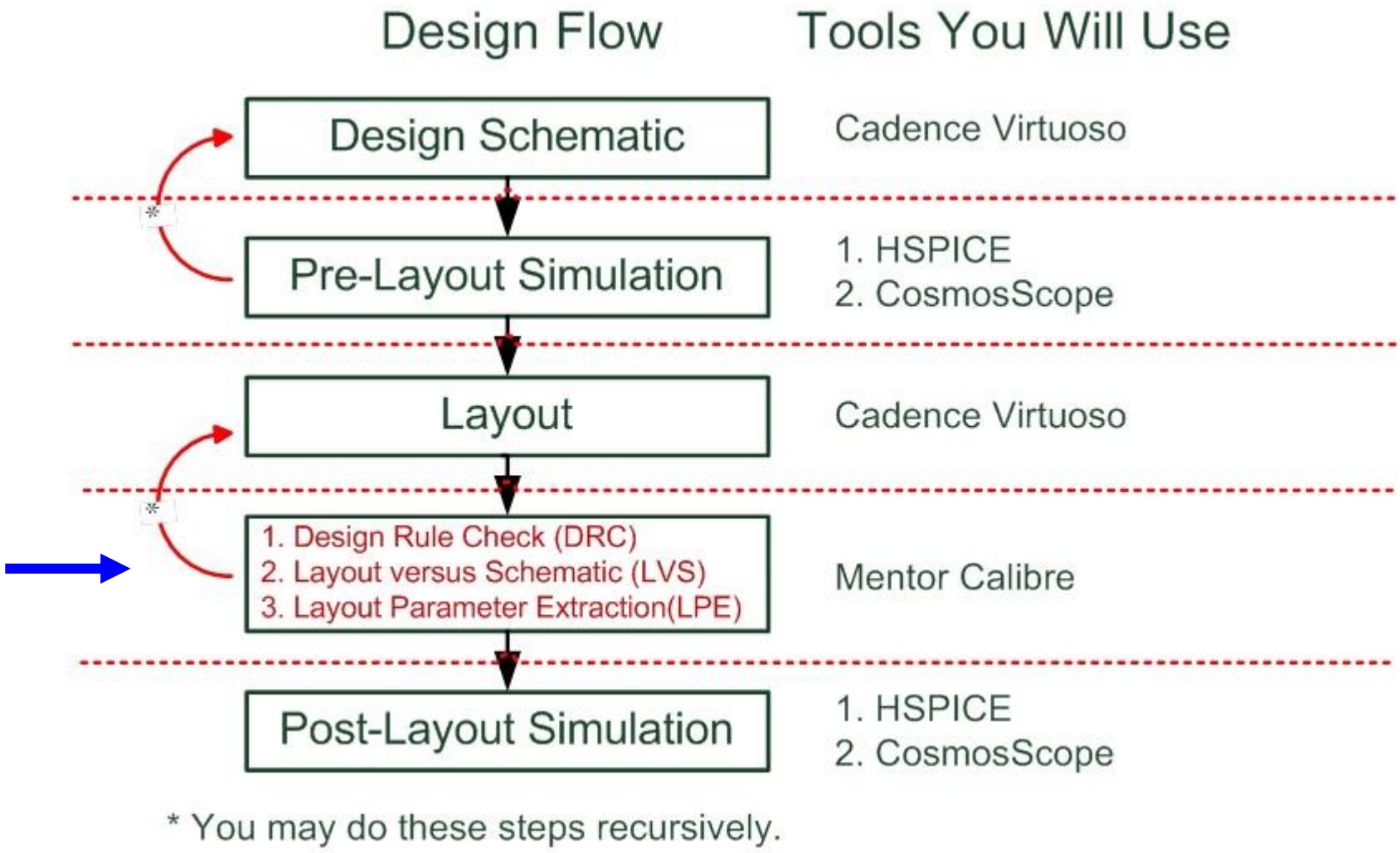
- m : move
- c : copy
- s : stretch/shrink
- k : ruler
- Shift + k: clear ruler
- Ctrl + z : zoom in
- Shift + z : zoom out
- f : fit the layout size
- Esc: cancel command

Layout : Circuits

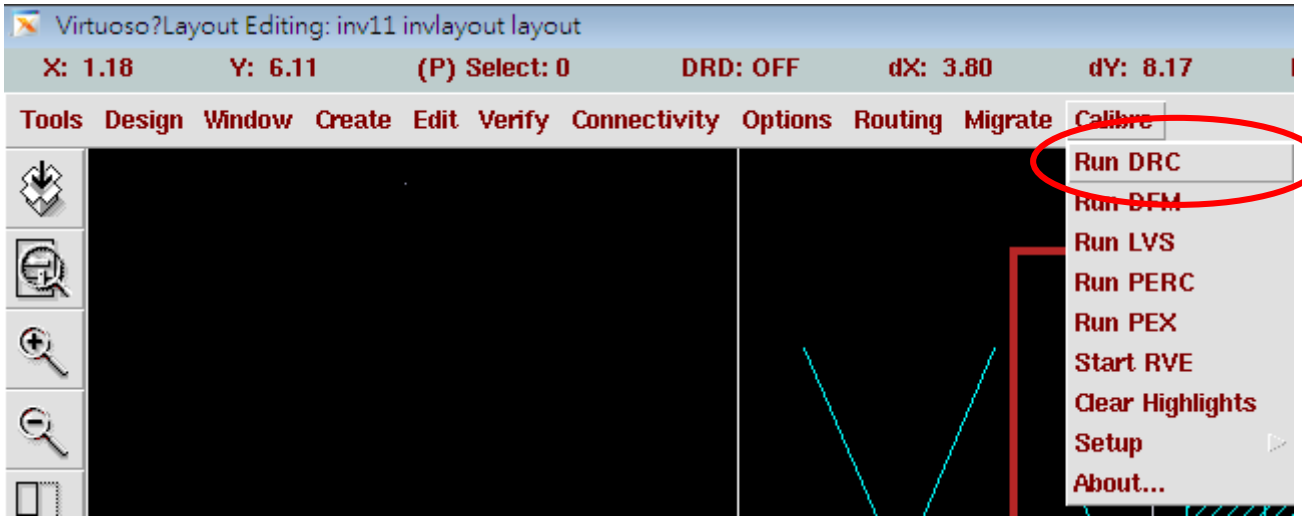


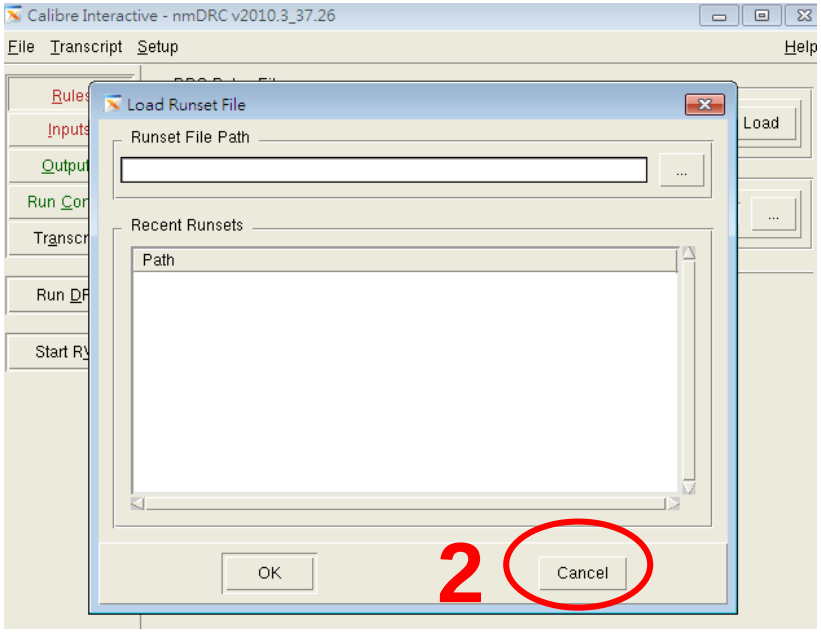
- **Hint: Do DRC**
  when you finish some part of your circuits.
- Connect m1 to m2
  - Stack layers
  - Metal1(bottom) → via1 → Metal2

Design Flow of Full-Custom Chip



Calibre DRC (1/5)

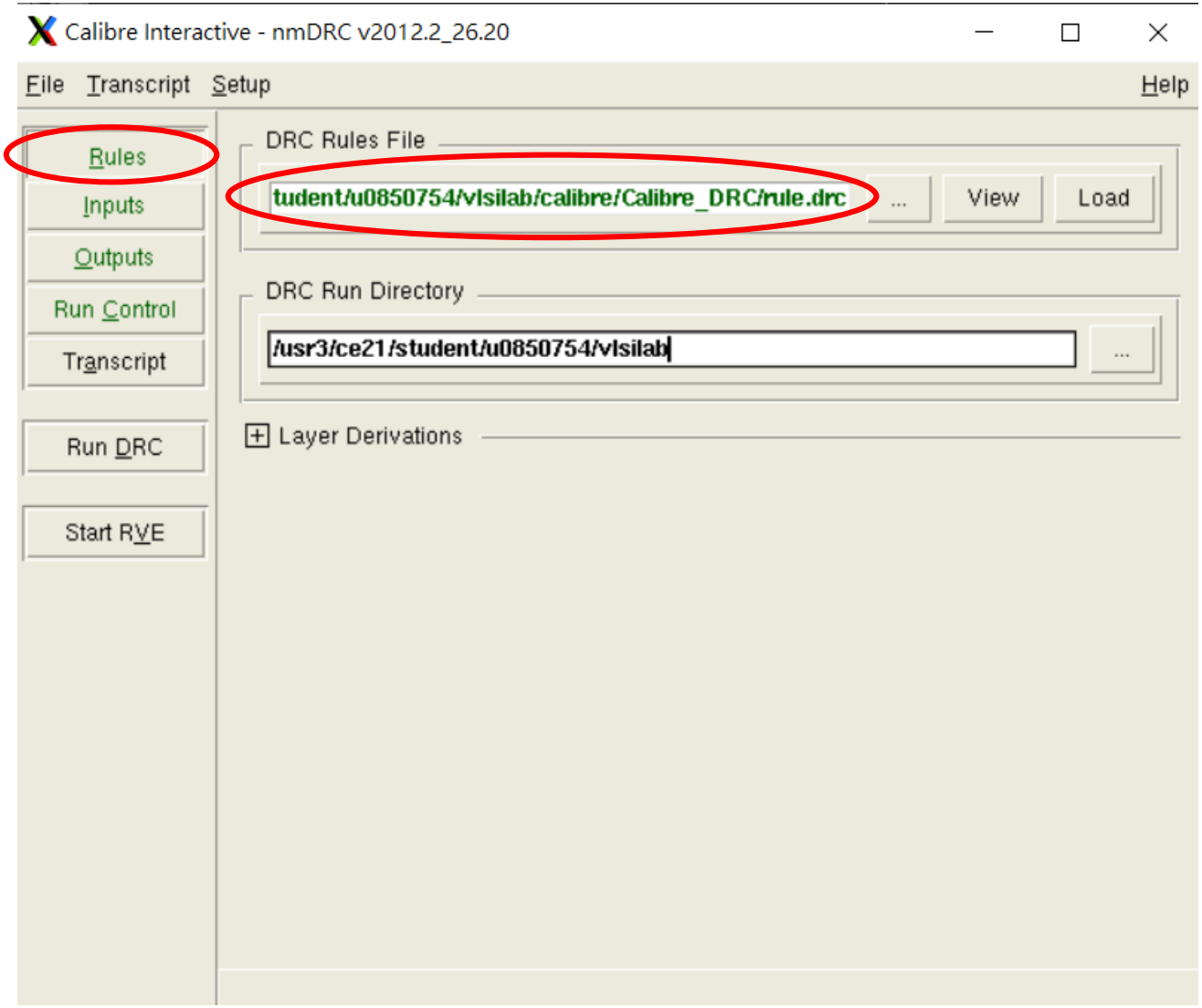




3 In the Rules tab

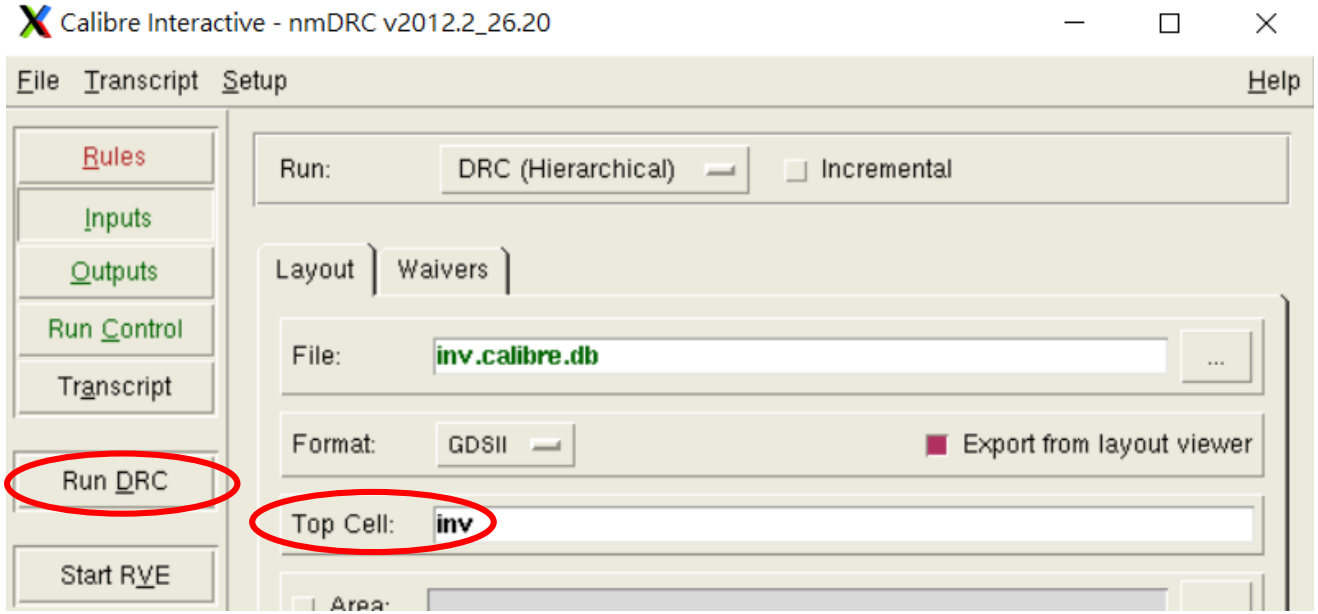
- Calibre-DRC Rules File field
  - Press the bottom "..."
  - Select rule.drc in the
  - ../calibre/Calibre_DRC/ directory
- Calibre-DRC Run Directory field
  - Select your work directory

Calibre DRC (2/5)



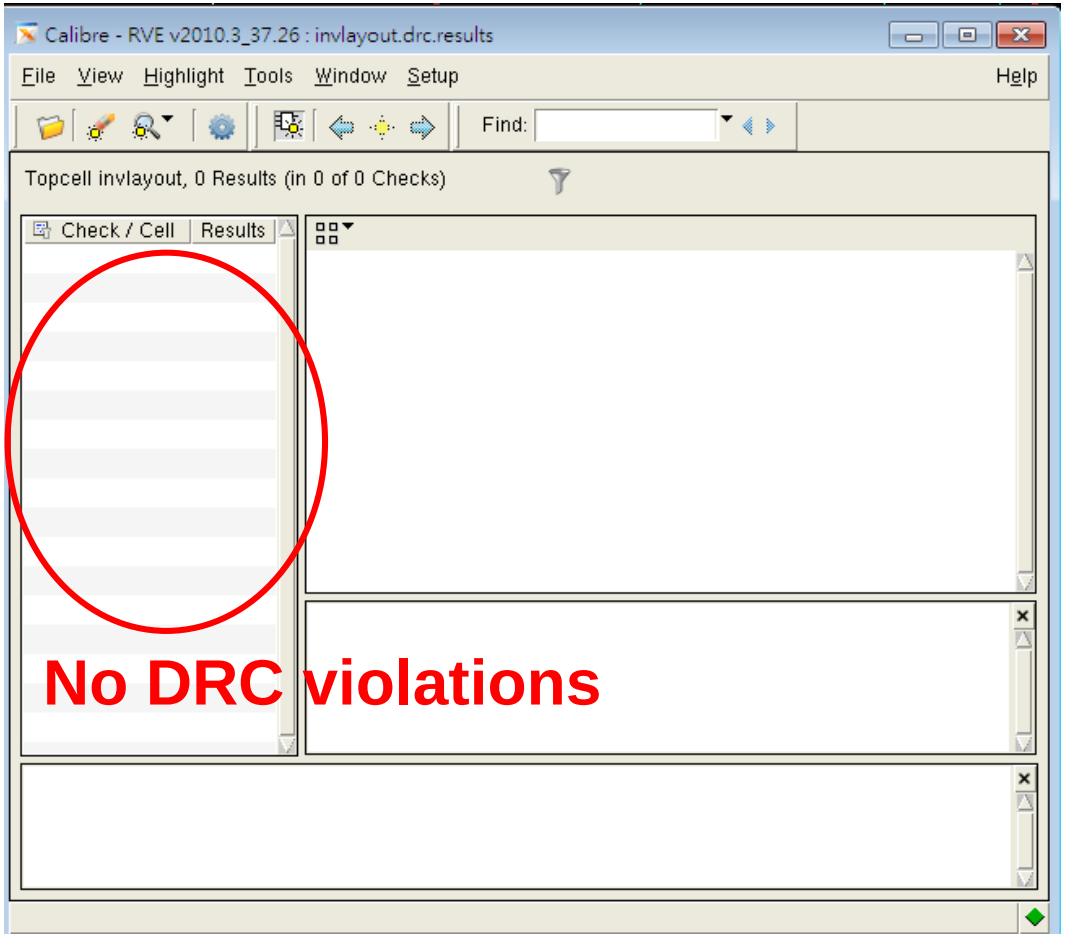
Calibre DRC (3/5)

- Use default setting



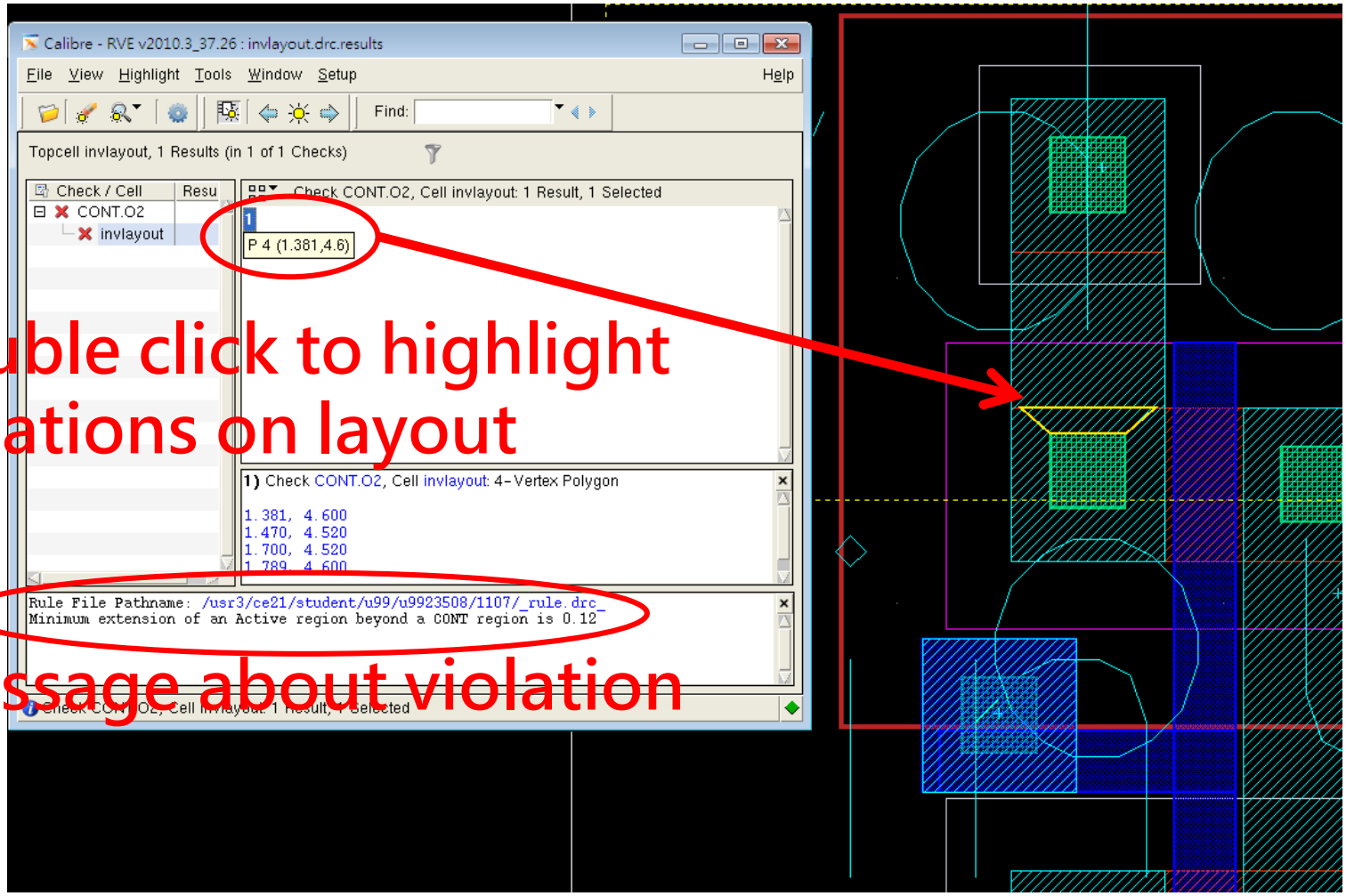
Calibre DRC (4/5)

- Collect all the design rule violation!

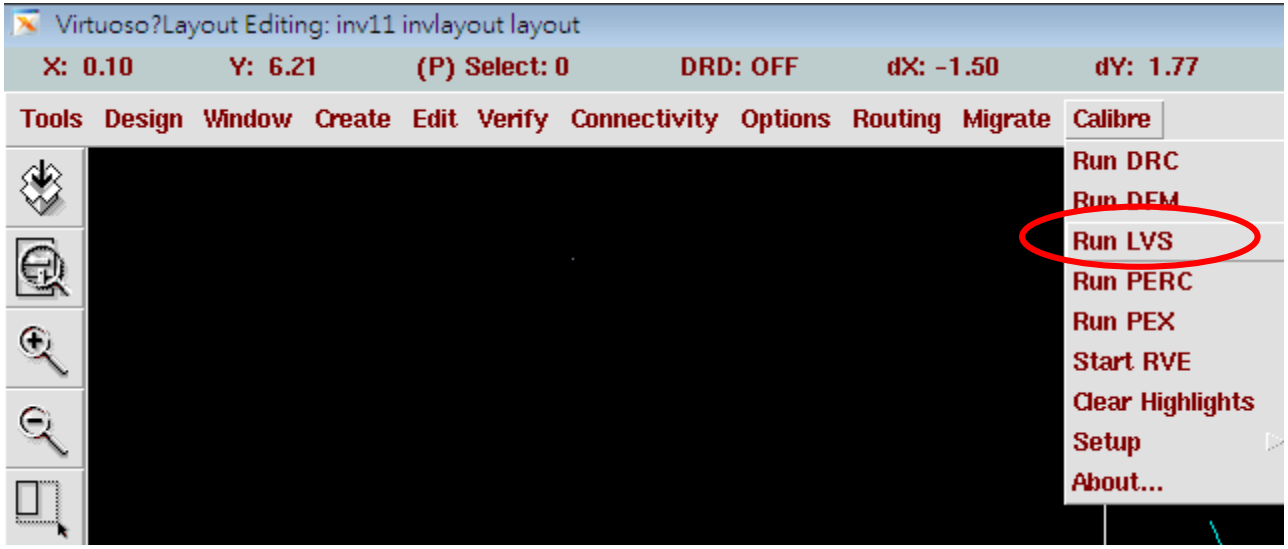


Calibre DRC (5/5)

- **DRC Violations**

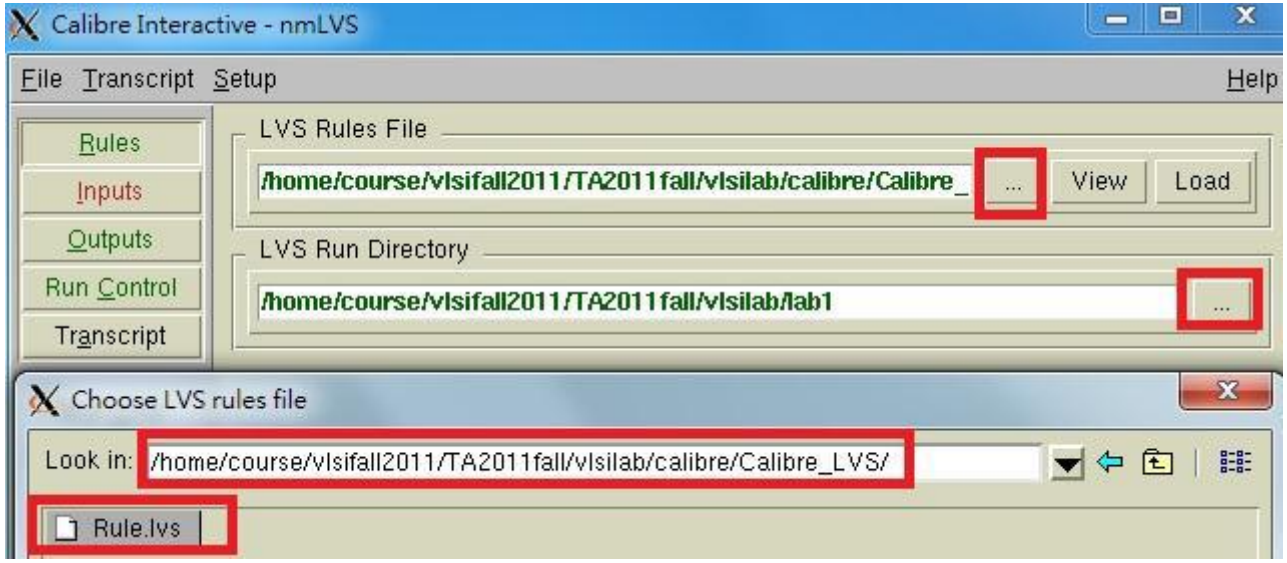


Calibre LVS (1/7)



Calibre LVS (2/7)

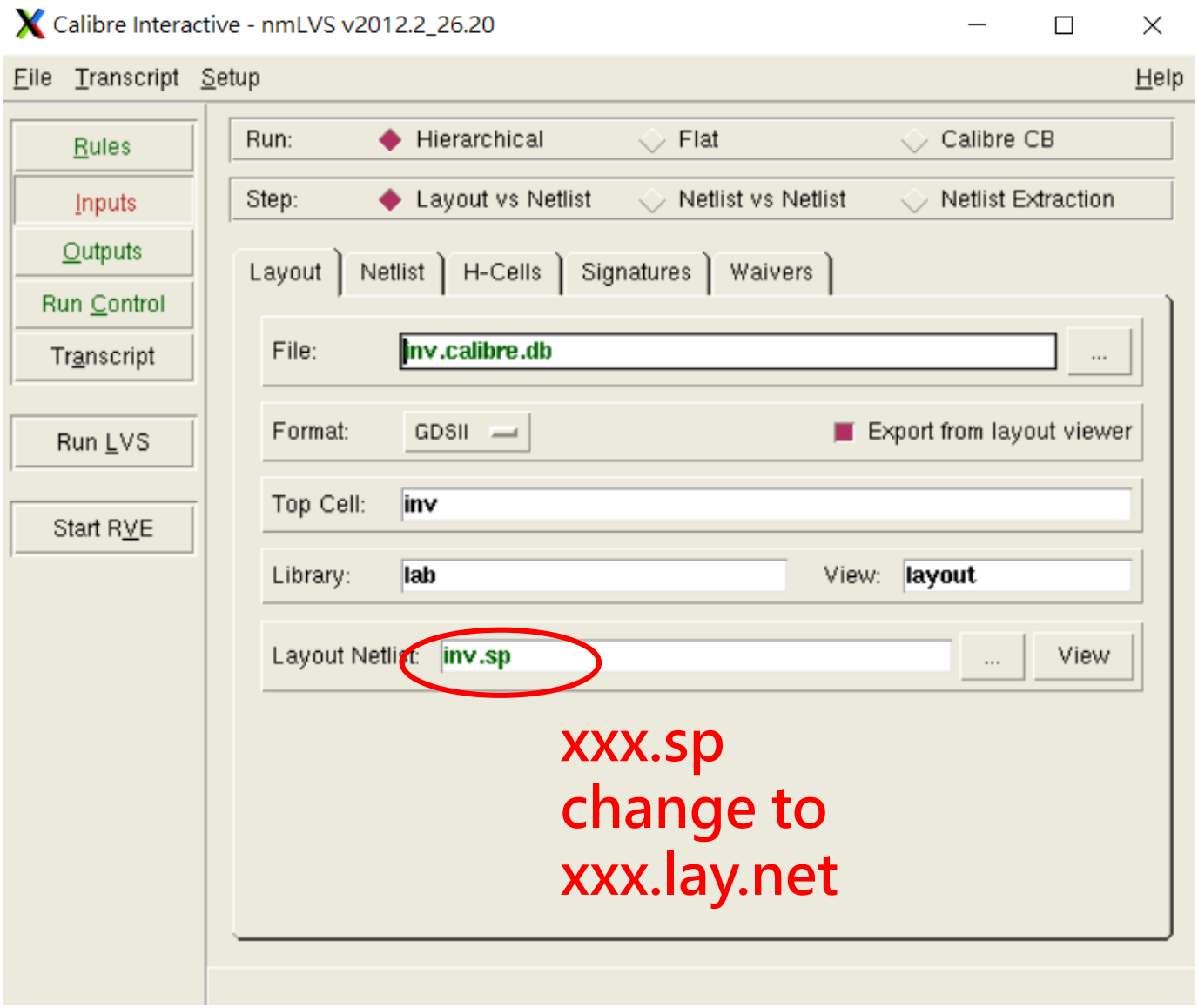
- In the Rules tab
  - Calibre-LVS Rules File field
    - Press the bottom "…"
    - Select Rule.lvs in the
    - ../calibre/Calibre_LVS/ directory
  - Calibre-LVS Run Directory field
    - Select your work directory



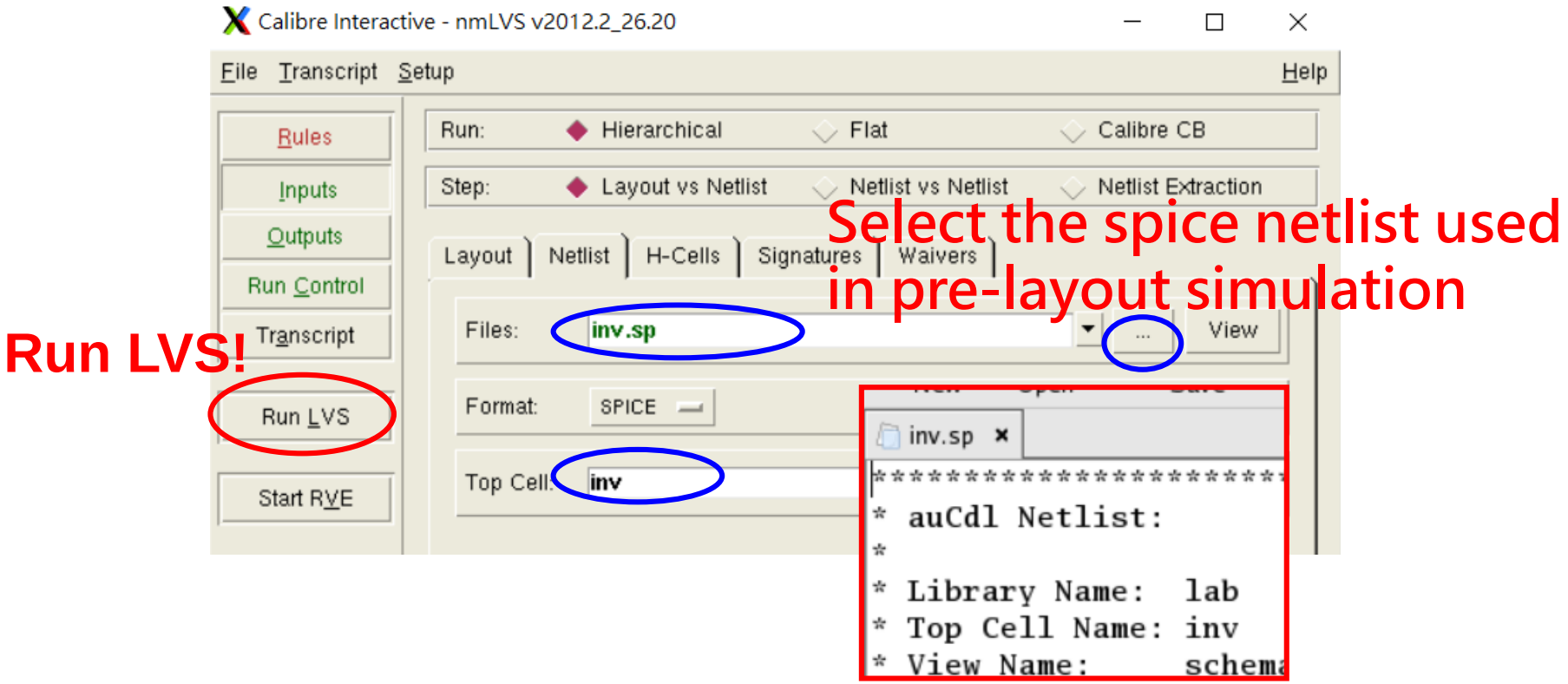
Calibre LVS (3/7)

- In the Inputs tab
  - Hierarchical : on
  - Layout VS Netlist : on
  - In the layout tab
    - Files : gds file name XXX.calibre.db
    - Export from layout viewer : on
    - Primary Cell : XXX
    - Layout Netlist : XXX.lay.net
  - In the Netlist tab
    - Files : inv.sp
    - Export from schematic viewer : off
    - Primary Cell : XXX

Calibre LVS (4/7)

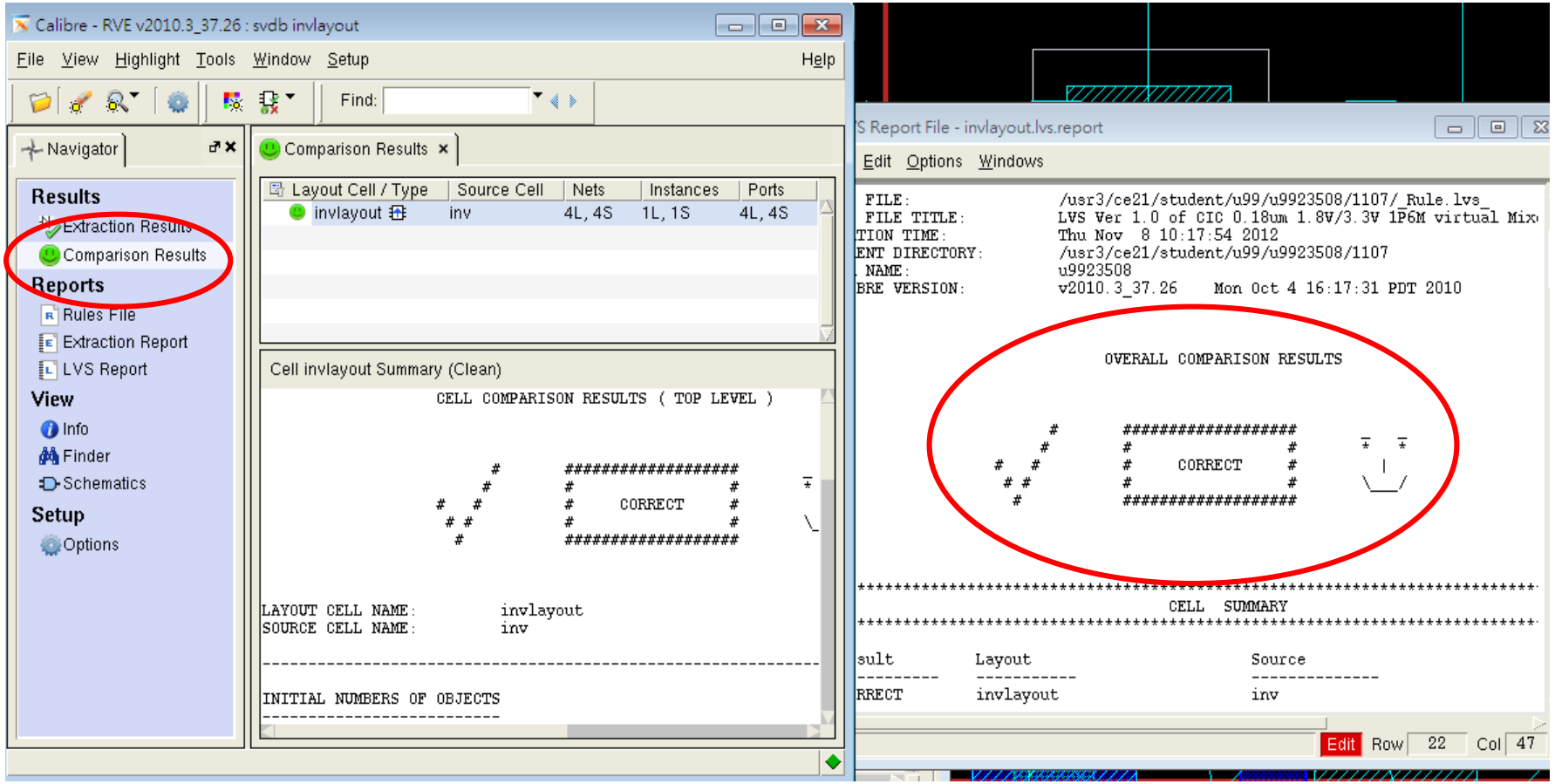


Calibre LVS (5/7)



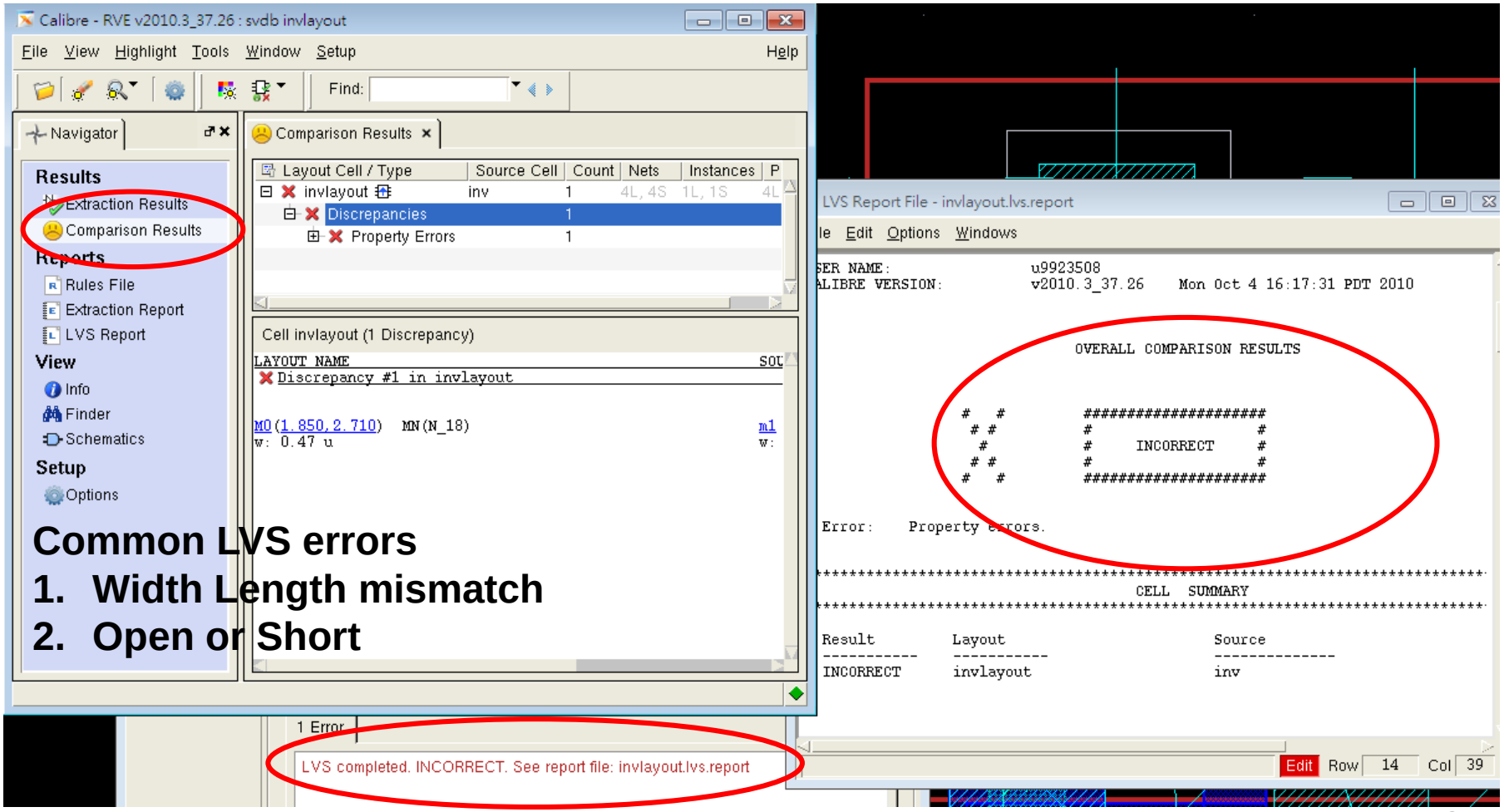
Calibre LVS (6/7)

- **The smile indicate comparison is correct**

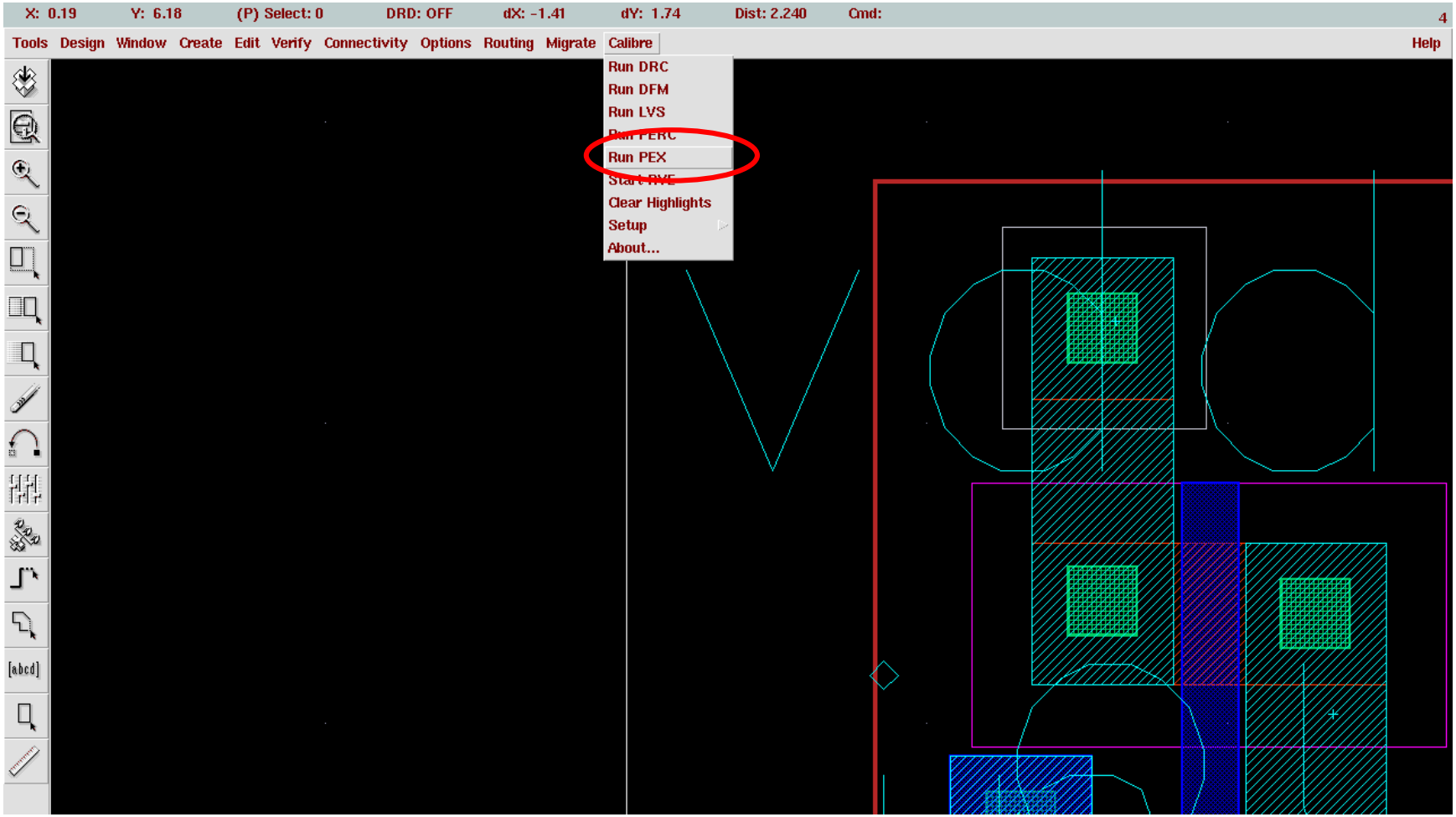


Calibre LVS (7/7)

- Incorrect results



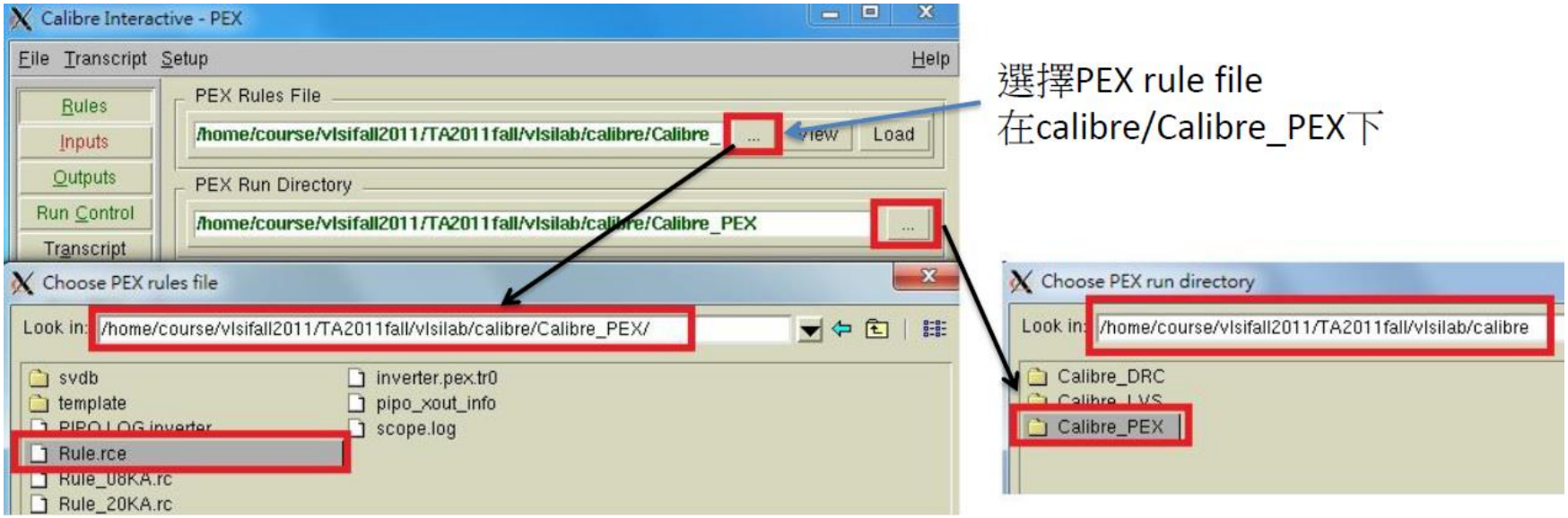
Calibre PEX (1/8)



Calibre PEX (2/8)

- In the Rules tab
  - Calibre-PEX Rules File field
    - Press the bottom "…"
    - Select Rule.rce in the
    - ../calibre/Calibre_PEX/ directory
  - Calibre-PEX Run Directory field
    - Select YOUR ACCOUNT /…/calibre/Calibre_PEX/ as your directory
    - Please check that your Run Directory includes "Rule.rce" 、" Rule_08KA.rc", and "Rule_20KA.rc"
    - 注意 : 這裡和DRC、LVS不同，不是選擇工作資料夾，而是選擇包含Rule.rce，Rule_08KA.rc ，Rule_20KA.rc三個檔案的資料夾。在這裡是Calibre_PEX，不過萃取出的spice file就會擺在Calibre_PEX裡面，如果你覺得不方便，可以把上述三個檔案複製到你的工作資料夾。

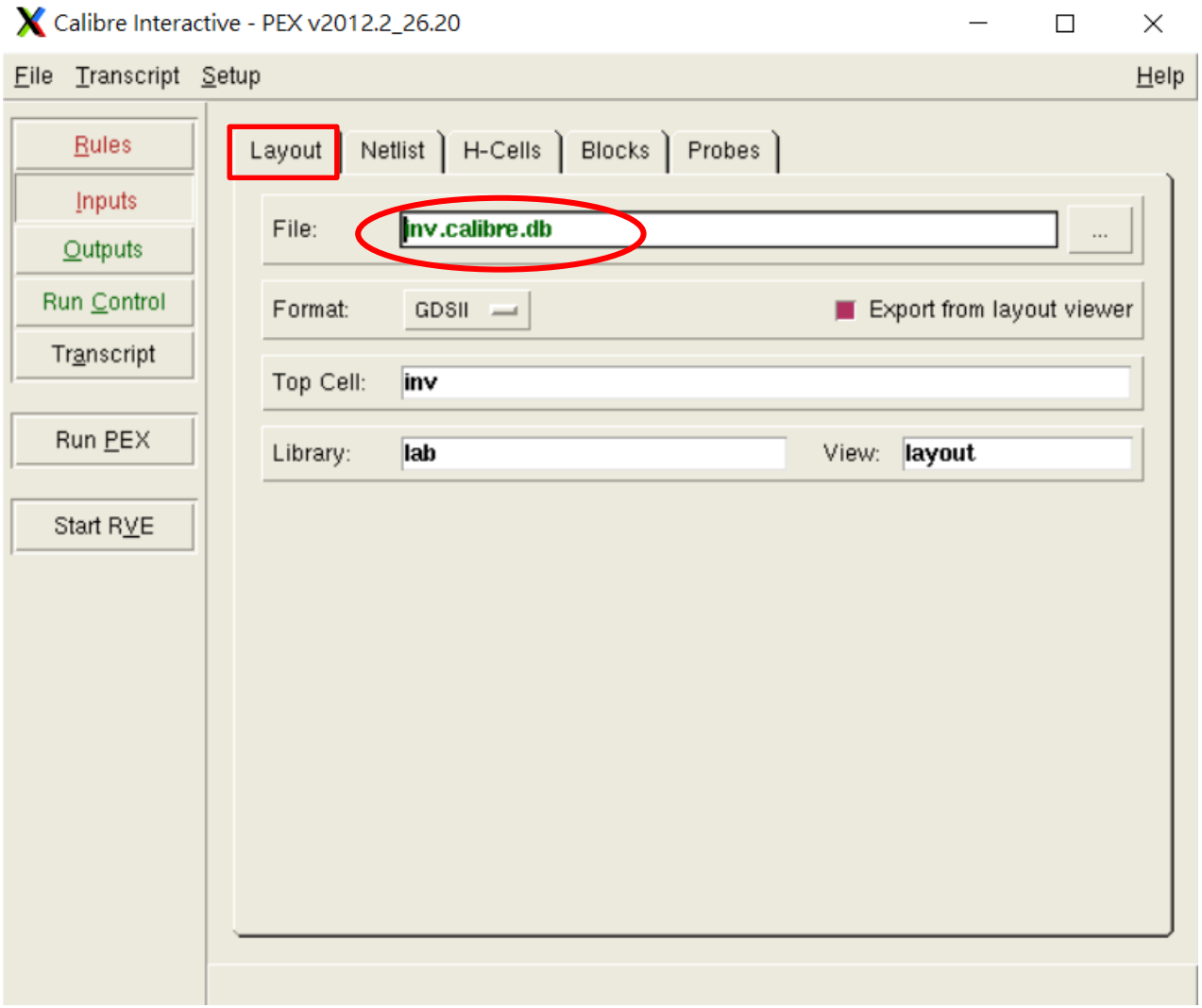
Calibre PEX (3/8)



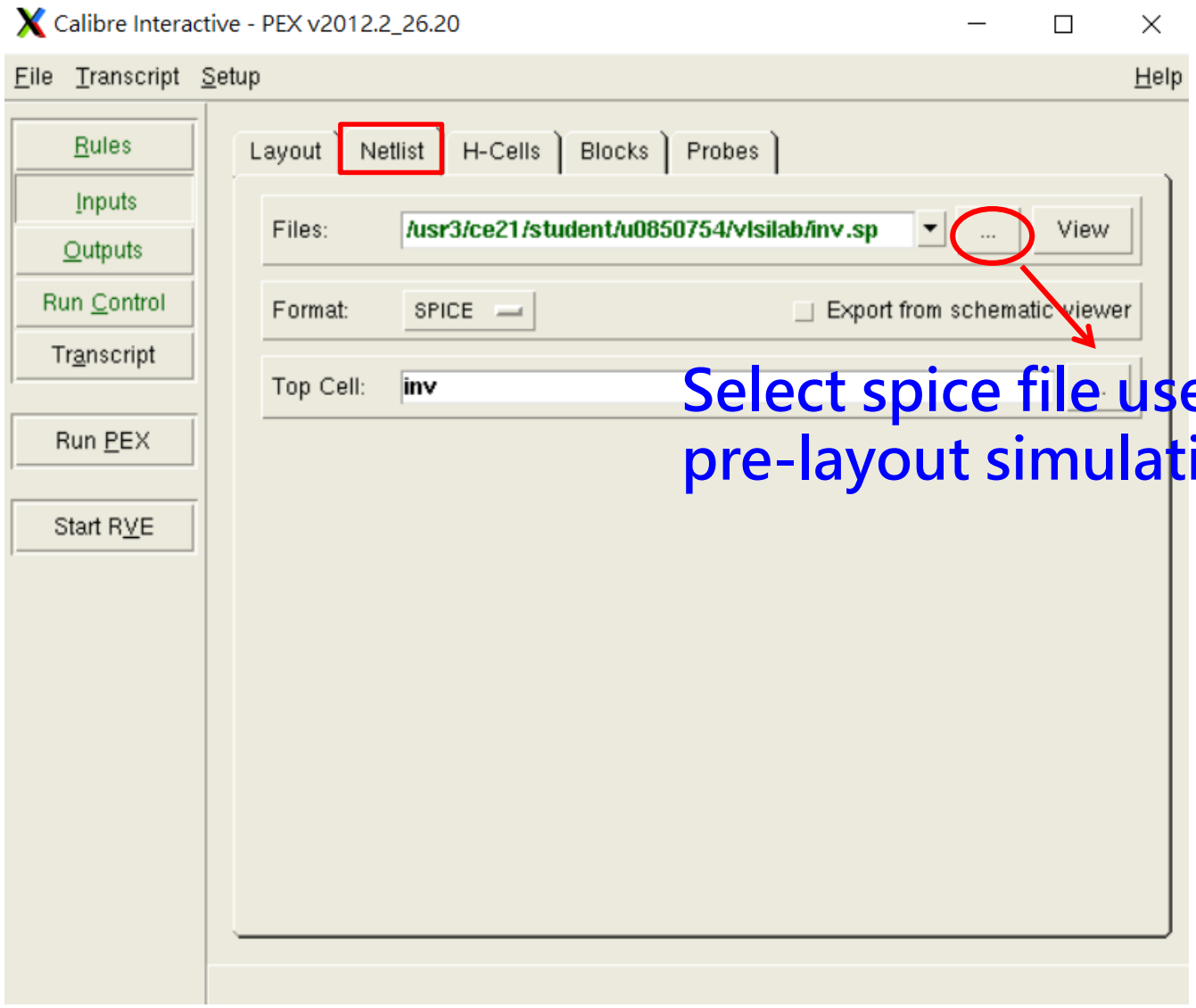
Calibre PEX (4/8)

- In the Inputs tab
  - In the layout tab
    - Files : gds file name XXX.calibre.db
    - Export from layout viewer : on
    - Primary Cell : XXX
  - In the Netlist tab
    - Files : inv.sp
    - Export from schematic viewer : off
    - Primary Cell : XXX

Calibre PEX (5/8)

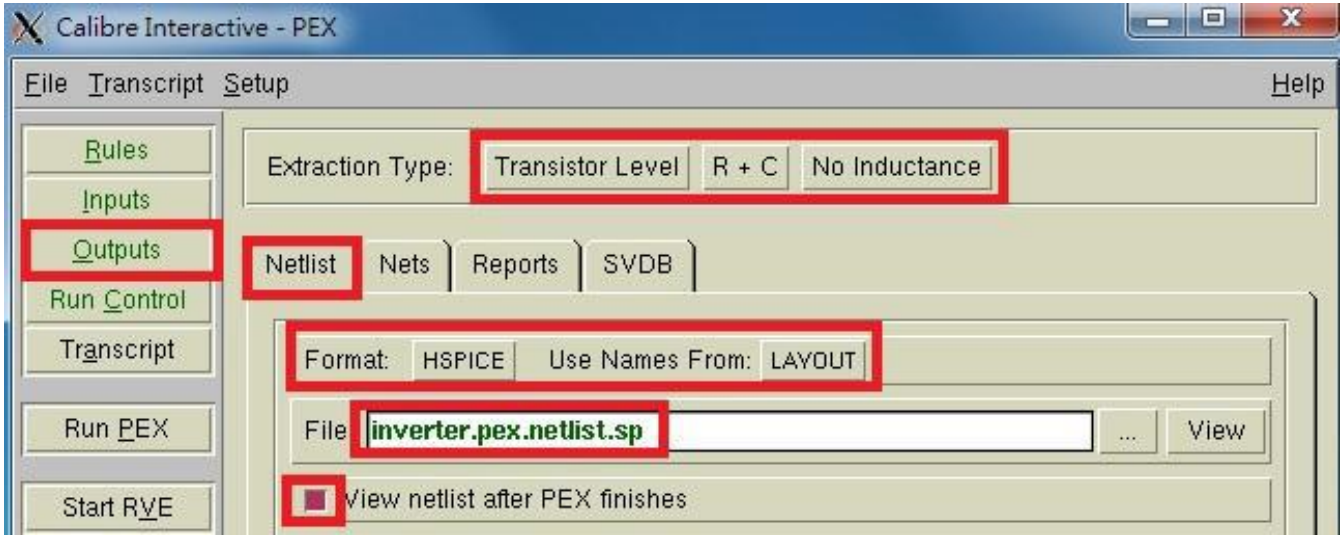


Calibre PEX (6/8)

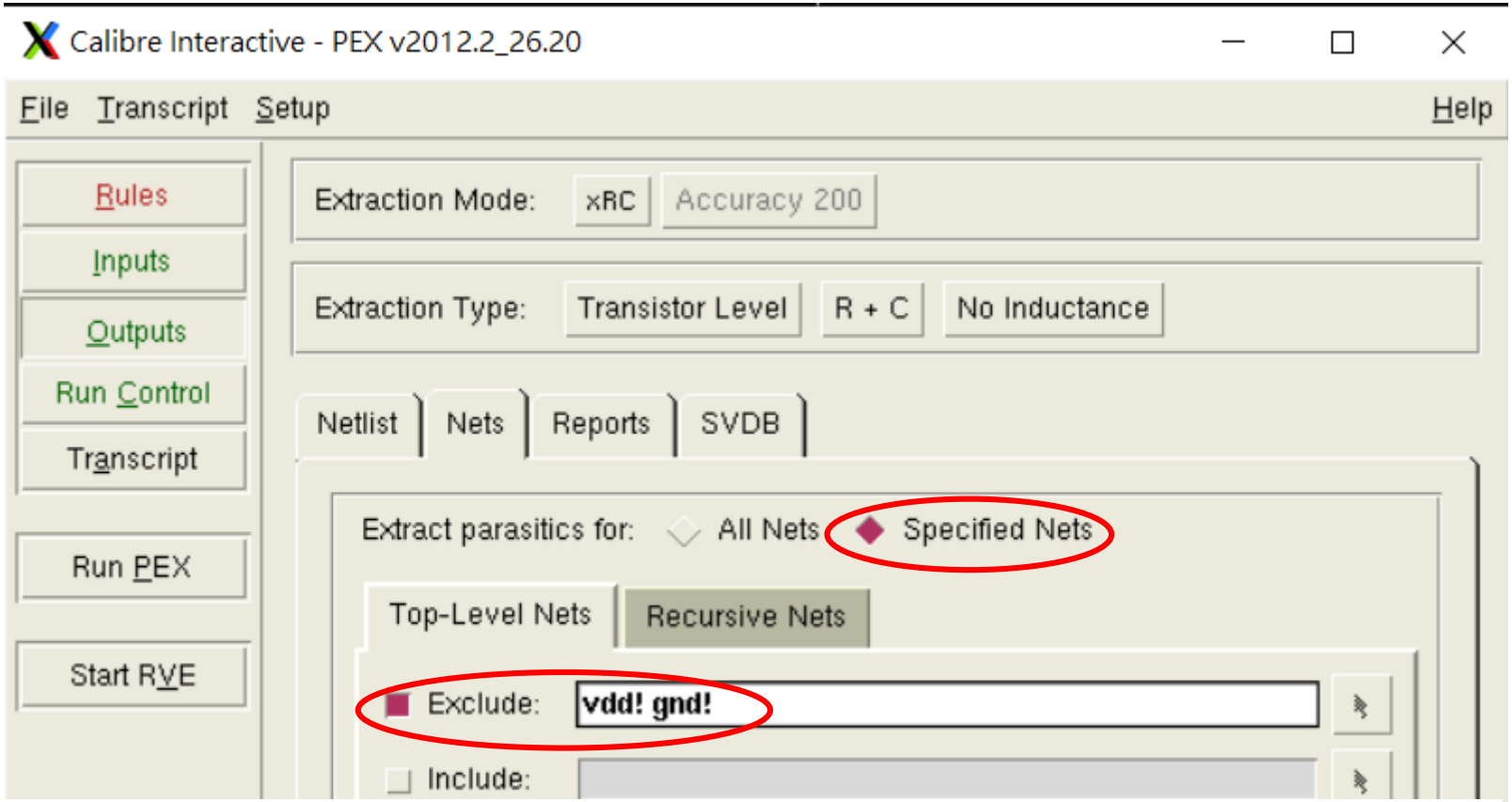


Calibre PEX (7/8)

- In the output tab
  - Extraction Type:
    - RC – Distributed RC
  - In the PEX Netlist field
    - Format : hspice – on
    - Name : layout – on
    - File : default file name+.sp
  - View Netlist after PEX finishes : on



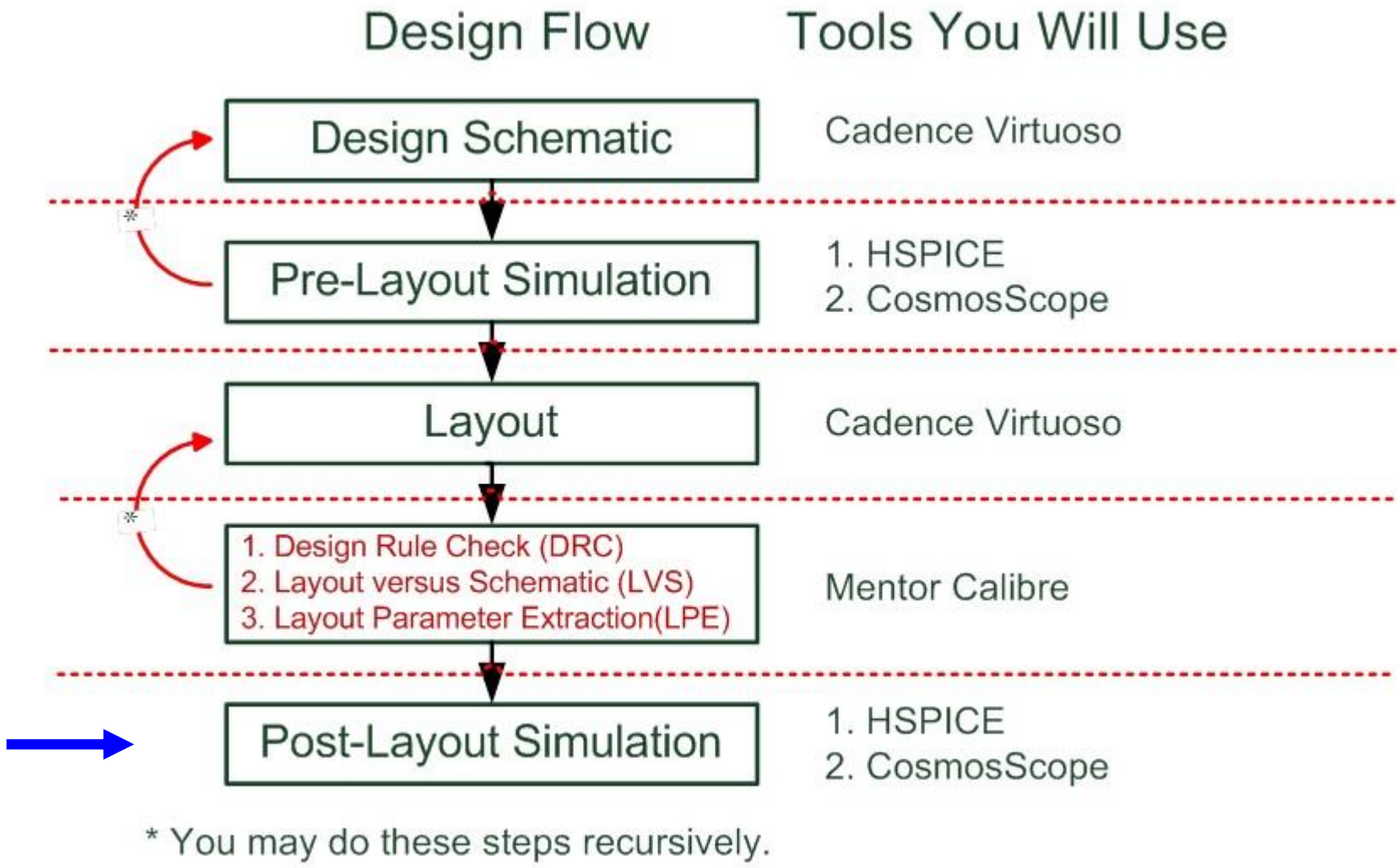
Calibre PEX (8/8)



Exclude 打上 vdd! gnd!

按下Run PEX，可能會有很多warning，多半可以不用在意。
輸出的新的檔案inverter.pex.netlist擺在你之前選的PEX Run Directory下

Design Flow of Full-Custom Chip



Post-Layout Simulation

- After PEX, inverter.pex.netlist.sp will be obtained
- Use inverter.pex.netlist.sp in Hspice perform post-layout simulation and get more realistic results
- Remember to check the order of subckt name between simulation file and inverter.pex.netlist.sp.
- 提醒：只要layout電路有做更動，一定要照 DRC→LVS→PEX 步驟重做。

Create Spice Netlist for post simulation

```
54@ce38 Calibre_PEX]$ gedit sim_inv.sp &
```

sim_inv.sp

```
**sim_inv

.protect
.lib 'cic018.l' tt
.unprotect

.include 'inv.pex.netlist.sp'

vvdd vdd! 0 1.8
vgnd gnd! 0 0

xinv GND! VDD! OUT IN inv

vvin in 0 pulse (0 1.8v 0 1n 1n 49n 100n)

.option post
.op
.tran 0.1n 500n

.end
```

Title

include library

Define voltage

Call subcircuits

Define input waveform

Demo steps

1. Check Schematic
2. Check Layout
3. Run DRC
4. Run LVS
5. Measure area of layout
6. Check post-sim waveform