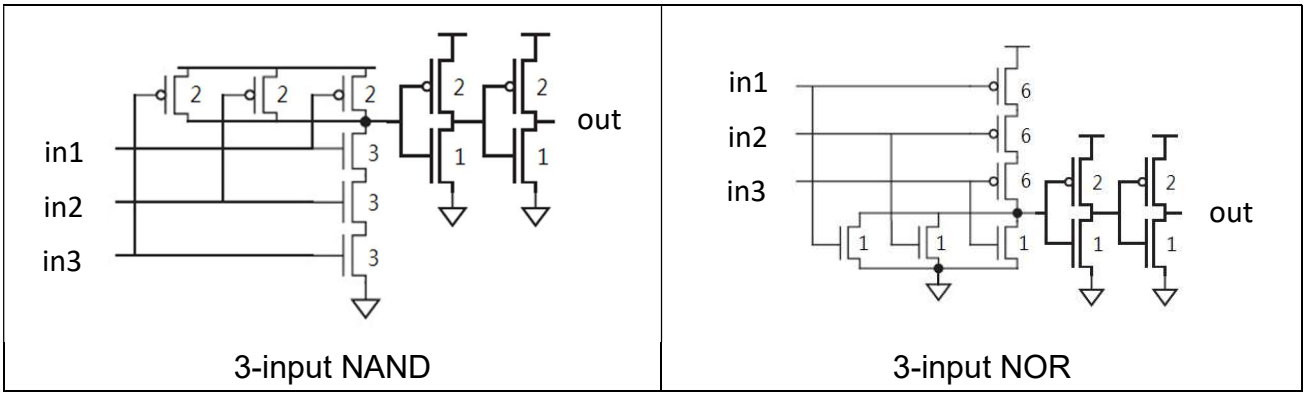
VLSI Lab2

I. Design a 3-input NAND gate and 3-input NOR gate.

Use PMOS W/L = 0.94um / 0.18um, NMOS W/L = 0.47um / 0.18um as the size of inverter.

A. Design a 3-input NAND and 3-input NOR, and add inverters as loading.

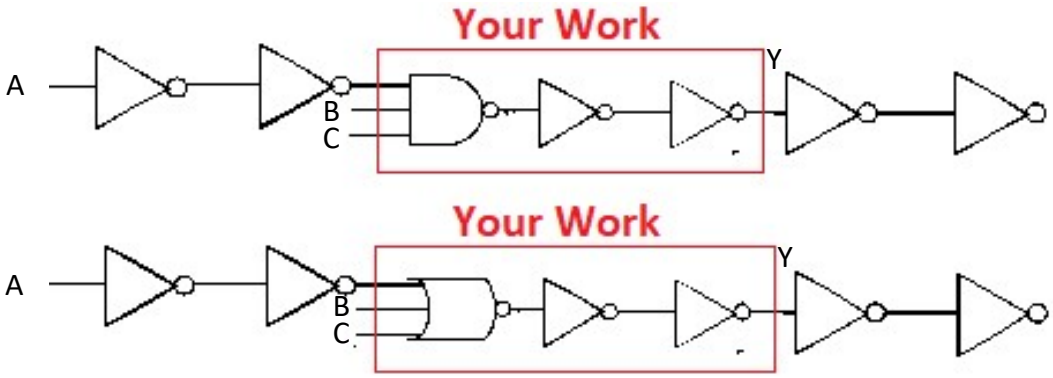
✓ **Paste layout screenshot with ruler in your report.**



3-input NAND | 3-input NOR

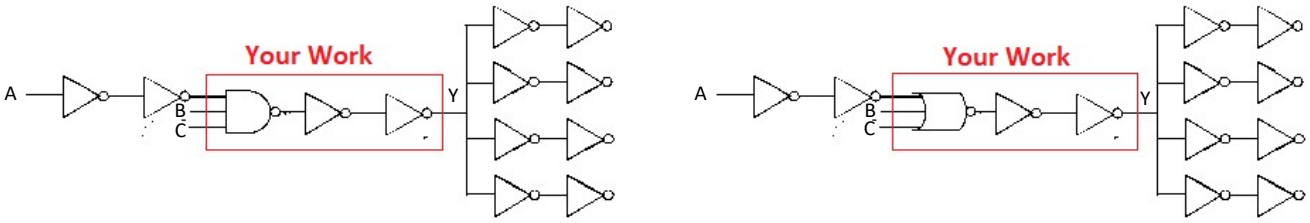
B. Add inverters on 3-input NAND and 3-input NOR as loading.

Hint: You can use inv.sp after PEX in Lab1.



C. Add inverters and FO4 on 3-input NAND and 3-input NOR as loading.

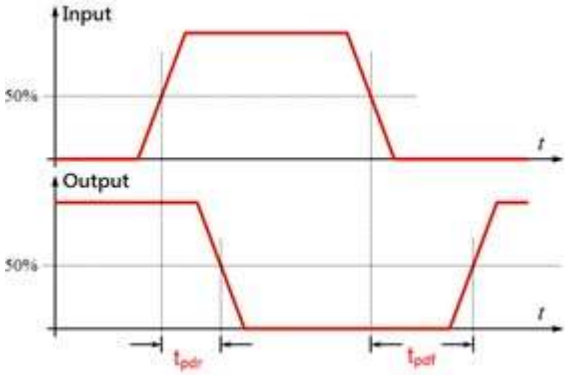
Hint: You can use inv.sp after PEX in Lab1.



D. Fill out following tables with Post-sim.

[Refer to statement of cell library datasheet in textbook CH3 p117, p118.]

✓ **Paste the following tables in your report.**



t_{pdr} = rise time propagation-delay

t_{pdf} = fall time propagation-delay

Using **cscope** to **measure the propagation-delay time** of waveforms, the reason is that it will add extra resistance and capacitance when loading another inverter. Although the delay of loading part is larger, the waveform of that is more stable, almost no glitch exists in the waveform.

Input signal:
Rise time = 1ns
Fall time = 1ns

NAND3	Delay(output loading: an inverter)	Delay(output loading: FO4)
A↑, B=1, C=1 → Y↓ (t_{pdr}_A)		
A ↓B=1, C=1 → Y↑, (t_{pdf}_A)		
A=1, B↑, C=1 → Y↓ (t_{pdr}_B)		
A=1, B↓, C=1 → Y↑ (t_{pdf}_B)		

NOR3	Delay(output loading: an inverter)	Delay(output loading: FO4)
A↓, B=0, C=0 → Y↑ (t_{pdr}_A)		
A↑, B=0, C=0 → Y↓ (t_{pdf}_A)		
A=0, B↓, C=0 → Y↑ (t_{pdr}_B)		
A=0, B↑ C=0 → Y↓ (t_{pdf}_B)		

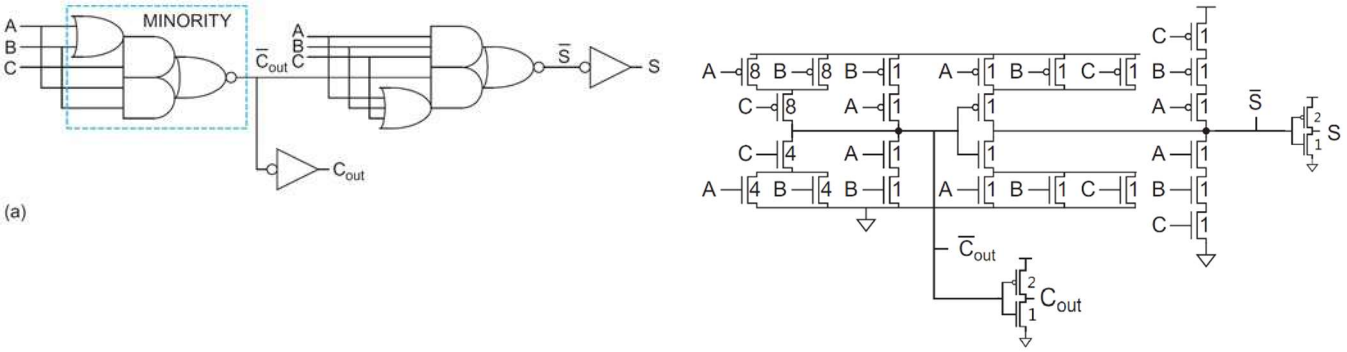
E. Show waveform of the above tables to verify your design.

F. Measure area, delay and power of the circuit.

II. Design a 1-bit full adder.

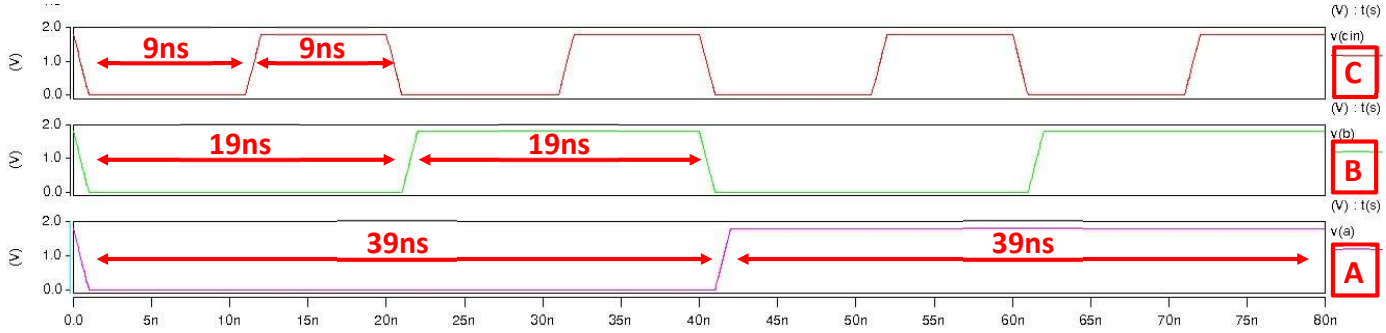
A. Design a 1-bit full adder based on page390, 391 in the textbook.

✓ **Paste layout screenshot with ruler in your report.**



Full adder for carry-ripple operation [from Fig.10.4 on P.390]

B. Show a waveform to verify your design (Set the input as below).

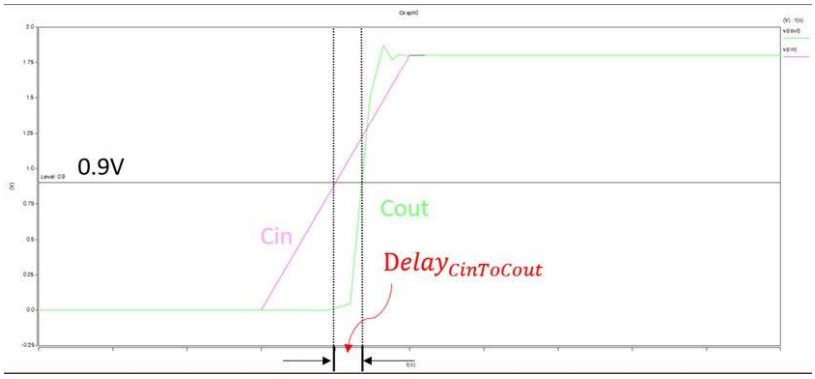


A	B	C_{in}
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Measure $Delay_{CinToCout}$

Delay time = 0ns
Rise time = 1ns
Fall time = 1ns

C. Measure area, delay and power of 1-bit full adder.



III. Question of the lab

✓ **Write down your observation in your report.**

Compare the delay between NAND3 / NOR3 with two inverters output loading and with FO4 output loading. Find the relationship between them.

IV. Grading Policy

A. Pre-sim waveform: 11% (NAND 3% + NOR 3% + 1-bit Full adder 5%)

B. DRC: 7% (NAND 2% + NOR 2% + 1-bit Full adder 3%)

- **Metal 3 ~ Metal 6 are forbidden to use in this lab.**

C. LVS: 7% (NAND 2% + NOR 2% + 1-bit Full adder 3%)

D. Post-sim waveform: 30%

- NAND / NOR, @ 4%
- NAND / NOR with two inverters loading, @ 4%
- NAND / NOR with FO4 loading, @ 4%
- 1-bit Full adder 6%

E. Performance of post-sim: 25% (NAND 6% + NOR 6%+ 1-bit Full adder 13%)

- For NAND and NOR

$$Figure\ of\ Merit\ (FoM) = Power \times \frac{t_{pdr\_A(inv\ loading)} + t_{pdf\_A(inv\ loading)}}{2} \times Area$$

- For 1-bit Full adder

$$Figure\ of\ Merit\ (FoM) = Power \times Delay_{CinToCout} \times Area$$

F. Report: 20%

1. Layout with ruler: 7% (NAND 2% + NOR 2%+ 1-bit Full adder 3%)
2. Post-sim waveform: 7% (NAND 2% + NOR 2%+ 1-bit Full adder 3%)
3. NAND + NOR table: 4%
4. Question: 2%

V. Demo time: 21Oct (Wed) 15:30 ~ 18:30

You have "one" chance to demo only!

After deadline, any requests for demo are denied.

VI. Report hand-in deadline: 21Oct (Wed) 23:59 on New E3

After deadline, any requests for handing in report are denied.

VII. Appendix

Power measurement by Hspice

```
.tran 0.1n 200n
.meas tran total_cur integ par('-i(vvdd)')
.meas tran total_pwr param='1.8*total_cur'
```

where "vvdd" is element name of power supply.