VLSI Lab3

I. Design a D flip-flop [Refer to Figure 9.19(b) in Textbook] (30%)

Use PMOS W/L = 0.94um / 0.18um, NMOS W/L = 0.47um / 0.18um
Set clock cycle = 10ns (duty cycle = 50%, rise time / fall time = 1ns)
Please add two inverters on each input and outputs as loading.
Hint: You can use inv.sp after PEX in Lab1.

✓ Paste layout screenshot with ruler in your report.

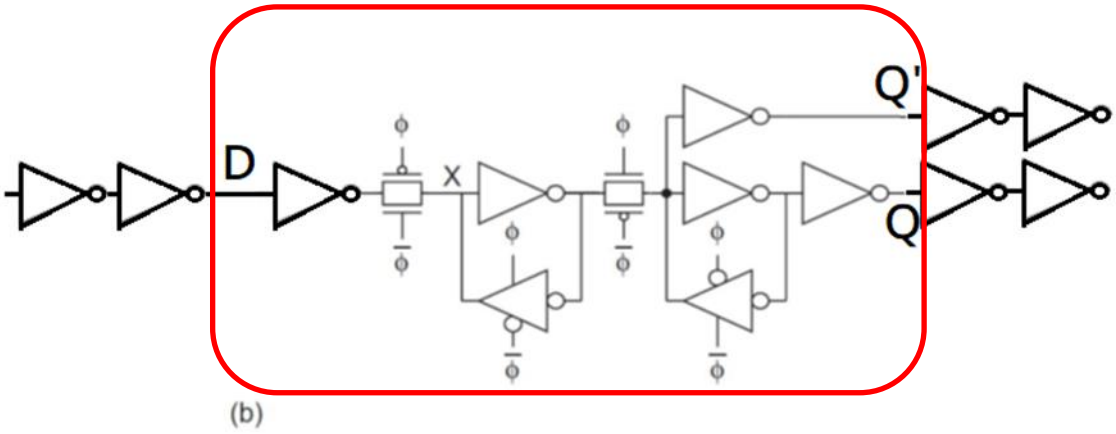


Figure. 9.19(b) D flip-flops

A. Measure the delays (a) t_{pcq} (b) t_{ccq} (c) t_{setup} for post-sim and explain the procedure for t_{setup}. (See Appendix)

✓ Paste post-sim waveform with measure results (t_{pcq}, t_{ccq}, t_{setup_1x}, $t_{setup\_1.1x}$) and explain the procedure for t_{setup} in your report.

Question 1: What is the difference between D flip-flop and D Latch? (Write in your report)

II. Design a 4-bit counter using D flip-flop count from 0000 to 1111. (40%)

Use PMOS W/L = 0.94um / 0.18um, NMOS W/L = 0.47um / 0.18um
Set clock cycle = 10ns (duty cycle = 50%, rise time / fall time = 1ns)
(Hint: There are more than one way to design it, but you can only give input signals at the first stage of design)
Please add two inverters on each outputs as loading.(except clk)
Hint: You can use inv.sp after PEX in Lab1.

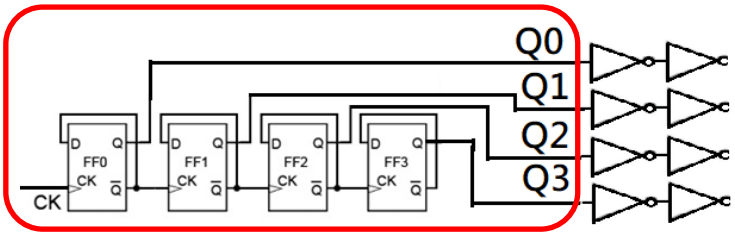


Figure. 4-bit counter reference circuit

- ✓ Explain your design with schematic in your report.
- ✓ Paste layout screenshot with ruler in your report.

A. Measure the $\mathbf{Delay_{0111\rightarrow1000}}$ for post-sim as follows.

- ✓ Paste post-sim waveform (include at least 0000 -> 0001 ->…-> 1110 -> 1111 -> 0000) and measure result ($\mathbf{Delay_{0111\rightarrow1000}}$) in your report.

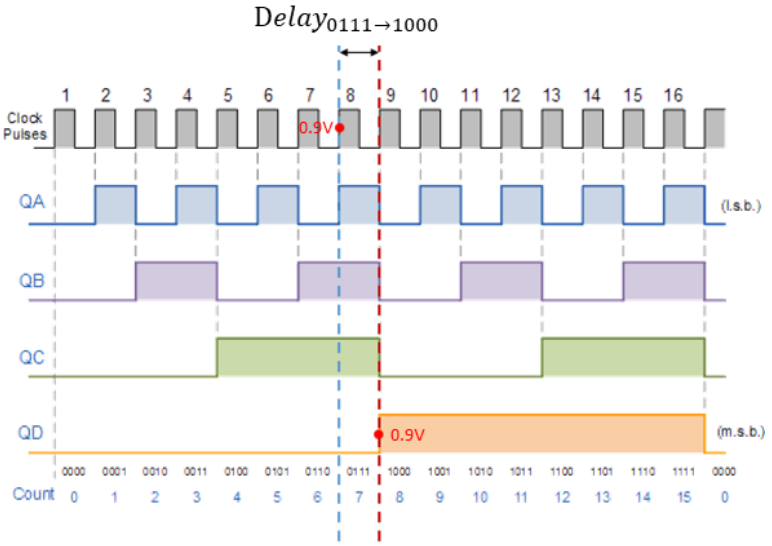


Figure. 4-bit counter delay measurement

Question 2: What is the difference between combinational circuit and sequential circuit? (Write in your report)

III. [BONUS] Design a BCD ripple counter, the counter count from 0000 to 1001 (0~9) and then restart from 0000. (30%)

Use PMOS W/L = 0.94um / 0.18um, NMOS W/L = 0.47um / 0.18um
Set clock cycle = 10ns (duty cycle = 50%, rise time / fall time = 1ns)
(Hint: You may use resettable D flip-flops and comparator for your design.)
Please add two inverters on each outputs as loading.(except clk)

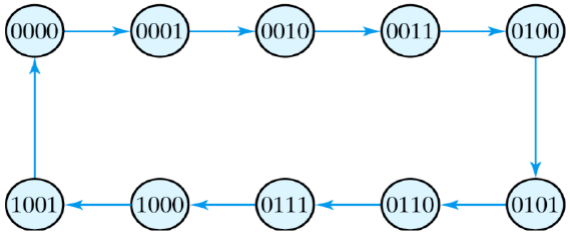


Figure. BCD counter state diagram

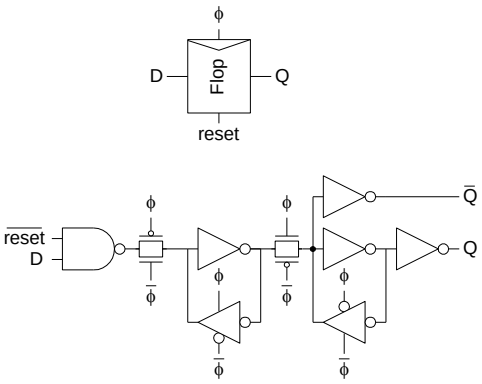


Figure. 9.24 Resettable flip-flops [p.355 in textbook]

- ✓ Explain your design with schematic in your report.
- ✓ Paste layout screenshot with ruler and post-sim waveform (include at least 0000 -> 0001 ->…-> 1000 -> 1001 -> 0000) in your report.

IV. Grading Policy (Demo: A~C , Report: D)

- ➢ **Metal 3 ~ Metal 6 are forbidden to use in this lab**

A. D flip-flop: 30%

1. Schematic & pre-sim waveform & hspice: 5%
2. Layout & DRC pass & LVS pass: 5%
3. Post-sim waveform & hspice (include measure t_{pcq}, t_{ccq}, t_{setup}): 10%
4. Performance of post-sim: 10%

$$[\ \boldsymbol{Figure\ of\ Merit\ (FoM) = t_{ccq} \times Area}\ ]$$

B. 4-bit Counter: 40%

1. Schematic & pre-sim waveform & hspice: 10%
2. Layout & DRC pass & LVS pass: 10%
3. Post-sim waveform & hspice (include at least 0000 -> 0001 ->…-> 1110 -> 1111 -> 0000 & measure $\mathbf{Delay_{CLK\_posedge \rightarrow 1000}}$): 10%
4. Performance of post-sim: 10%

$$[\ \boldsymbol{Figure\ of\ Merit\ (FoM) = Delay_{CLK\_posedge \rightarrow 1000} \times Area}\ ]$$

C. [BONUS] BCD counter: 30%

1. Schematic & pre-sim waveform & hspice: 10%
2. Layout & DRC pass & LVS pass: 10%
3. Post-sim waveform & hspice (include at least 0000 -> 0001 ->…-> 1000 -> 1001 -> 0000): 10%

D. Report: 30% + [BONUS] 5%

1. D flip-flop: 15%
   - Layout screenshot with ruler: 2%
   - Post-sim waveform & measure the delays (t_{pcq}, t_{ccq}, t_{setup_1x}, $t_{setup\_1.1x}$): 6%
   - Explain the procedure for t_{setup}: 3%
   - Question1: 4%
2. 4-bit Counter: 15%
   - Explain your design with schematic: 3%
   - Layout screenshot with ruler: 2%
   - Post-sim waveform (include at least 0000 -> 0001 ->…-> 1110 -> 1111 -> 0000): 3%
   - Measure the delay ($\mathbf{Delay_{0111 \rightarrow 1000}}$): 2%
   - Question2: 5%

3. [BONUS] BCD counter: 5%
   - Explain your design with schematic: 2%
   - Layout screenshot with ruler & post-sim waveform (include at least 0000 -> 0001 ->…-> 1000 -> 1001 -> 0000): 3%

V. Demo time: 11/4 (Wed.) 15:30 ~ 18:30 You only have "one" chance to demo!

After deadline, any requests for demo are denied.

VI. Report hand-in deadline: ~11/4(Wed.) 23:59 on new E3

After deadline, any requests for handing in report are denied.

VII. Appendix

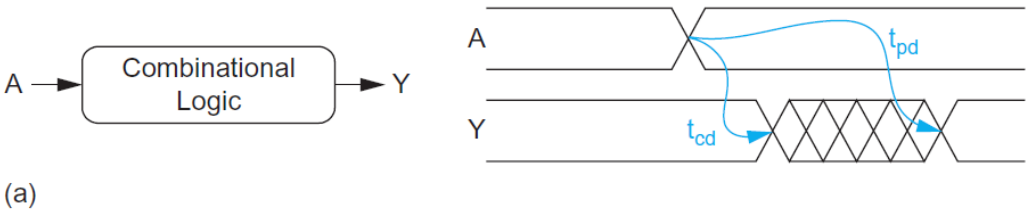
Power measurement by Hspice

```
.tran 0.1n 1u
.meas tran total_cur integ par('-i(vvdd)')
.meas tran total_pwr param='1.8*total_cur'
```

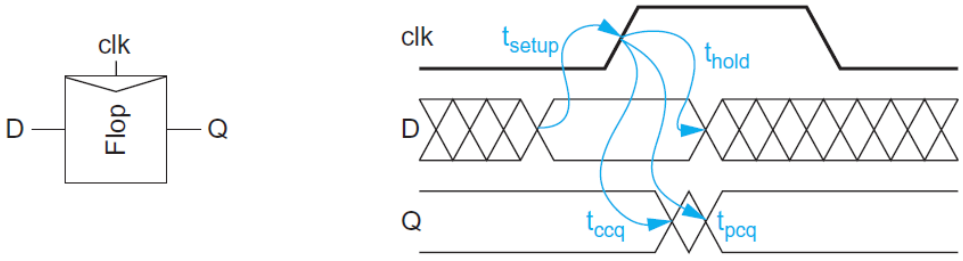
where "vvdd" is element name of power supply.

TABLE 10.1 Sequencing element timing notation

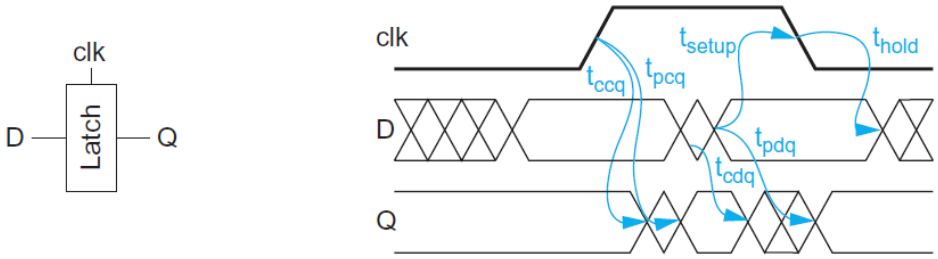
Term	Name
t_{pd}	Logic Propagation Delay
t_{cd}	Logic Contamination Delay
t_{pcq}	Latch/Flop Clock-to-Q Propagation Delay
t_{ccq}	Latch/Flop Clock-to-Q Contamination Delay
t_{pdq}	Latch D-to-Q Propagation Delay
t_{cdq}	Latch D-to-Q Contamination Delay
t_{setup}	Latch/Flop Setup Time
t_{hold}	Latch/Flop Hold Time



(a)

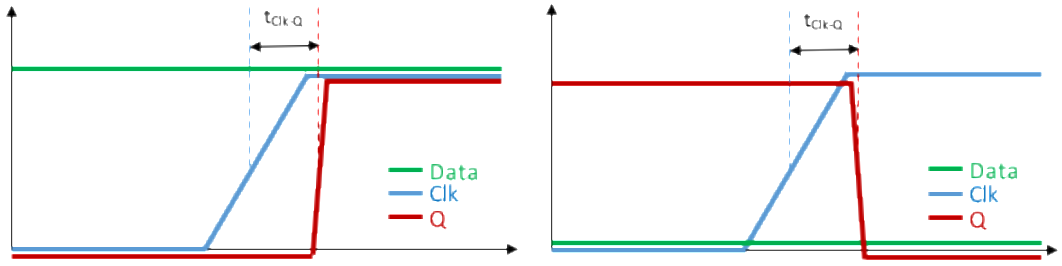


(b)



(c)

- t_{pcq} & t_{ccq} of D flip-flop:
  - Rise與fall狀態量到時間比較長的當t_{pcq}，短的當t_{ccq}



- t_{setup} of D flip-flop:
  - initialize $t_{D->Clk}$ = 1ns

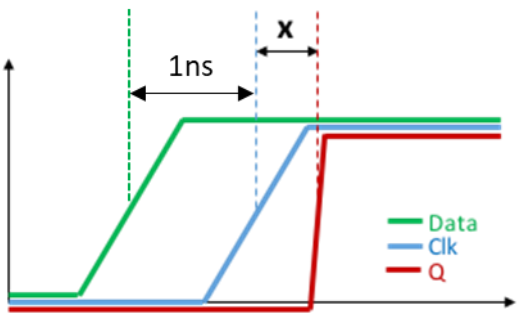


Figure. t_{setup_1x}

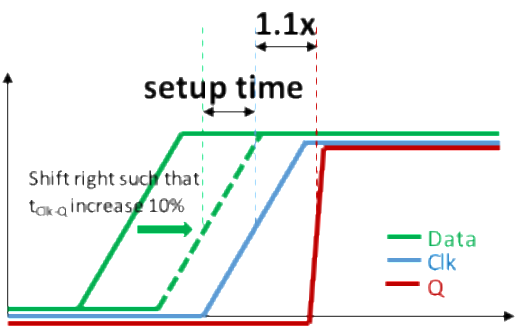


Figure. $t_{setup\_1.1x}$