VLSI Lab5

I. Design a 4-bit Shift Register

Figure 1 is a 4-bit shift register. You can use your 1-bit D flip flop in Lab3 to realize the circuit. Make sure inputs and outputs are added buffers as loading.

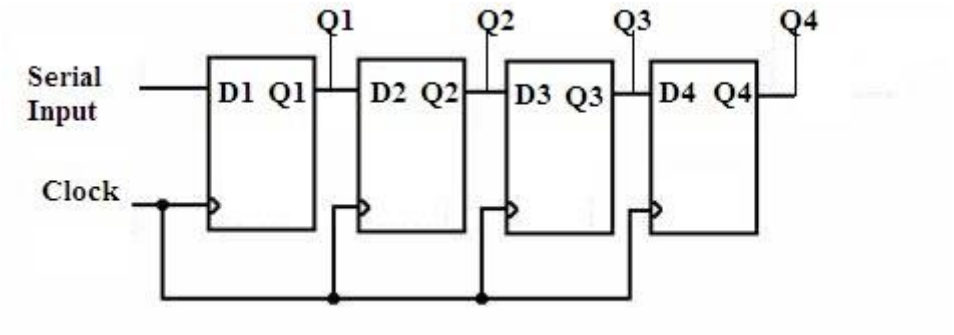

Figure 1. 4-bit Shift Register

II. Design a 4-bit Shift Register Based Multiplier, using carry ripple adder and shift register.

Figure 2a is a structure of shift register based multiplier and figure 2b is reference schematic. You can simplify the circuit. Make sure inputs and outputs are added buffers as loading.

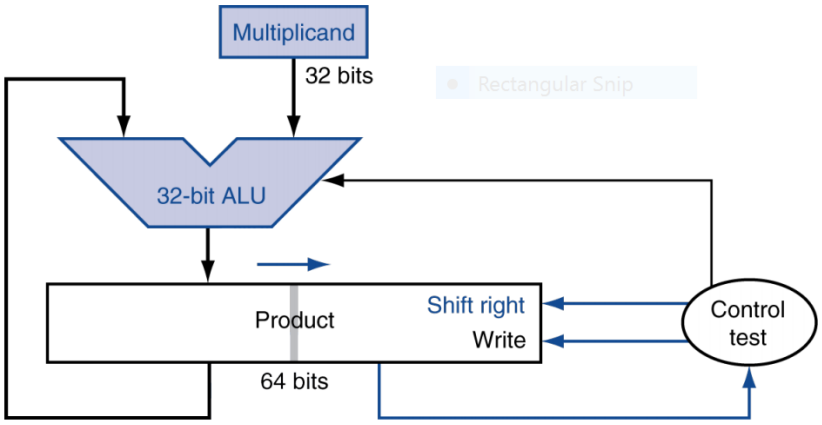

Figure 4a. Structure of shift register based multiplier

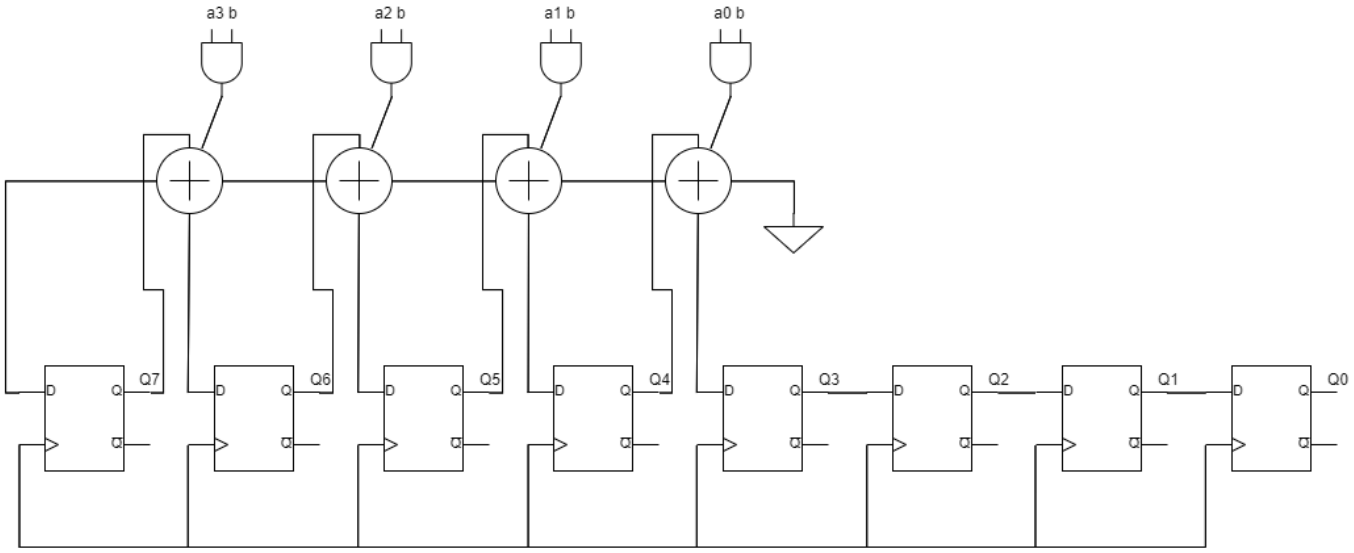

Figure 2b. 4-bit shift register based multiplier

III. Design a 4-bit Array Structure Multiplier, using carry ripple adder

Figure 3 is reference schematic. You can simplify the circuit. Make sure inputs and outputs are added buffers as loading.

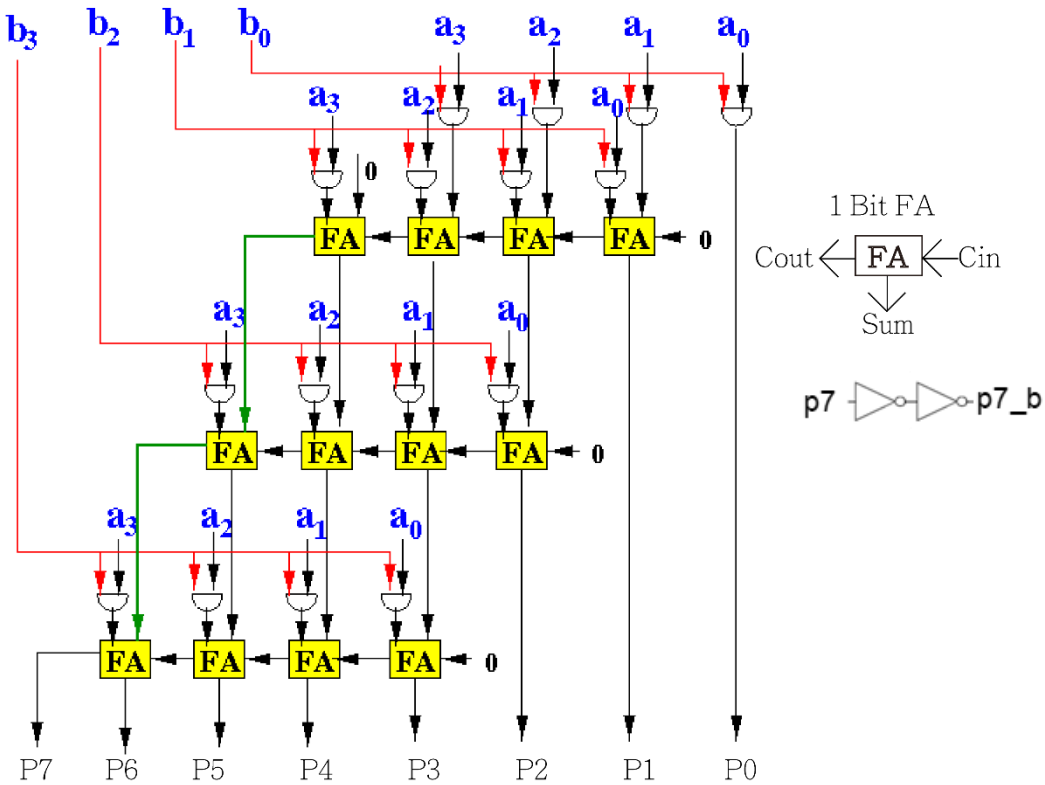

Figure 3. 4-bit array structure multiplier

IV. Design a 4-bit Wallace Tree Multiplier

Figure 4a is a structure of Wallace tree and figure 4b is the reference schematic. You can simplify the circuit. Make sure inputs and outputs are added buffers as loading.

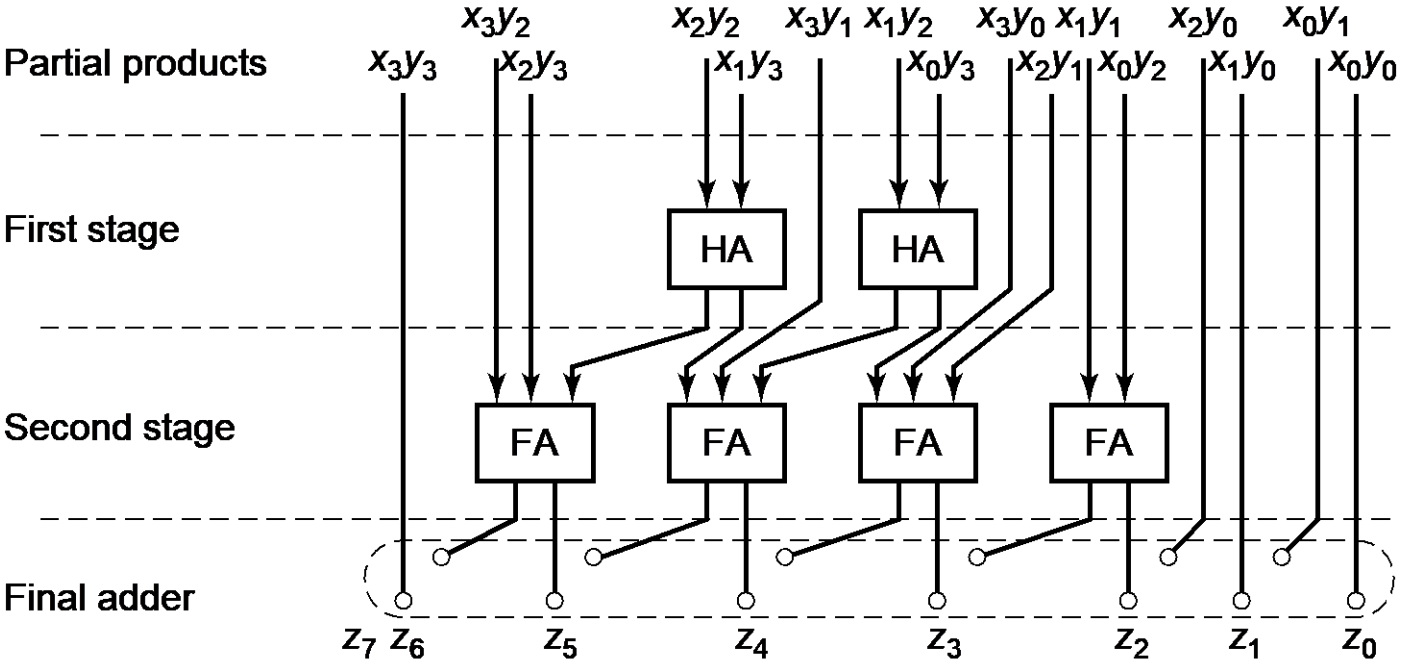

Figure 4a. Structure of Wallace tree

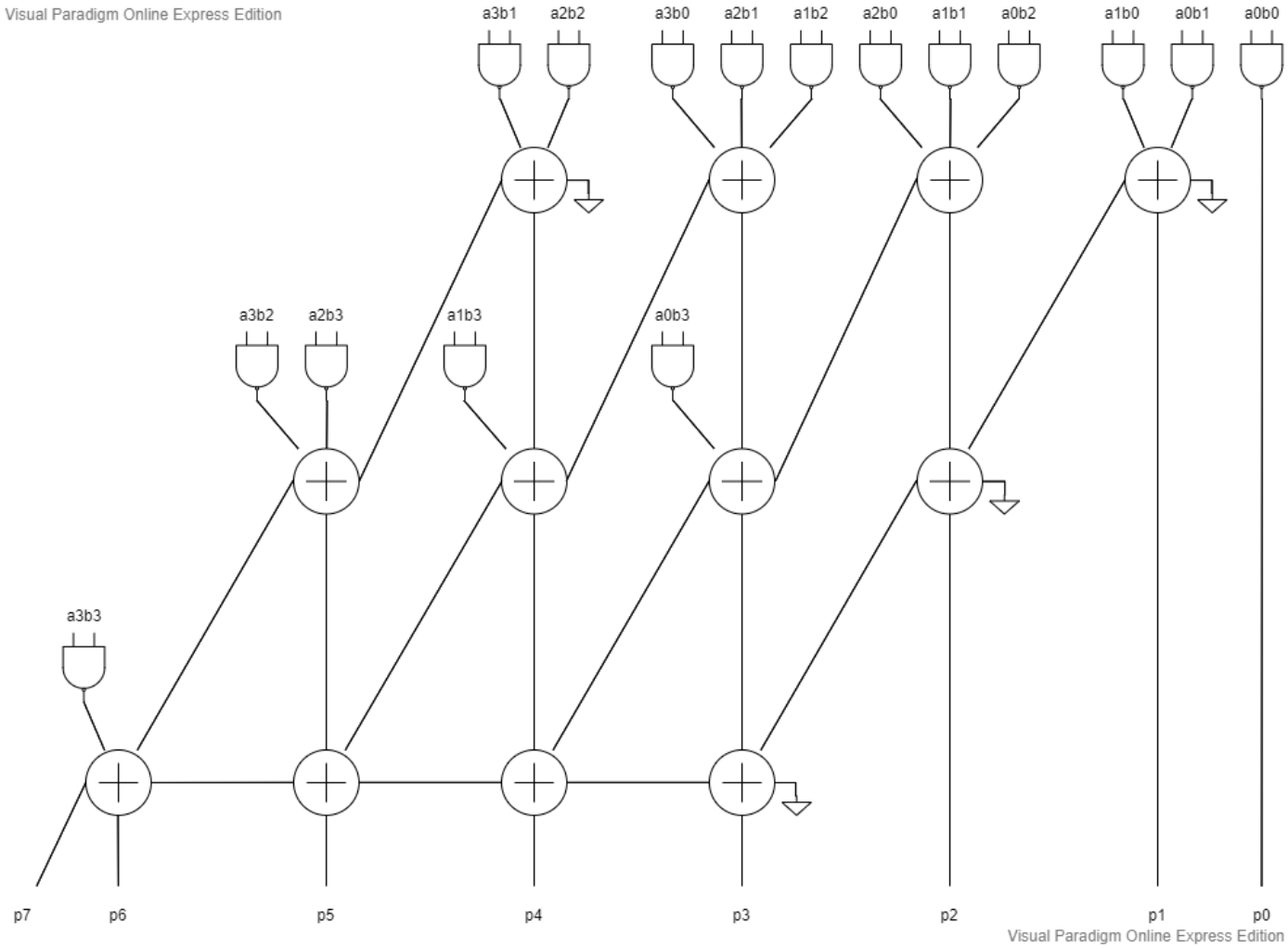

Figure 4b. 4-bit Wallace Tree Multiplier

V. Questions of this lab

Compare three types of multiplier you designed, show their advantages and disadvantages.

VI. Grading Policy

- The minimum size of NMOS is W/L = 0.47um / 0.18um, you can decide the transistor size of your design.
- Metal 3 ~ Metal 6 are forbidden to use in this lab

A. **4-bit Shift Register: 10%**

1. Pre-sim waveform: 2%
2. DRC & LVS: 4%
3. Post-sim waveform: 2%
4. Performance: 2%

$$Figure\ of\ Merit\ (FoM) = t_{delay,clk \to Q4} \times Area$$

B. **4-bit Shift Register Based Multiplier: 25%**

1. Pre-sim waveform: 5%
2. DRC & LVS: 10%
3. Post-sim waveform: 5%
4. Performance: 5%

$$Figure\ of\ Merit\ (FoM) = t_{delay,a3 \to Q7} \times Area$$

C. **4-bit Array Structure Multiplier: 25%**

1. Pre-sim waveform: 5%
2. DRC & LVS: 10%
3. Post-sim waveform: 5%
4. Performance: 5%

$$Figure\ of\ Merit\ (FoM) = t_{delay,a3 \to P7} \times Area$$

D. **4-bit Wallace Tree Multiplier: 25%**

1. Pre-sim waveform: 5%
2. DRC & LVS: 10%
3. Post-sim waveform: 5%
4. Performance: 5%

$$Figure\ of\ Merit\ (FoM) = t_{delay,a3 \to P7} \times Area$$

E. **Report: 15%**

1. **Shift register: 3%**
   - Layout screenshot with ruler: 1%
   - Post-sim waveform & measure delay: 2%
2. **Shift register based multiplier: 3%**
   - Layout screenshot with ruler: 1%
   - Post-sim waveform & measure delay: 2%
3. **Array structure multiplier: 3%**
   - Layout screenshot with ruler: 1%
   - Post-sim waveform & measure delay: 2%
4. **Wallace tree multiplier: 3%**

- Layout screenshot with ruler: 1%
- Post-sim waveform & measure delay: 2%

5. **Question: 3%**

VII. Demo time

1/13 (Wed.) or 1/15 (Fri.) at 15:30 ~ 18:30

You only have “one” chance to demo!

After deadline, any requests for demo are denied.

VIII. Report hand-in deadline:

1/15 (Fri.) 23:59 on New E3

After deadline, any requests for handing in report are denied.