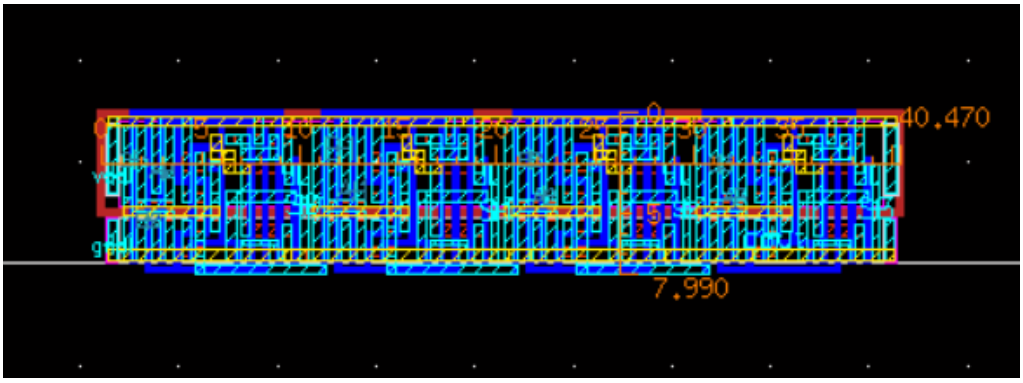
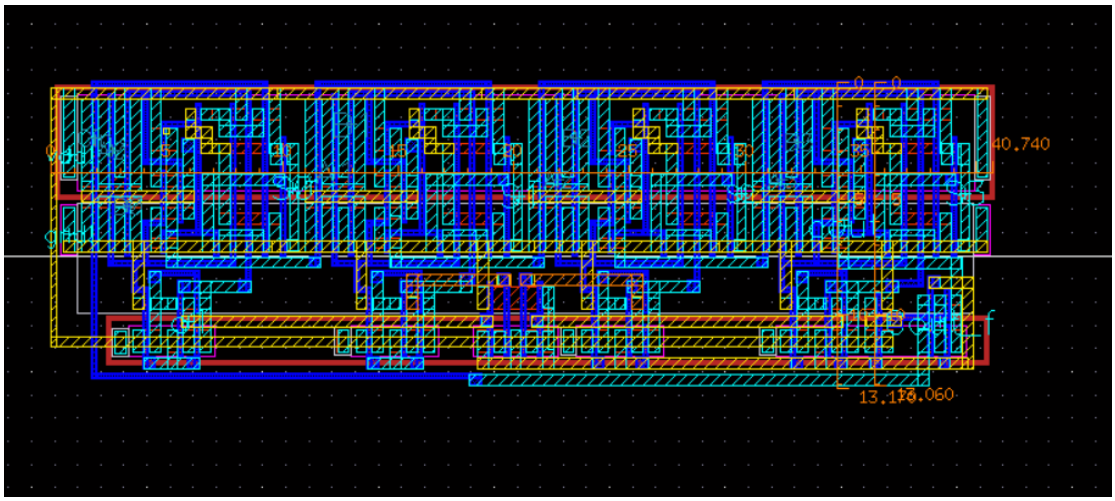
(I)Layout with ruler:

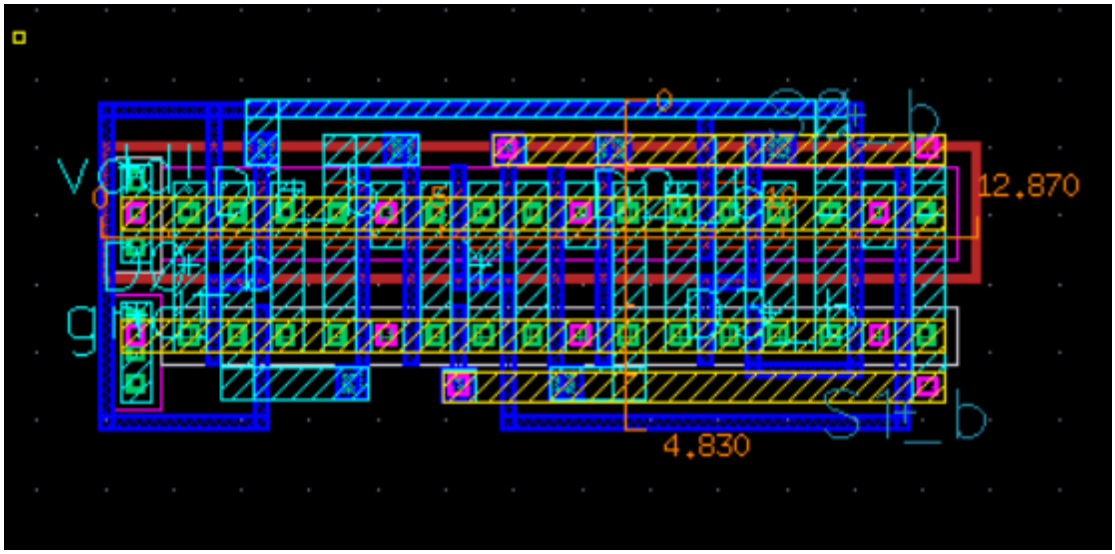
1.4-bit carry-ripple adder: 40.47*7.99=323.3553



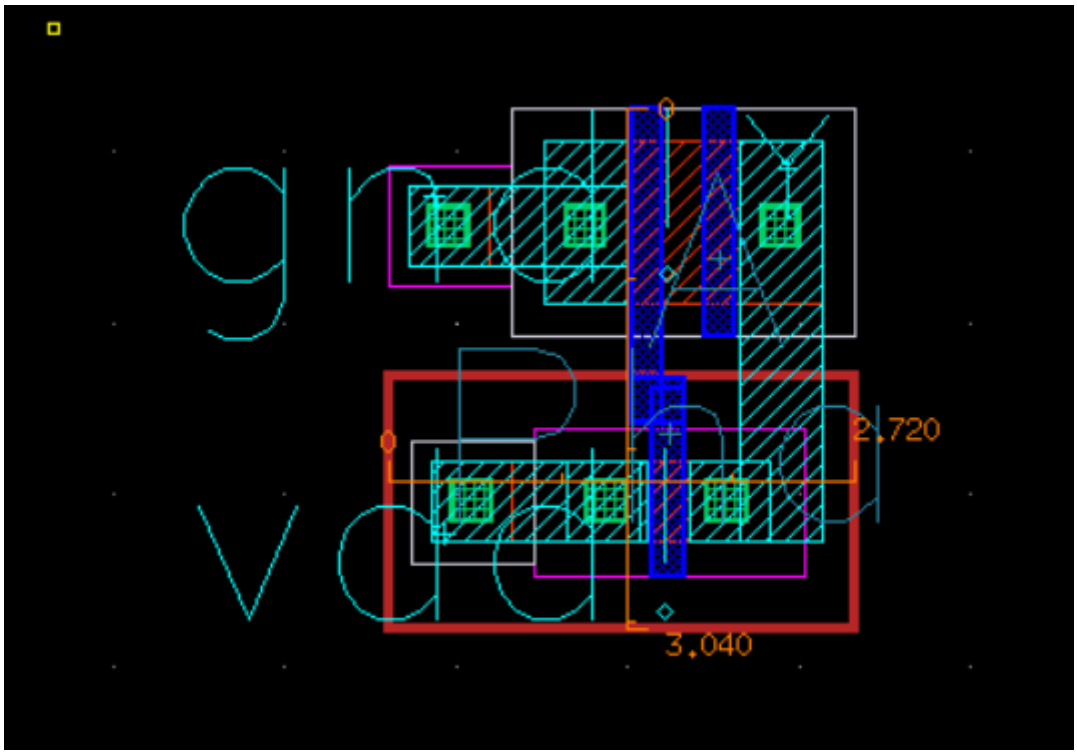

2.4-bit carry-skip adder: 40.74*13.06=532.0644




3.4:1 MUX: 12.87*4.83 = 62.1621

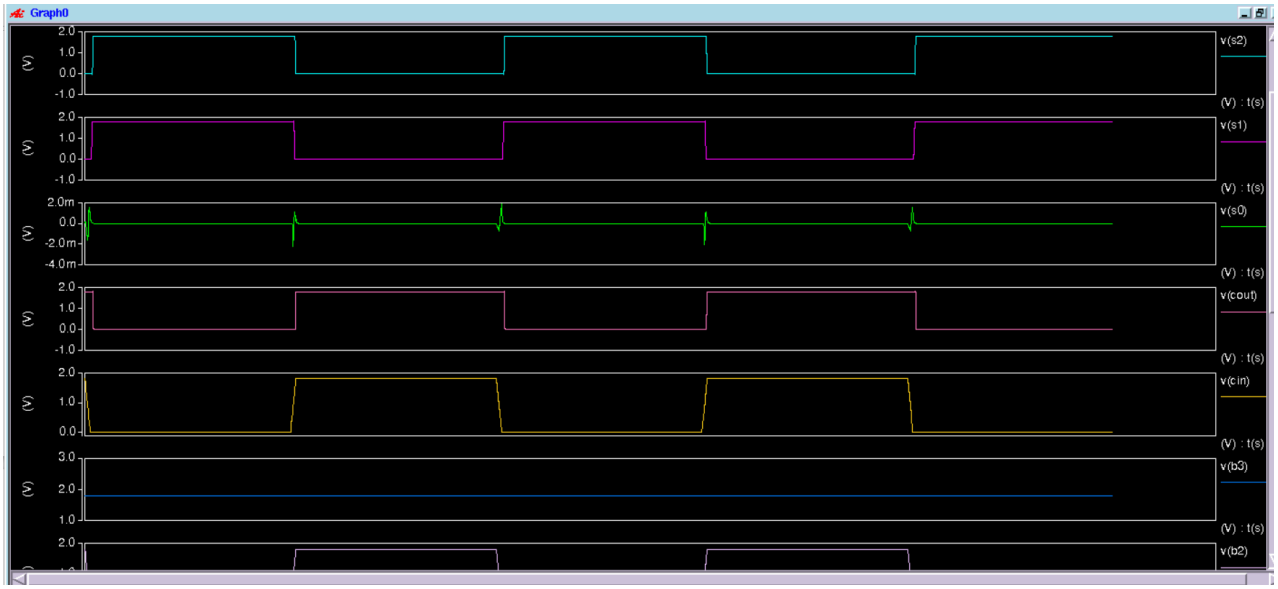


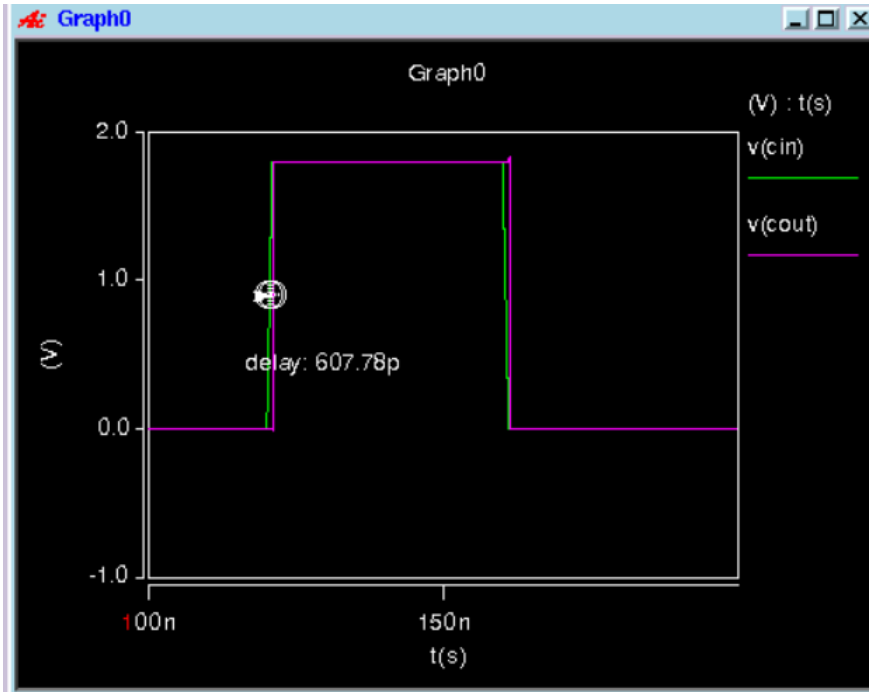
4.Dynamic inverter: 3.04*2.72 = 8.2688



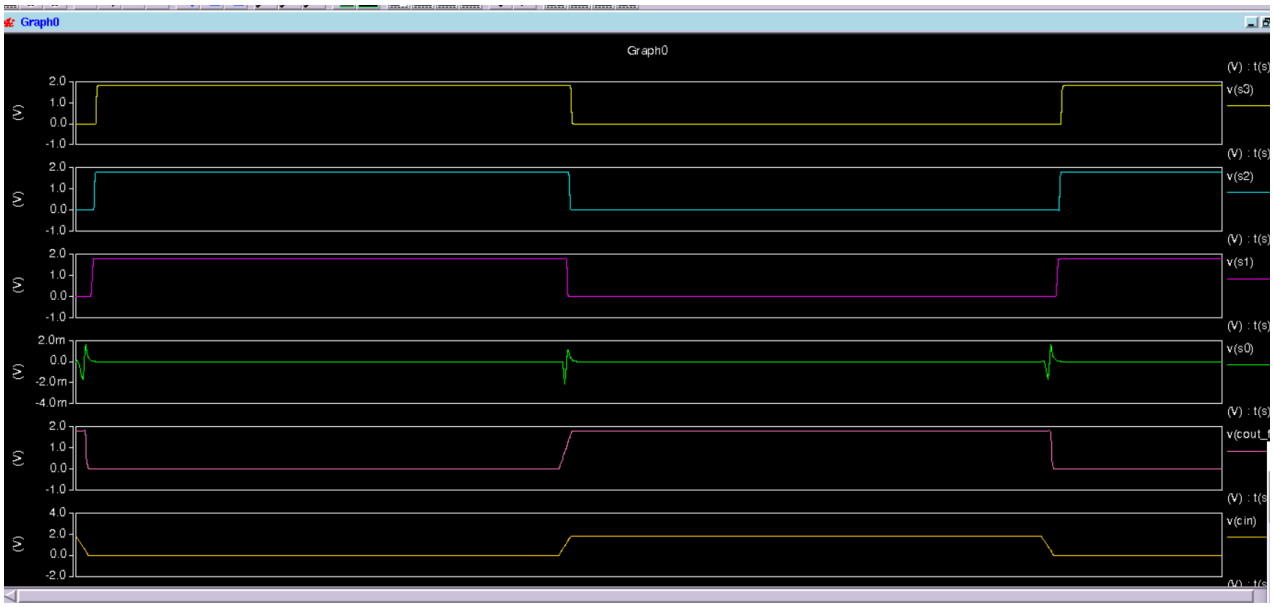

(ii)Postsim wavefrom

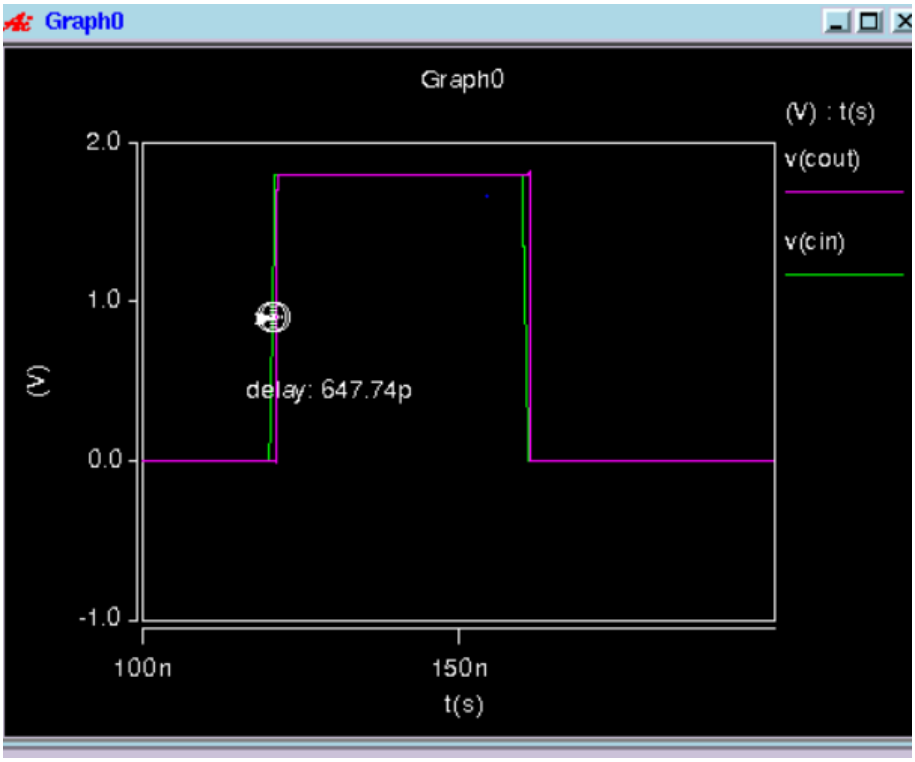
1. 4-bit carry-ripple adder(cin to cout delay:607.78p)



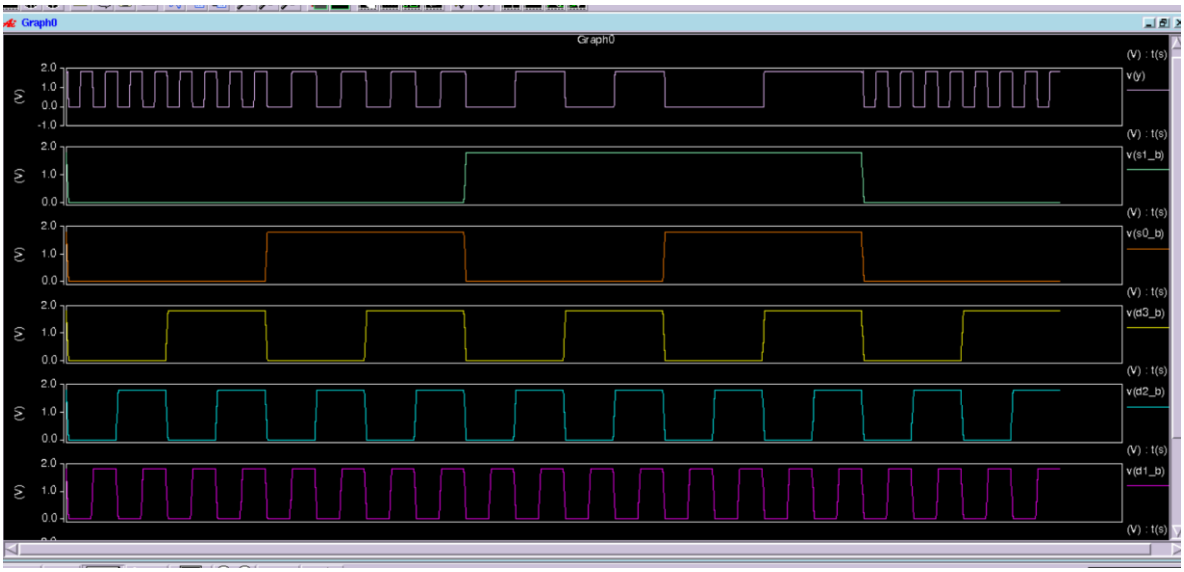


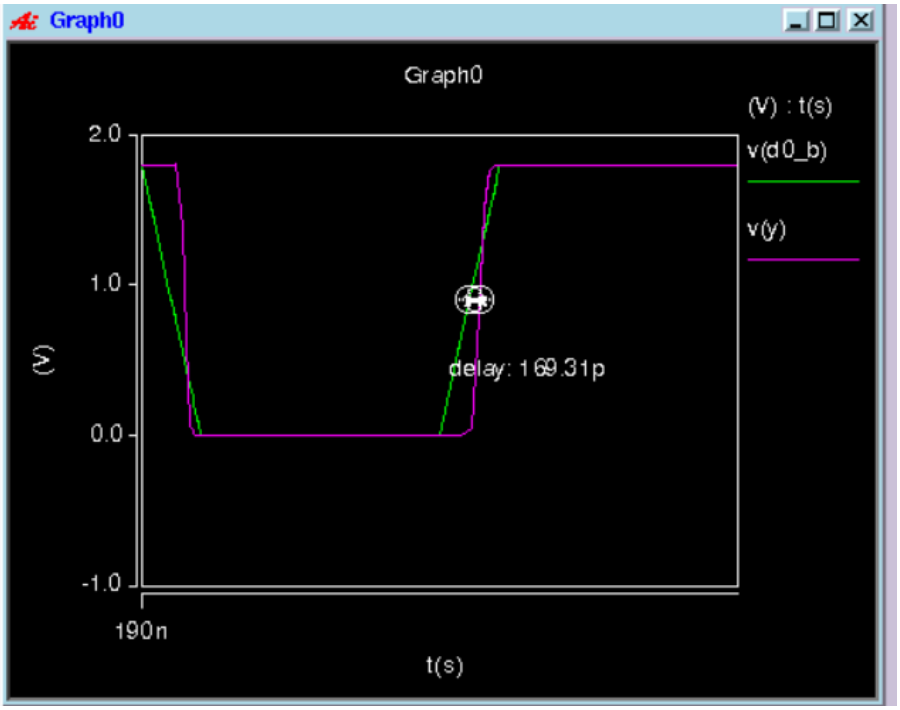

2. 4-bit carry-skip adder(cin to cout delay:647.74p)



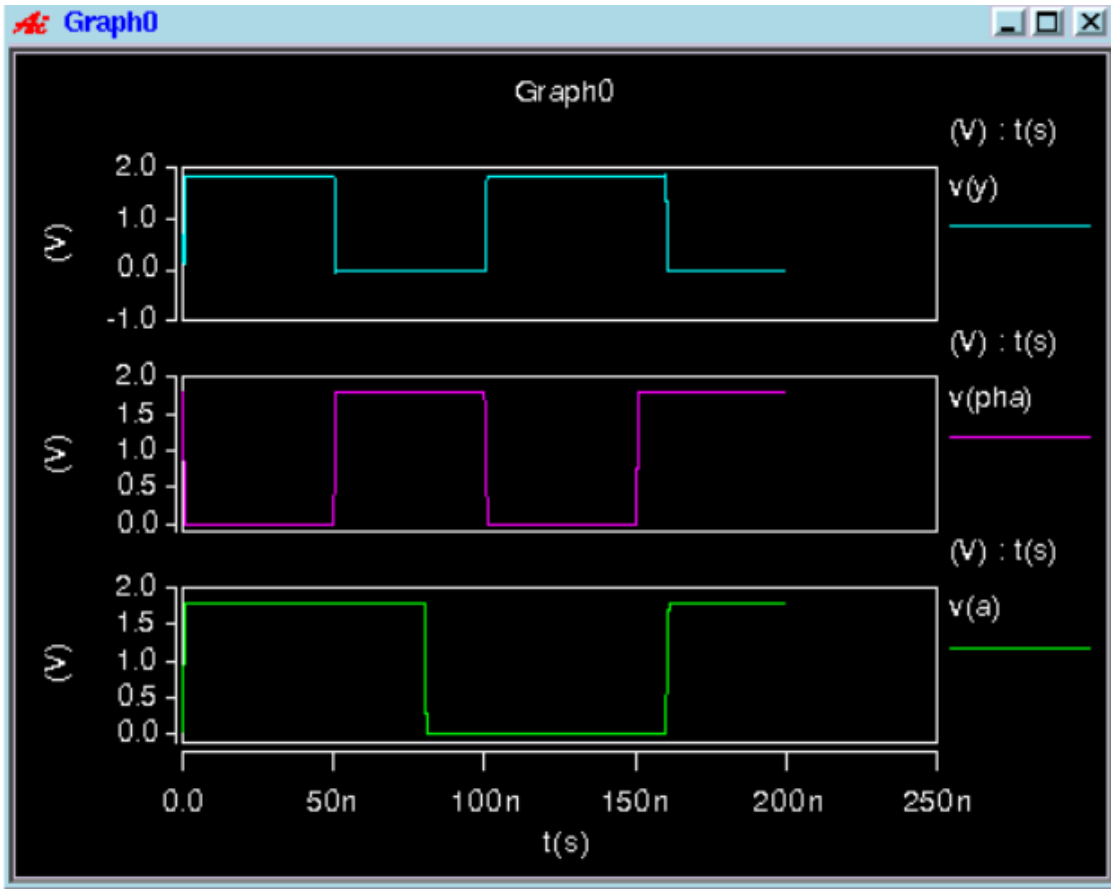


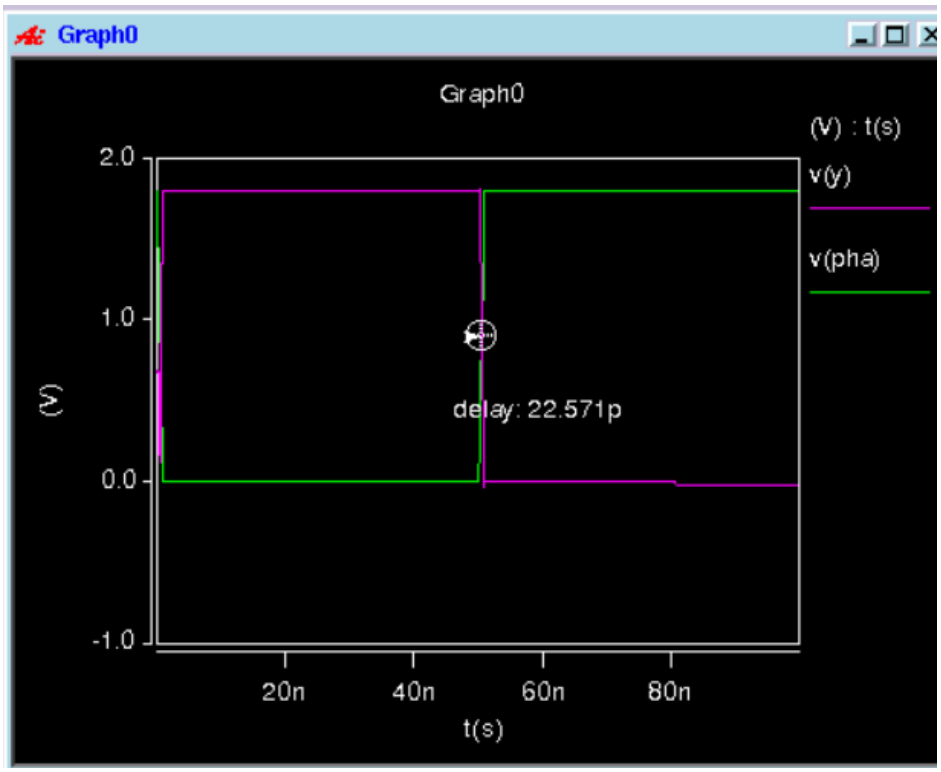

3. 4:1 MUX(DelayD0_b to Y :169.31p)






4. Dynamic inverter(DelayΦ to Y:22.571p)






(iii)Questions of the labs:

1. Compare the DelayCin To Cout between 4-bit carry-ripple adder and 4-bit carry-skip adder, and explain the reason of the difference.
   依照這次助教的測資比較，carry-ripple 較快，而使用 lab 測資則是 carry-skip 快。我覺得應該是這次只連了 4 顆 full adder，carry-skip 效果沒有很顯著，所以他們互有快慢，如果再串連更多 full adder，carry-skip 應該會較快。
2. Discuss what are the benefits using transmission gates to realize a 4:1 MUX, and explain the reasons.
   transmission gates 最大的好處是可以減少 layout 的面積，相較於其他畫法使用較少的電晶體，而且 delay 也比較短。
3. What is “Monotonicity Problem” and how can we resolve this problem?
   這個現象發生在 dynamic gate。如果在 pha 在 evaluate 的狀況下更動 inputA 的值(由 1->0)，output Y 理論上要馬上跟著更動，但是他沒有（如上面 dynamic inverter 圖示），而是到下一次 precharge 才改變值由 0->1，這個現象稱為 Monotonicity Problem。
   To resolve the problem:we should follow dynamic stage with inverting static gate. The invering static gate can help recharging the next dynamic stage During evaluation period.