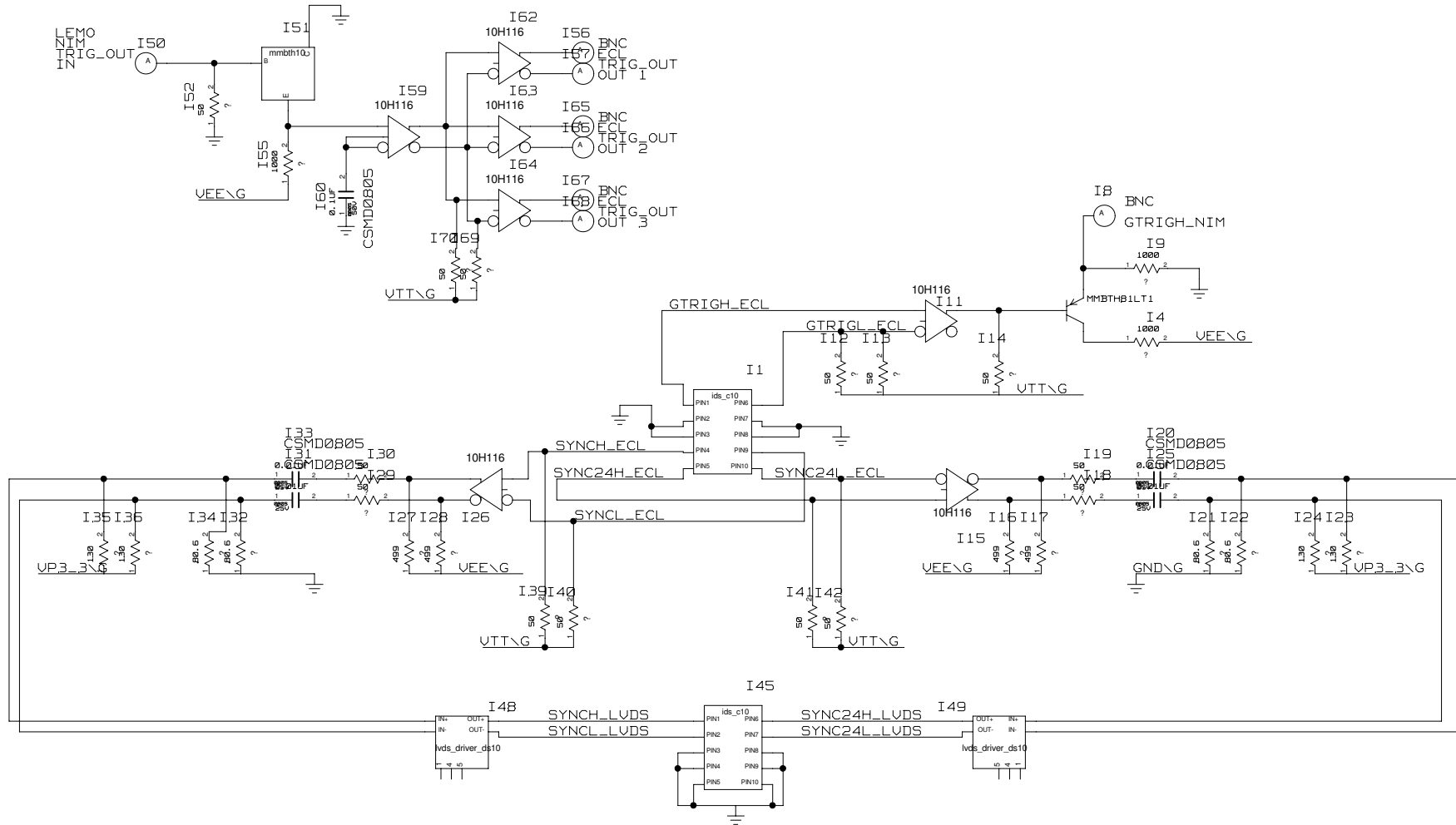

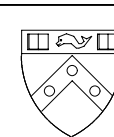
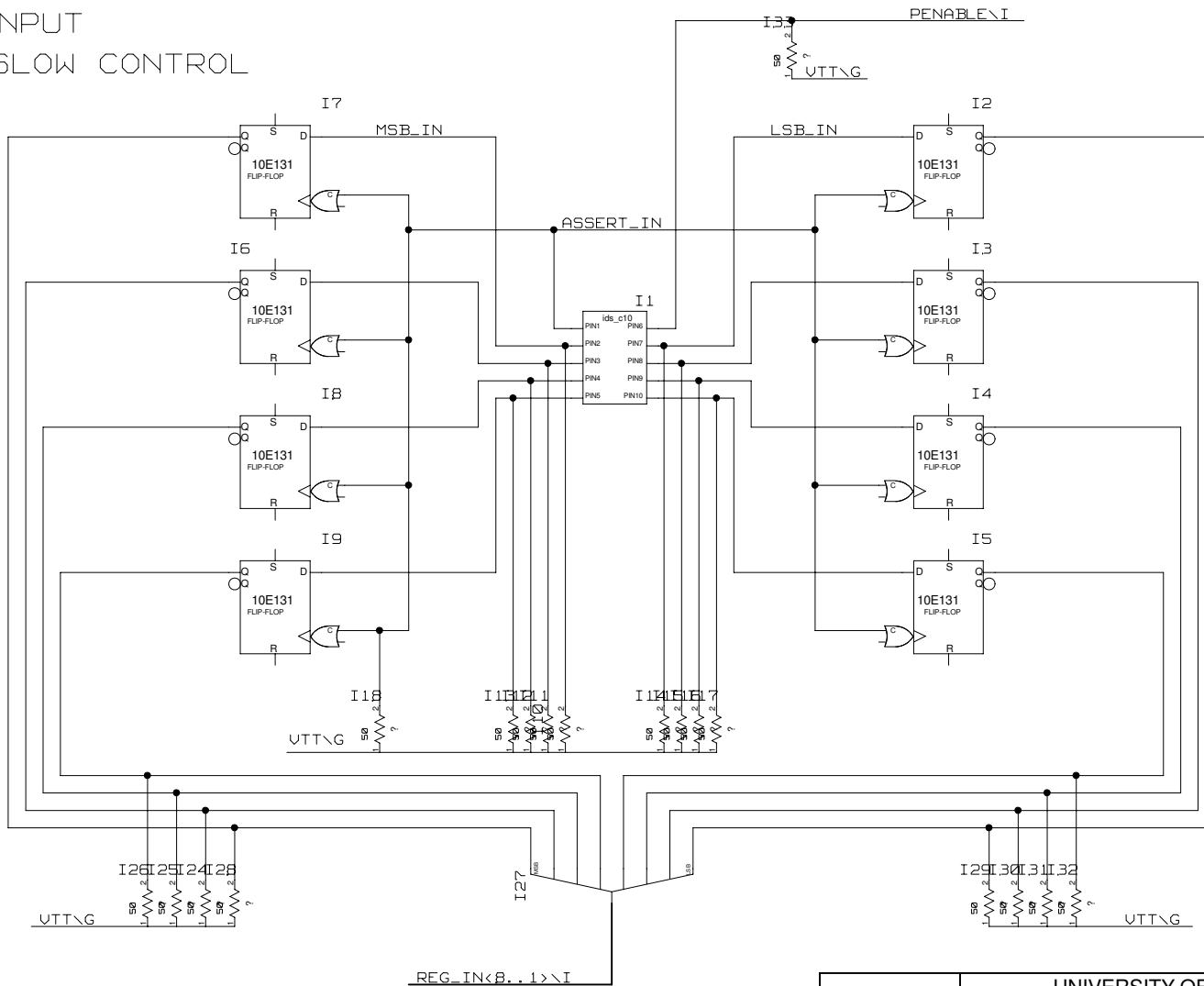


CAEN CONVERSATIONS



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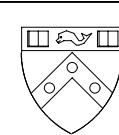
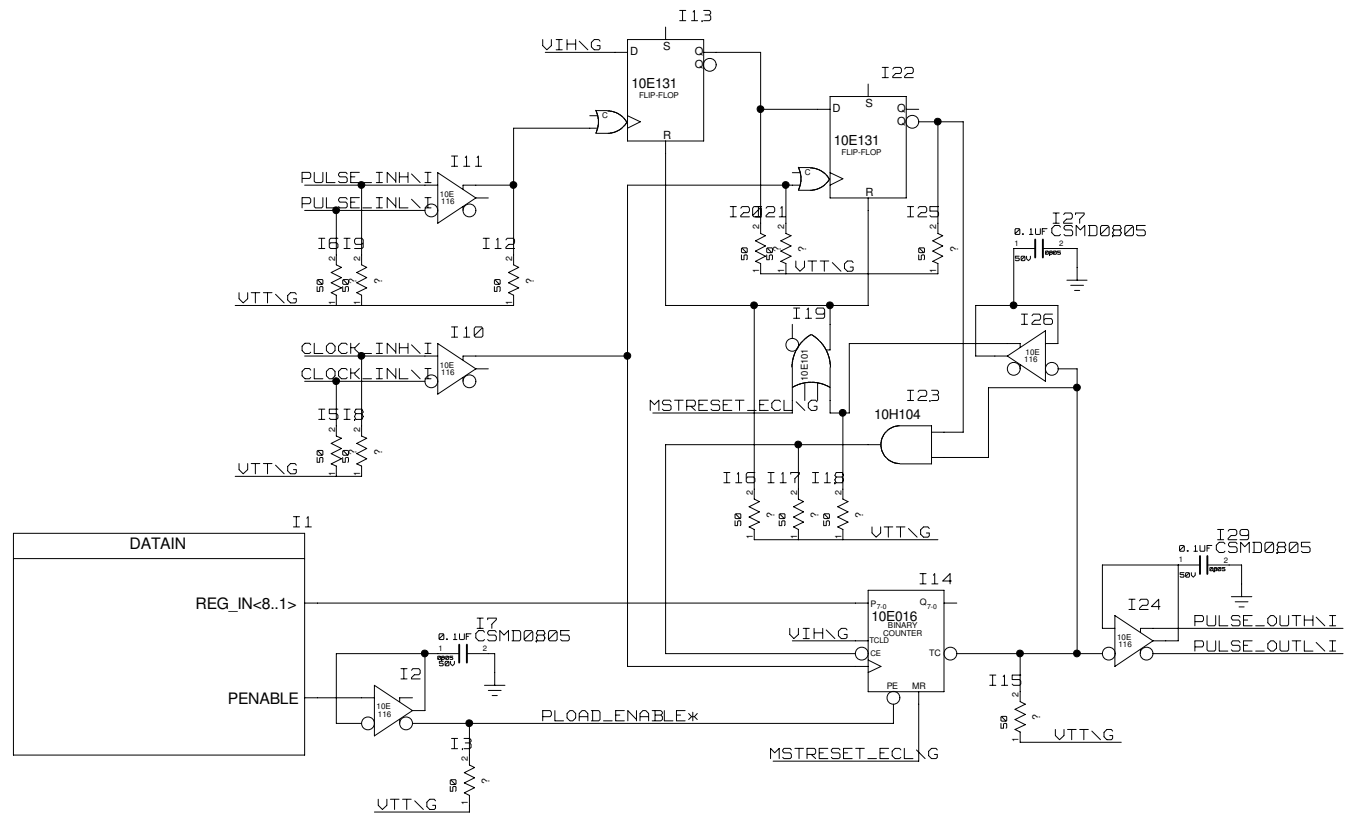
DATA INPUT
FROM EG SLOW CONTROL



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HIGH ENERGY PHYSICS

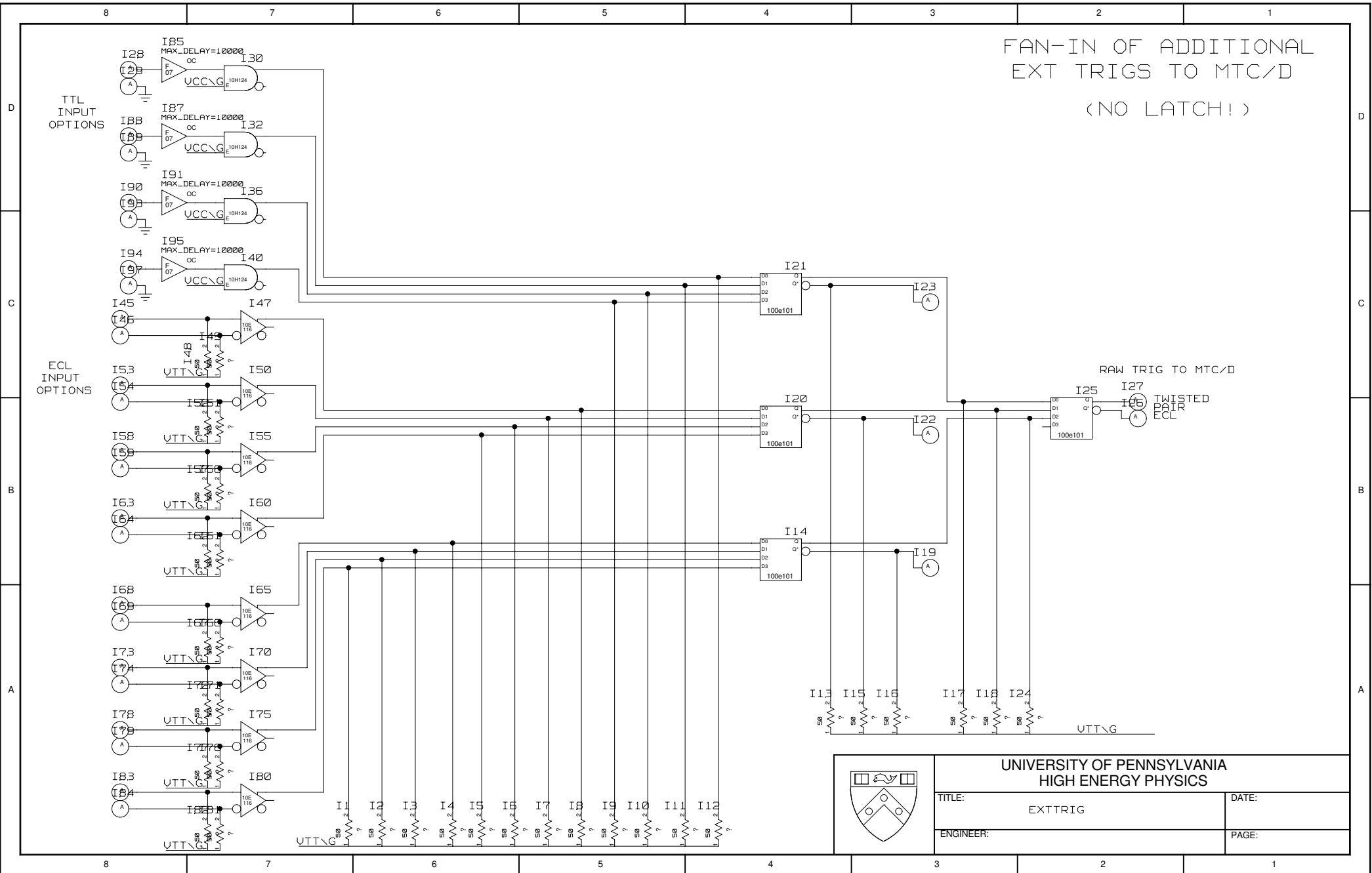
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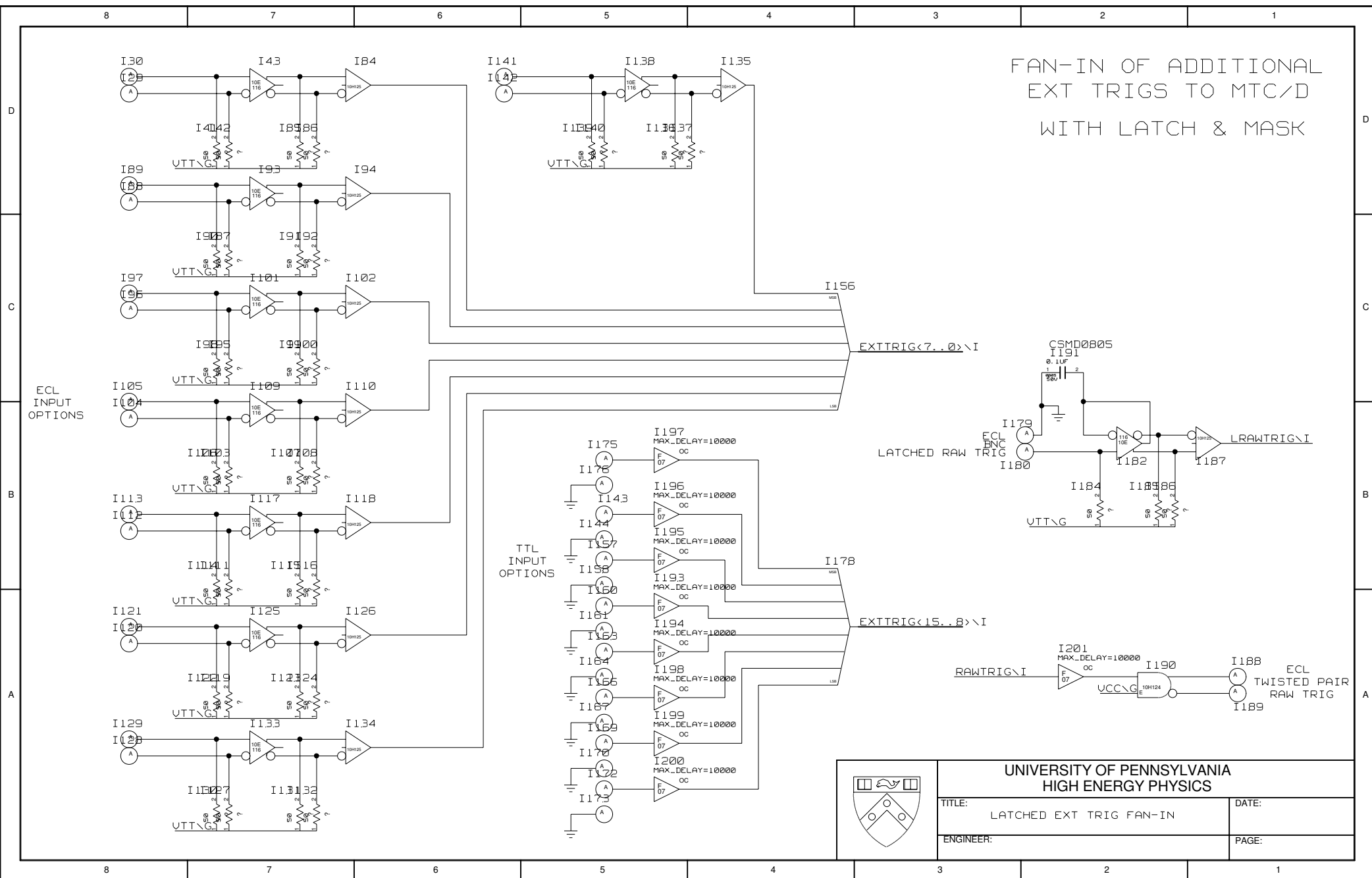
GENERIC PROGRAMMABLE DELAY

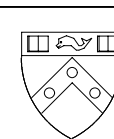
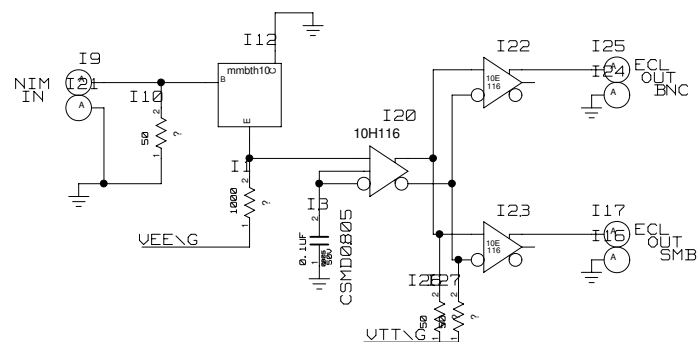


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TITLE:	PROGDELAY	DATE:
ENGINEER:		PAGE:

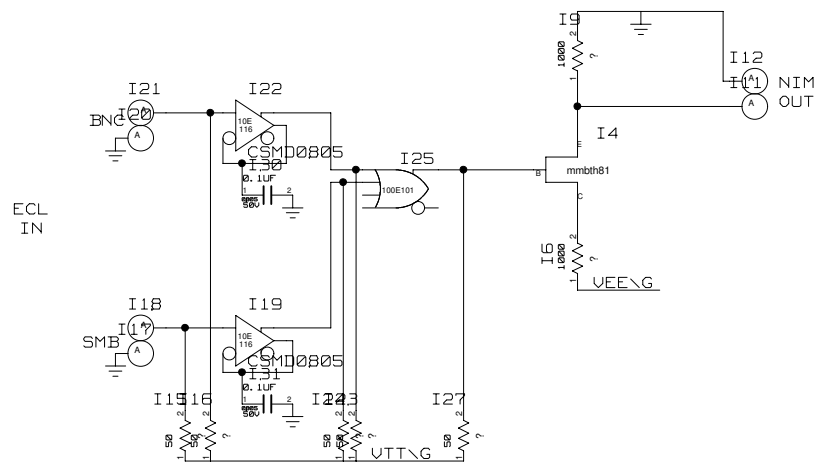


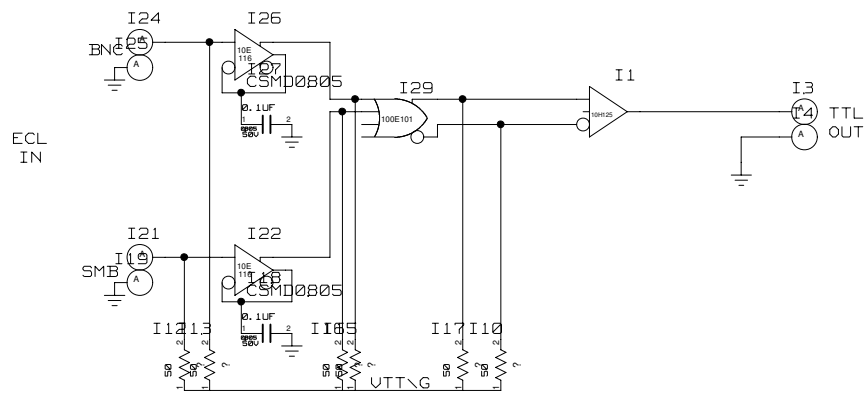





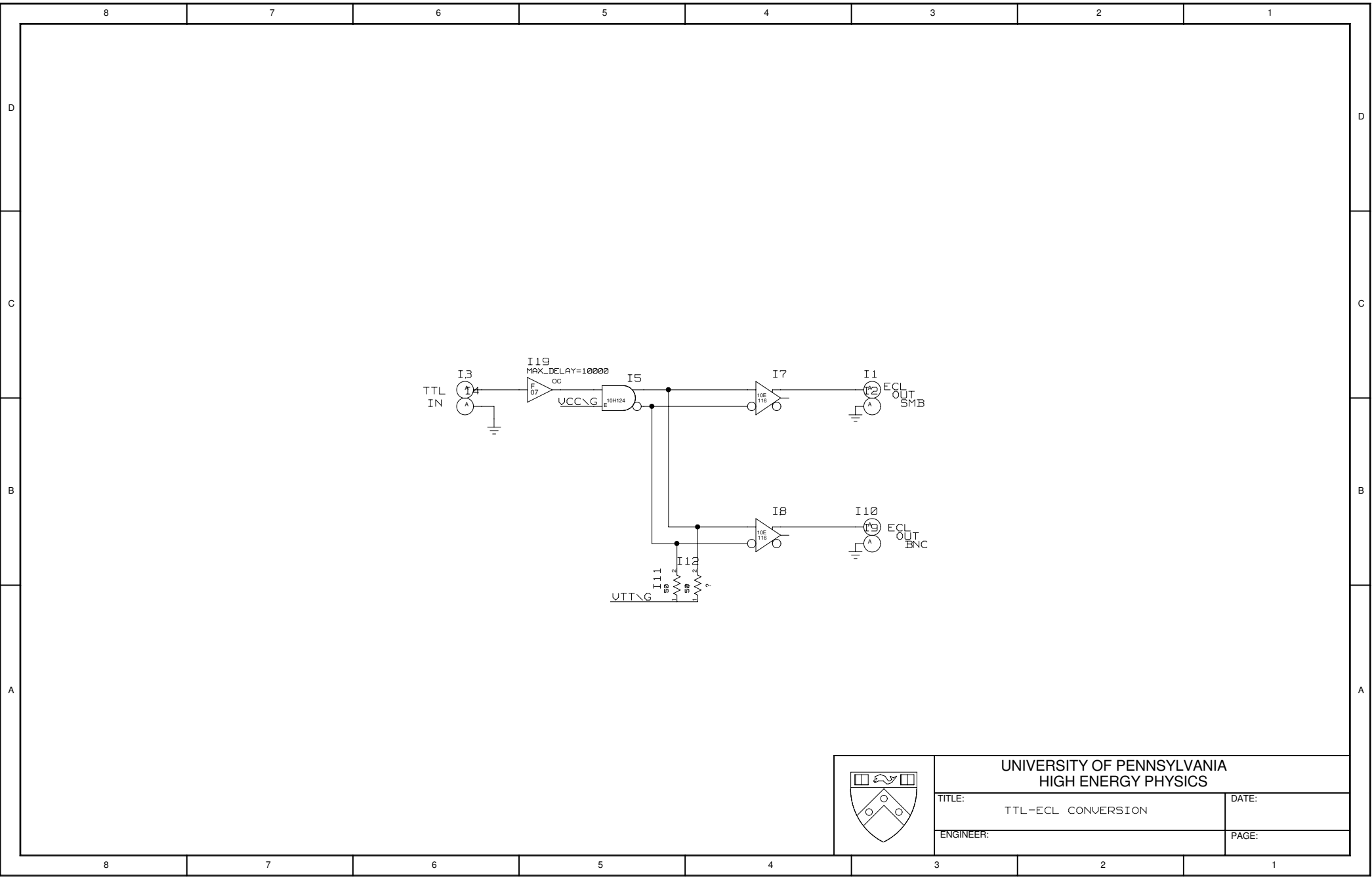
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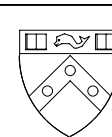
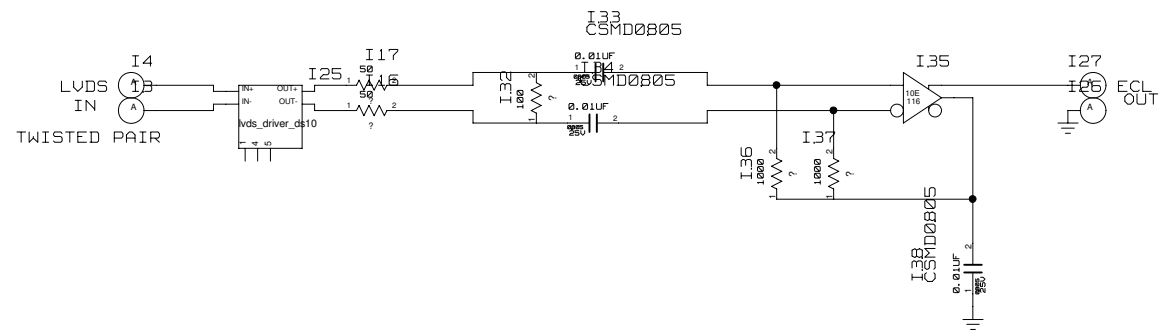
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ENGINEER:		PAGE:





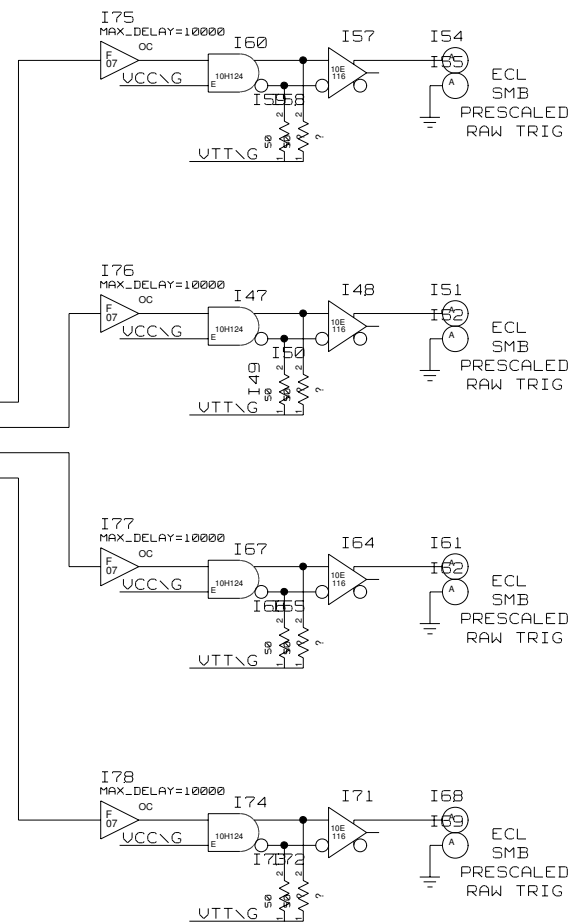
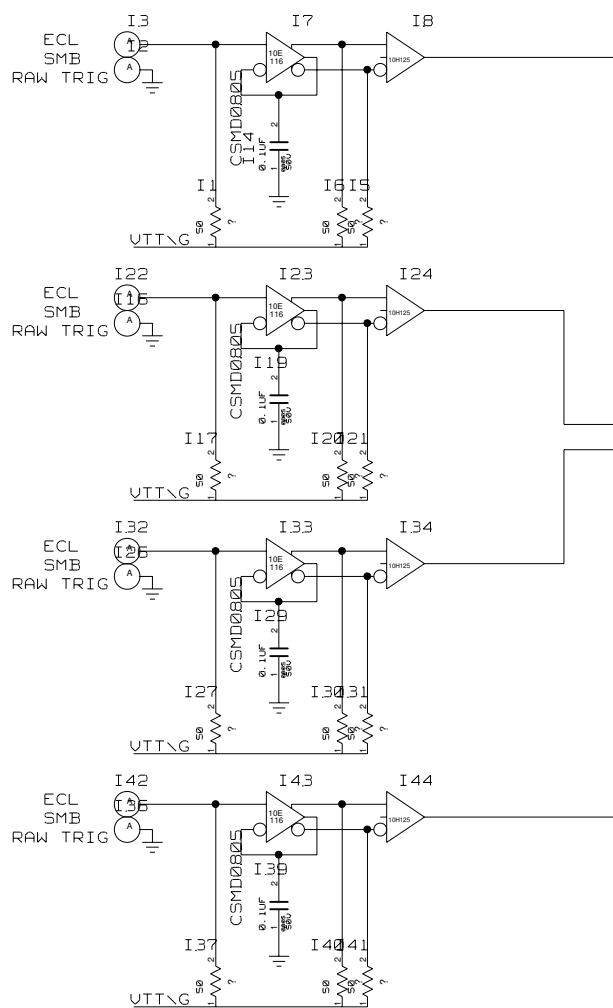
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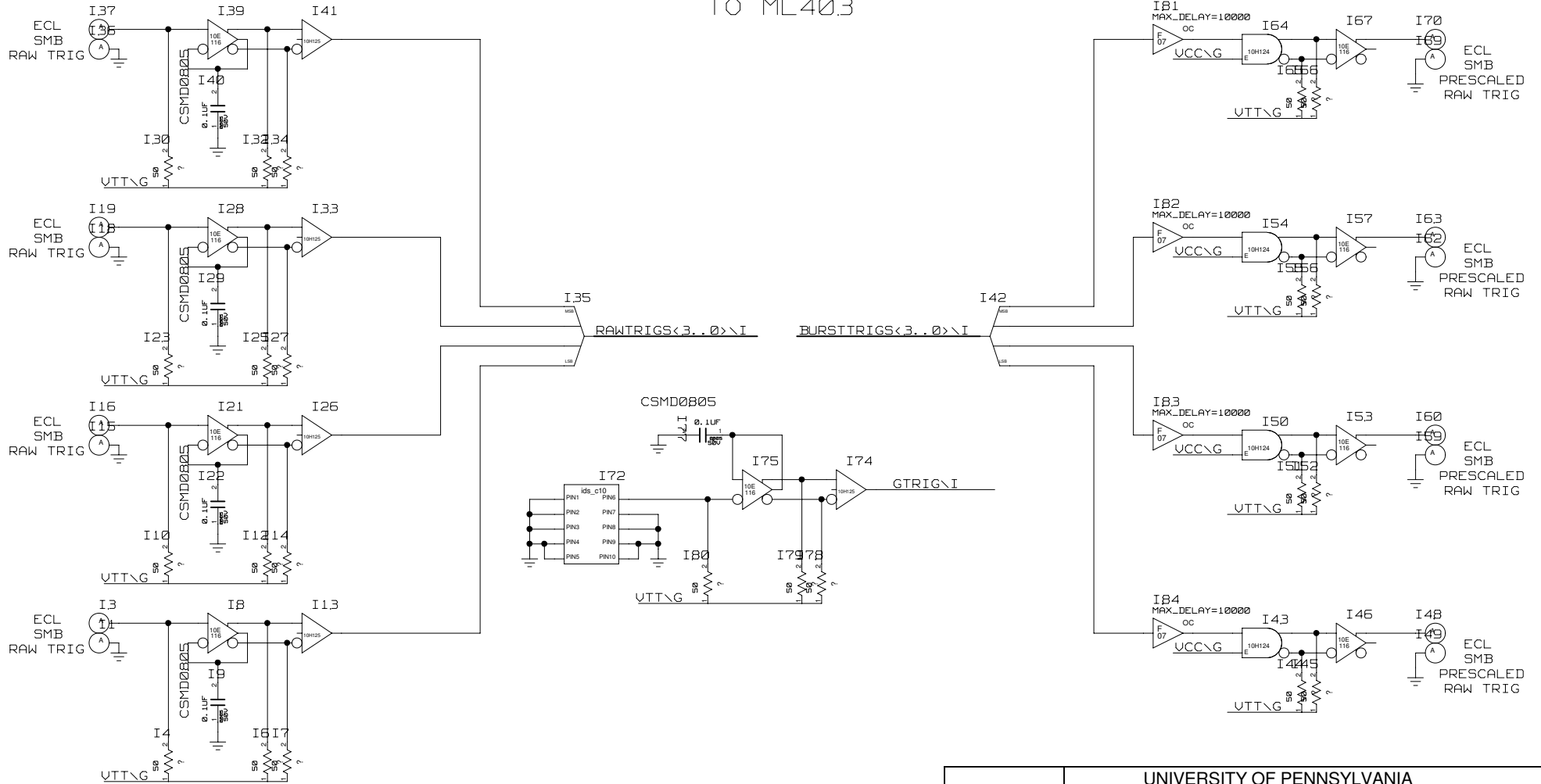


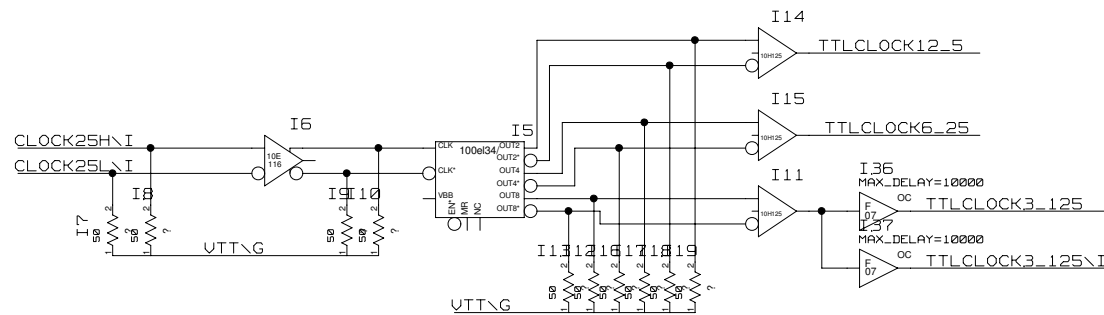
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ENGINEER:	PAGE:



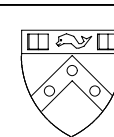
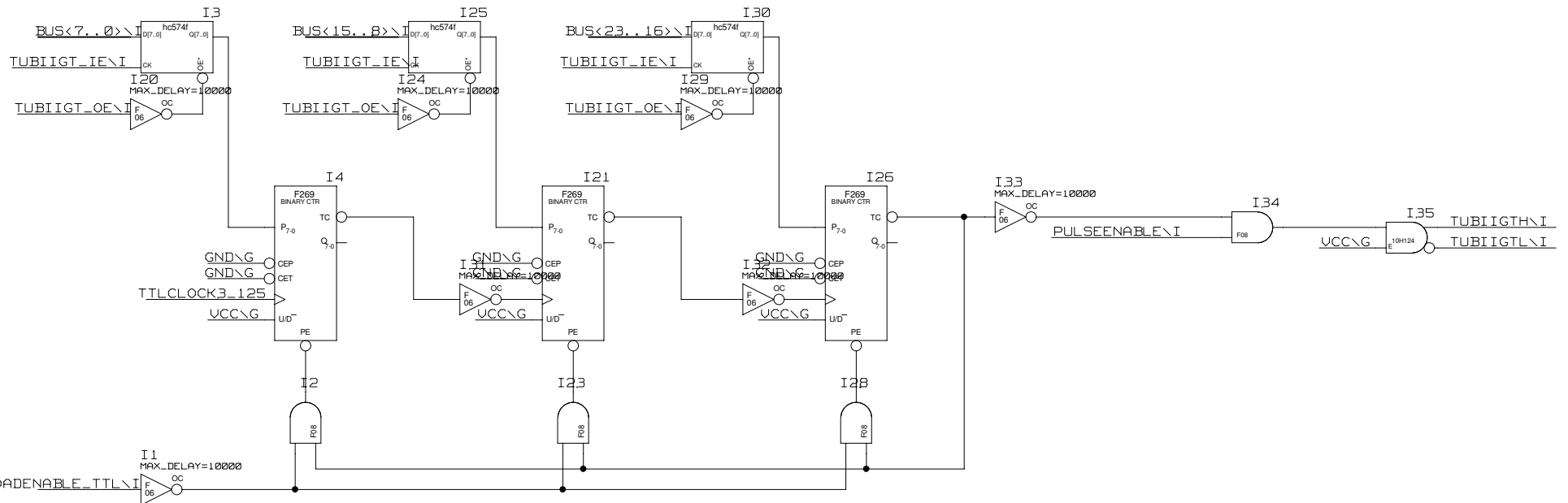
BURST TRIGGER: INPUTS AND OUTPUTS TO ML403





GENERIC TUBII PULSE GENERATION

3.125MHZ - 0.2HZ



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HIGH ENERGY PHYSICS

TITLE:	TUBII GT	DATE:
ENGINEER:		PAGE:

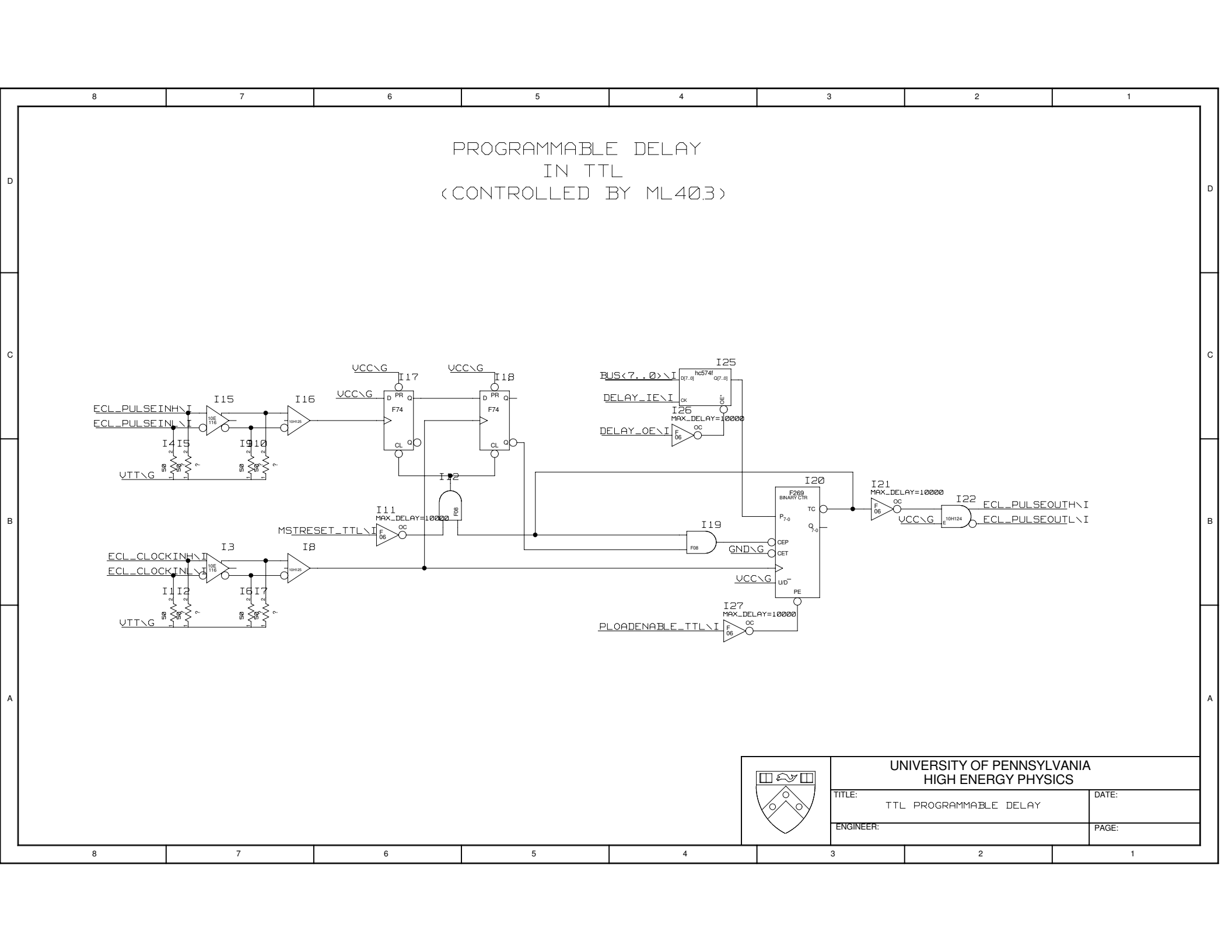
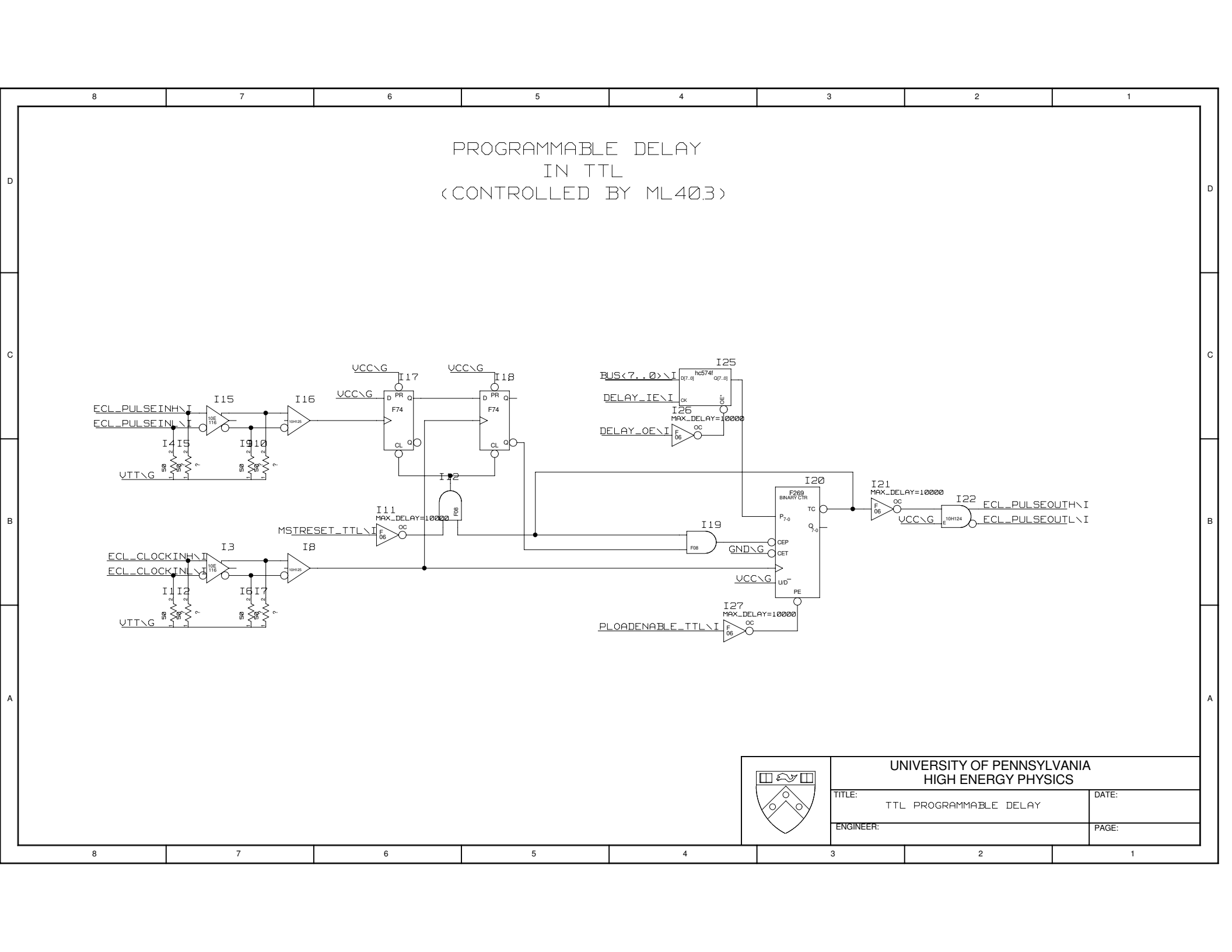
PROGRAMMABLE DELAY
IN TTL
(CONTROLLED BY ML403)

The circuit diagram illustrates a programmable delay in TTL, controlled by the ML403. The circuit is composed of several integrated circuits (ICs) and passive components:

- ICs:**
 - I15, I16:** 74F04 inverters.
 - I17, I18:** 74F74 D-type flip-flops.
 - I11, I19:** 74F08 3-input AND gates.
 - I12, I22:** 74F00 NAND gates.
 - I21, I27:** 74F06 monostable multivibrators.
 - I20:** 74F269 binary counter.
 - I25:** ML403 bus interface.
- Inputs:**
 - ECL_PULSEINH, ECL_PULSEIN:** Input signals for pulse generation.
 - ECL_CLOCKIN, ECL_CLOCKIN:** Input signals for clock generation.
 - PLOADENABLE_TTL:** Input signal for load enable.
- Outputs:**
 - ECL_PULSEOUTH, ECL_PULSEOUTL:** Output signals for pulse generation.
- Power and Grounding:**
 - VTT, VCC:** Power supply connections.
 - GND:** Ground connections.
- Control and Timing:**
 - The circuit uses a combination of inverters, flip-flops, AND gates, NAND gates, and monostable multivibrators to generate a programmable delay.
 - The delay is controlled by the ML403 bus (I25) and the 74F06 monostable multivibrators (I21, I27).

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HIGH ENERGY PHYSICS

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- Outputs:**
 - ECL_PULSEOUTL:** Output signal for the programmable delay.
- Power and Grounding:**
 - VTT:** Power supply for the ECL logic.
 - VCC:** Power supply for the TTL logic.
 - GND:** Ground connection.
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 - The delay is programmable via the ML403 bus (I25).
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IN TTL
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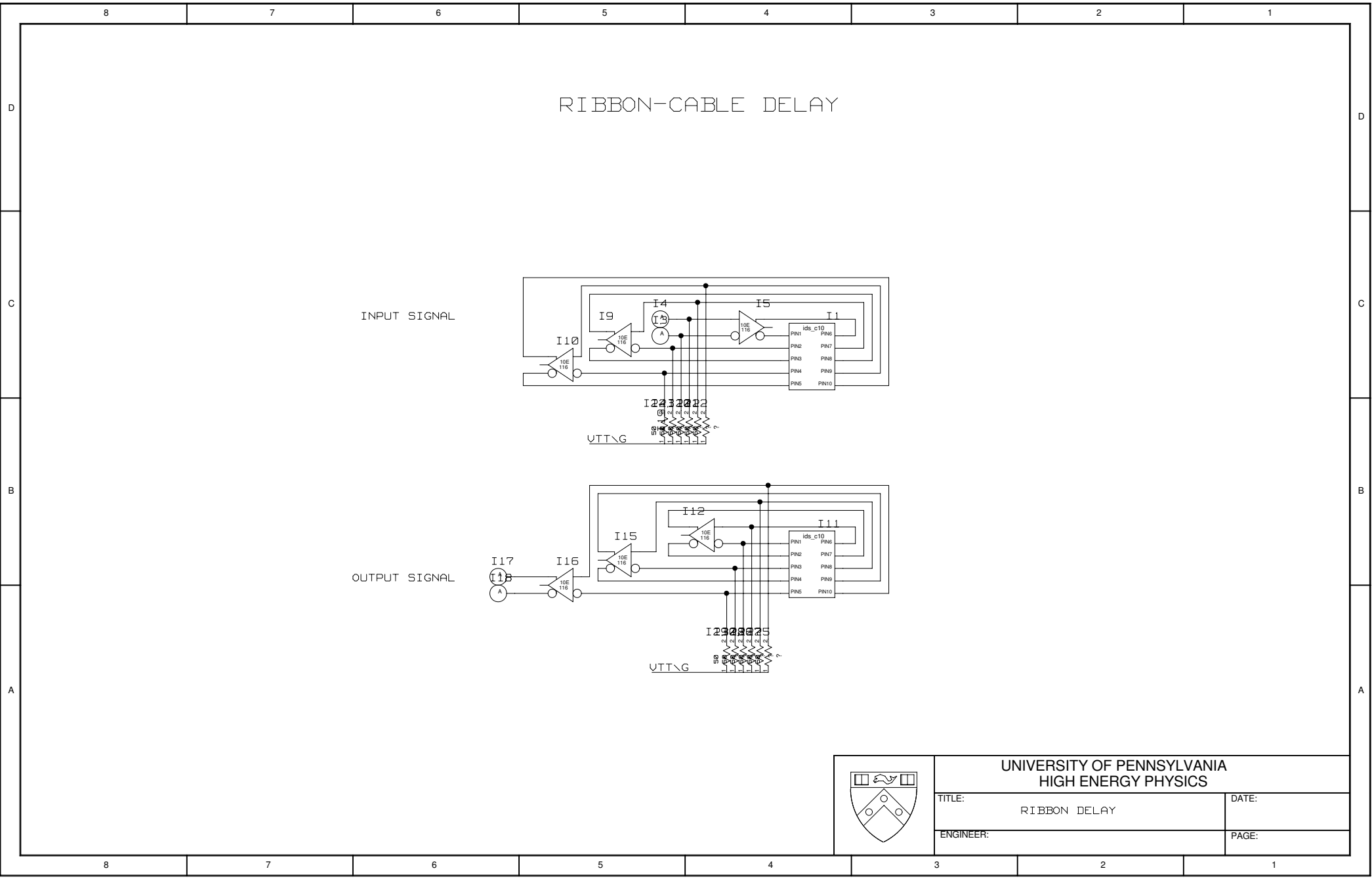
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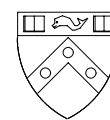
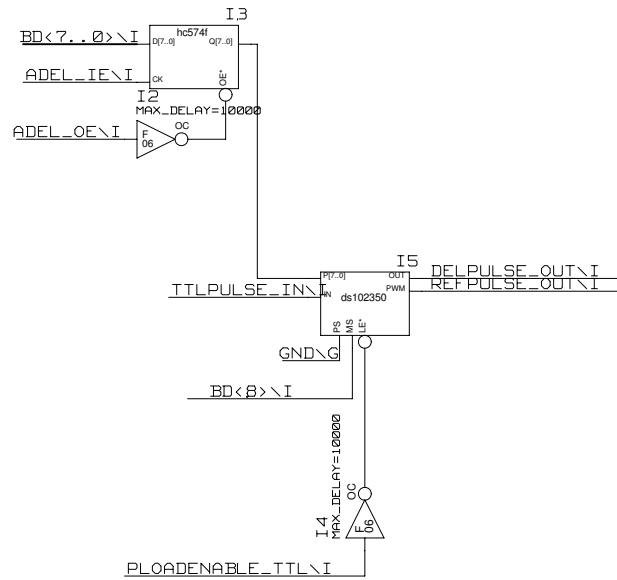
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0 - 127.5 NS DELAY
IN 0.5NS STEPS



TITLE:	DATE:
ASYNC DELAY	
ENGINEER:	PAGE:

0 - 1275 NS DELAY
IN 5.0NS STEPS

