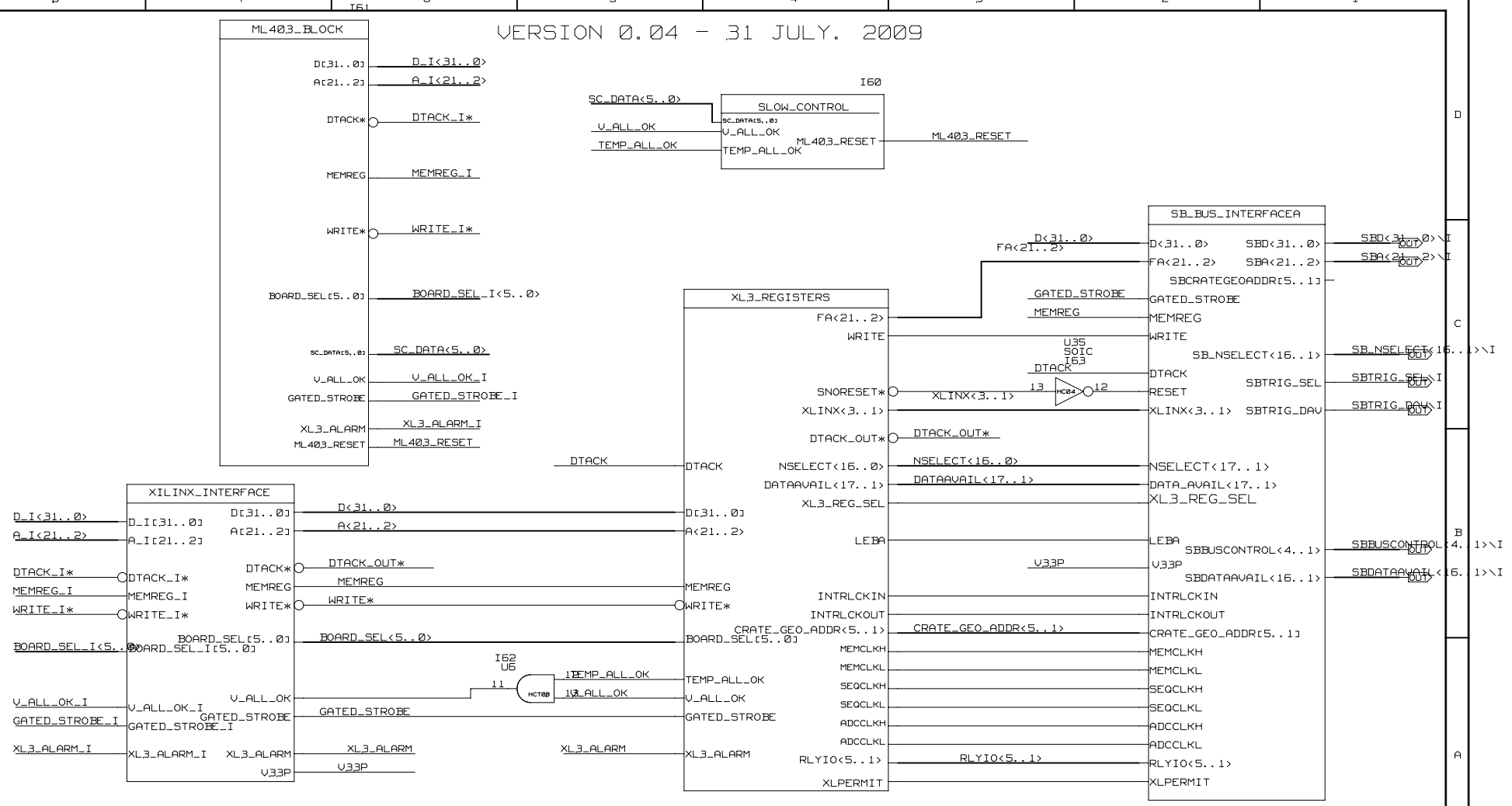
XL3 BOARD BLOCK VIEW

VERSION 0.04 - 31 JULY. 2009



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HIGH ENERGY PHYSICS

TITLE: XL3 VME EXTENDER SYSTEM	ABBREV=XL3 LAST_MODIFIED=Thu Dec 16 15:10:25 2010
ENGINEER: RVB, PW	DATE: PAGE: 1 OF 17

TRANSLATOR 2 (XL2) REGISTER DEFINITIONS

FIRST REGISTER GROUP - CRATE CONTROL

ALWAYS ENABLED - IRREGARDLESS OF STATE OF REG 0

REG 0 - SELECT REGISTER

BITS 0..15 SELECT ANY (OR ALL) FECS 0..15

BIT 16 SELECT TRIGGER CARD

BIT 17 SELECT XL2 CARD

REG 1 - DATA AVAILABLE

BITS 0..15 DATA AVAILABLE IN FEC 0..15

BIT 16 DATA AVAILABLE IN TRIGGER CARD

BIT 17 DATA AVAILABLE IN XL2 CARD

BIT 30 REQUEST TO HALT BACKPLANE TRAFFIC

BIT 31 REQUEST FLAG - OR OF BITS 0..17, 30

REG 2 - XL2 CSR

BITS 0..4 GEOGRAPHIC CRATE ADDRESS, READ ONLY

BIT 6 LIGHT 'HALT ACK' LIGHT

BIT 7 CRATE RESET (OR'ED WITH SYSRESET)

BITS 8..11 XLINX CONTROL AND LOADS
8 = DONE_PROG* (R/W) (CF XILINX ACTIVE)
9 = DATA IN (TO FEC XILINX) (R/W)
10 = CONFIGURATION CLOCK (TO FEC XILINX) (R/W)
11 = XILINX ACTIVE FLAG - HOLDS SELECT REGISTER STEADY (R/W)

BITS 26..30 ERRORS, FROM XL2 LOGIC (TBD)

BIT 31 ERROR FLAG

REG 3 - MASKS

BITS 0..15 - MASK OFF DATA AVAILABLE FROM FECS 0..15

SECOND REGISTER GROUP - CLOCK, HVRELAYS, TEST

SECOND GROUP AND BEYOND REQUIRE CORRECT LOADING OF SELECT REGISTER (REG 0)

REG 4 - CLOCK CSR

BIT 0 = SHIFT CLOCK IN FOR MEMORY CLOCK

BIT 1 = DATA IN FOR MEMORY CLOCK

BIT 2 = OUTPUT ENABLE FOR MEMORY CLOCK

BIT 3 = SOFTWARE MEMORY CLOCK

BIT 4 = SHIFT CLOCK IN FOR SEQUENCER CLOCK

BIT 5 = DATA IN FOR SEQUENCER CLOCK

BIT 6 = OUTPUT ENABLE FOR SEQUENCER CLOCK

BIT 7 = SOFTWARE SEQUENCER CLOCK

BIT 8 = SHIFT CLOCK IN FOR ADC CLOCK

BIT 9 = DATA IN FOR ADC CLOCK

BIT 10 = OUTPUT ENABLE FOR ADC CLOCK

BIT 11 = SOFTWARE ADC CLOCK

BIT 12 = SPARE

BIT 13 = SPARE

BIT 14 = SPARE

BIT 15 = MASTER CLOCK ENABLE

REG 5 - HV RELAY CONTROL

BIT 0 - RELAY CLOCK

BIT 1 - RELAY DATA

BIT 2 - RELAY RESET

BIT 3 - RELAY DATA OUT

BIT 4 - RELAY LOAD

REG 6 - XILINX UBER CONTROL AND CHECK

BITS<8..5> - CONTROL - ENABLE XILINX LOAD IF = 0101

BITS<4..1> - ADDRESS LINE MODIFIERS (A<21..18>)

A<21> = 1 AND A<20> = 0 FORCES XILINX LOAD MODE ON MB

REG 7 - GENERAL READ/WRITE/DISPLAY TEST REGISTER

BITS<31..0> - DATA

THIRD REGISTER GROUP - HV CONTROL REGISTERS 8-11

REG 8 - HV CSR

R/W BIT 0 SET HV SUPPLY A AC POWER ON

R BIT 1 SPARE 1, SHOULD = 0

R BIT 2 HV INTERLOCK (BACKPLANE) STATUS (1 = ALL BOARDS IN)

R BITS 3..5 HV A ERROR CONDITIONS, TO BE DETERMINED

R/W BITS 6..7 HV A CONTROL BITS, TO BE DETERMINED

R/W BIT 16 SET HV SUPPLY B AC POWER ON

R BIT 17 SPARE 17, SHOULD = 0

R BITS 19..21 HV B ERROR CONDITIONS, TO BE DETERMINED

R/W BITS 22..23 HV B CONTROL BITS, TO BE DETERMINED

R BIT 31 ERROR FLAG

REG 9 - HV SETPOINTS

BITS 0..11 HV A SET POINT (LSB = 1/4096TH OF FSR)

BITS 16..27 HV B SET POINT (LSB = 1/4096TH OF FSR)

REG 10 - HV VOLTAGE READBACK

BITS 0..11 HV A VOLTAGE (LSB = 1/4096 OF FSR)

BITS 16..27 HV B VOLTAGE

REG 11 - HV CURRENT READBACK

BITS 0..11 HV A CURRENT (LSB = 1/4096 OF FSR)

BITS 16..27 HV B CURRENT

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TITLE: XL2A
VME EXTENDER SYSTEM

ABBREV=XL2A

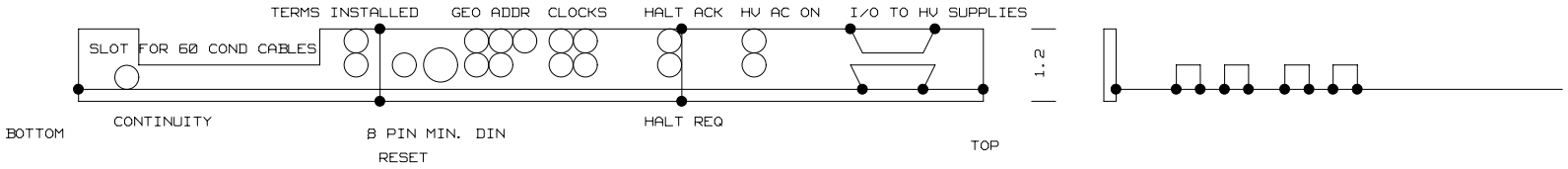
LAST_MODIFIED=Tue Sep 21 13:49:14 2010

DATE:

ENGINEER: RVB

PAGE: 2 OF 17

TRANSLATOR 2 (XL2) PANEL LAYOUT



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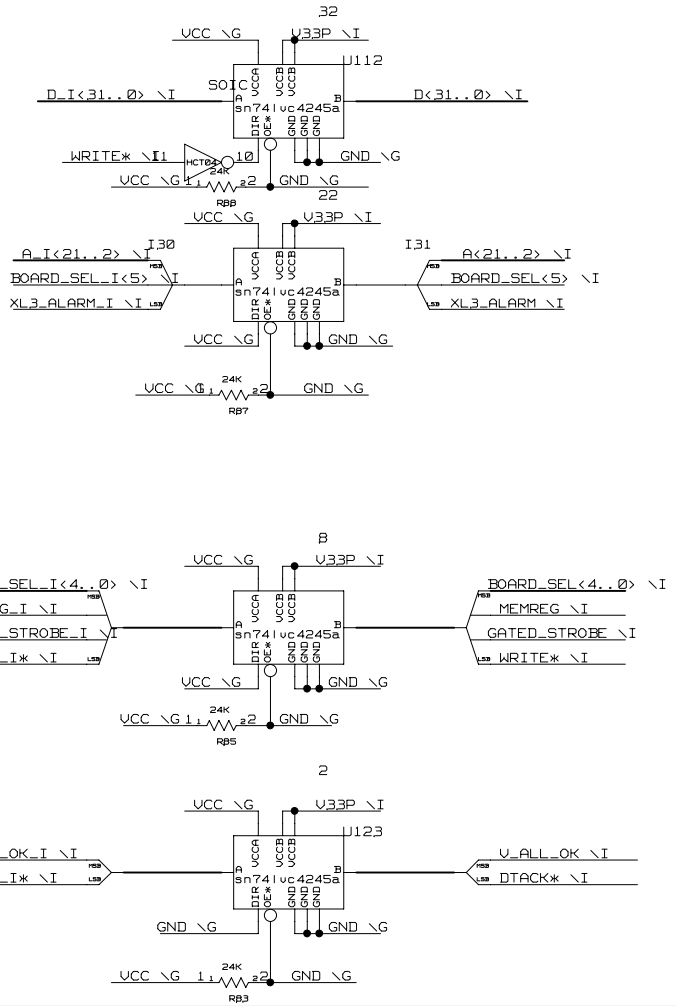
HIGH ENERGY PHYSICS

TITLE: XL2A VME EXTENDER SYSTEM ABBREV=XL2A LAST_MODIFIED=Tue Sep	DATE: 21 13:49:15 2010
ENGINEER: RVB	PAGE: 3 OF 13

XILINX INTERFACE



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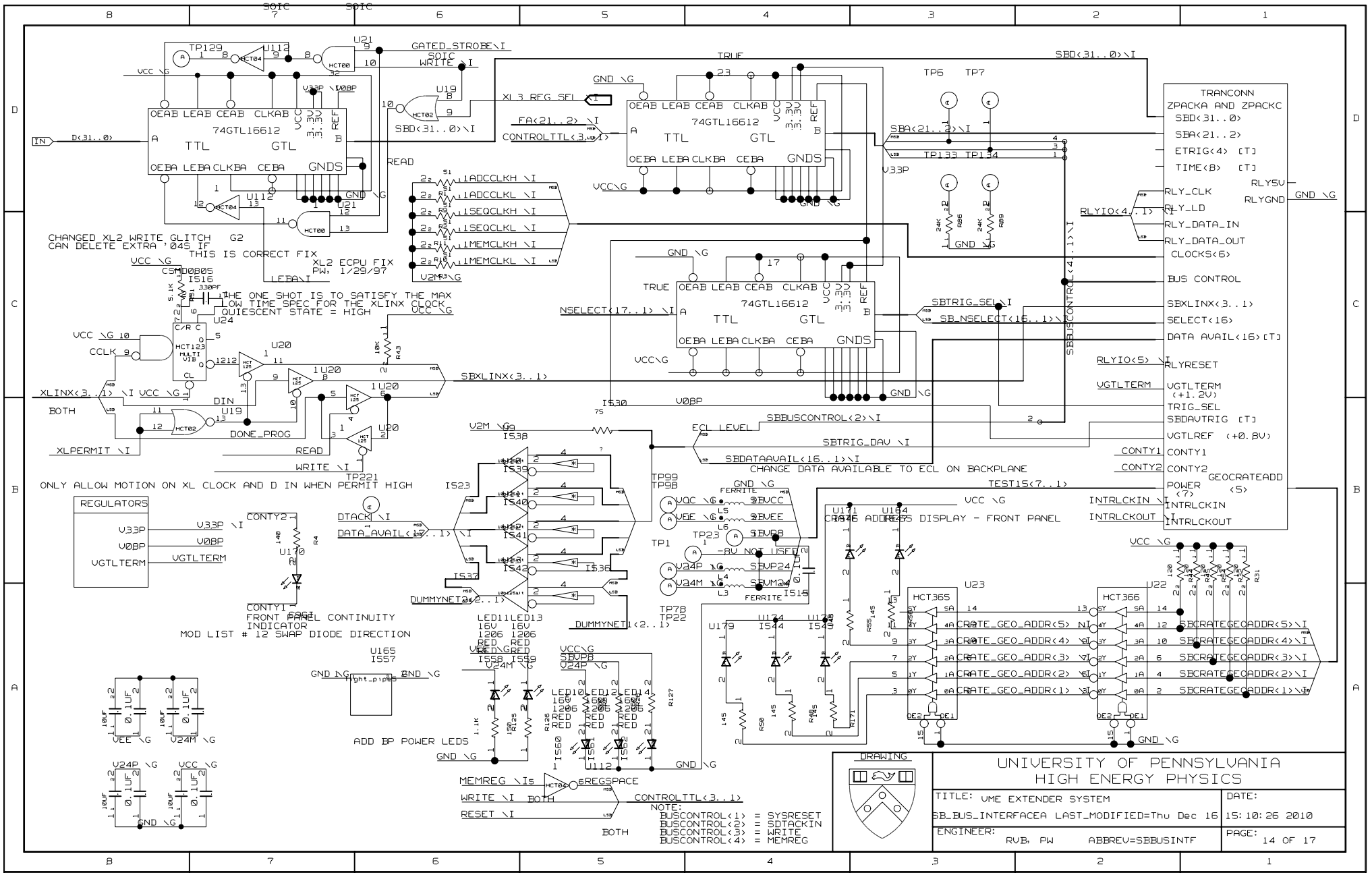
HIGH ENERGY PHYSICS

TITLE: CLOCK CLOCK LAST_MODIFIED=Thu Dec 16	DATE: 15:10:26 2010
ENGINEER: RVB	PAGE: 12 OF 17

SB BUS INTERFACEA



TRANCONN PAGE 1

SNOBUS PIN ARRANGEMENT - TRANSLATOR STATION

REVISED VERSION WITH:
NO MORE THAN 4 BUS LINES PER ROW
VMB ON C4, C5 PINS
SEPARATE ROWS FOR VP24, VM24
ADJUSTED TO ALLOW FOR PADDLE CARD ORIENTATION
CORRECTED VPB PIN IN C ROW

TRANSLATOR VIEW
TRANSLATOR TERMINATES THE TRIGGER AND TIMING BUSSES
TRANSLATOR DOES HAVE 17 SELECT LINES
NAMING: TOP SIGNALS END IN T, BOTTOM IN B
SB PREFIX = SNOBUS - BACKPLANE SIGNALS

HIGH/LOW TRUE FINAL OR PENULTIMATE H OR L

CONN165

	A		B		C		D		E
1	A1	SBGEOCA<1> \I	B1	SBGEOCA<2> \I	C1	SBGEOCA<3> \I	D1	SBGEOCA<4> \I	E1	CONTY1 \I
2	A2	SBESUMLB	B2	GND \G	C2	SBESUMHB	D2	SBGEOCA<5> \I	E2	GND \G
3	A3	GND \G	B3	GND \G	C3	GND \G	D3	GND \G	E3	GND \G
4	A4	SBGLTRH	B4	SBGLTRL	C4	VMB	D4	SBTESTTH	E4	SBTESTTL
5	A5	SBSYNCLRH	B5	SBSYNCLRL	C5	VMB	D5	SBSYNCLR24H	E5	SBSYNCLR24L
6	A6	GND \G	B6	GND \G	C6	GND \G	D6	GND \G	E6	GND \G
7	A7	GND \G	B7	SBA<2> \I	C7	SBA<3> \I	D7	SBA<4> \I	E7	SBA<5> \I
8	A8	SBA<6> \I	B8	GND \G	C8	SBA<7> \I	D8	SBA<8> \I	E8	SBA<9> \I
9	A9	SBA<10> \I	B9	SBA<11> \I	C9	GND \G	D9	SBA<12> \I	E9	SBA<13> \I
10	A10	SBA<14> \I	B10	SBA<15> \I	C10	SBA<16> \I	D10	GND \G	E10	SBA<17> \I
11	A11	SBA<18> \I	B11	SBA<19> \I	C11	SBA<20> \I	D11	SBA<21> \I	E11	GND \G
12	A12	GND \G	B12	SBD<0> \I	C12	SBD<1> \I	D12	SBD<2> \I	E12	SBD<3> \I
13	A13	SBD<4> \I	B13	SBD<5> \I	C13	SBD<6> \I	D13	GND \G	E13	SBD<7> \I
14	A14	SBD<8> \I	B14	SBD<9> \I	C14	GND \G	D14	SBD<10> \I	E14	SBD<11> \I
15	A15	SBD<12> \I	B15	GND \G	C15	SBD<13> \I	D15	SBD<14> \I	E15	SBD<15> \I
16	A16	GND \G	B16	SBD<16> \I	C16	SBD<17> \I	D16	SBD<18> \I	E16	SBD<19> \I
17	A17	SBD<20> \I	B17	SBD<21> \I	C17	SBD<22> \I	D17	SBD<23> \I	E17	GND \G
18	A18	SBD<24> \I	B18	SBD<25> \I	C18	SBD<26> \I	D18	GND \G	E18	SBD<27> \I
19	A19	SBD<28> \I	B19	SBD<29> \I	C19	GND \G	D19	SBD<30> \I	E19	SBD<31> \I
20	A20	SBREGSPACE	B20	GND \G	C20	VM24	D20	VM24	E20	SBRESET
21	A21	GND \G	B21	SBDTACK	C21	SBWRITE	D21	VGTLREF \I	E21	GND \G
22	A22	VP24	B22	VP24	C22	GND \G	D22	GND \G	E22	SBDONE_PROGXL
23	A23	SBDINXL	B23	GND \G	C23	SBCLKXL	D23	GND \G	E23	GND \G
24	A24	VPB	B24	VPB	C24	VPB	D24	VPB	E24	VPB
25	A25	GND \G	B25	GND \G	C25	GND \G	D25	GND \G	E25	GND \G
26	A26	VP5	B26	VP5	C26	VP5	D26	VP5	E26	VP5
27	A27	VP5	B27	VP5	C27	VP5	D27	VP5	E27	VP5
28	A28	SBCLKADH	B28	SBCLKADL	C28	GND \G	D28	SBCLKMEMH	E28	SBCLKMEML
29	A29	SBCLKSQH	B29	SBCLKSQL	C29	GND \G	D29	GND \G	E29	GND \G
30	A30	VM5	B30	VM5	C30	VM5	D30	VM5	E30	VM5
31	A31	VM5	B31	VM5	C31	VM5	D31	VM5	E31	VM5
32	A32	SBESUMLT	B32	GND \G	C32	SBESUMHT	D32	GND \G	E32	GND \G
33	A33	GND \G	B33	GND \G	C33	GND \G	D33	GND \G	E33	CONTY2 \I

REFDE1

TOP TRIGGER
GND LINE
TIMING
GEOGRAPHIC ADDRESS
BUS ADDRESS
BUS DATA
BUS CONTROL
XILINX LOAD PINS
MAIN POWER DIST
CLOCK
GND LINE
BOTTOM TRIGGER

SBREGSPACE
SBWRITE
SBDTACK
SBRESET
→ SBBUSCONTROL<4..1> \I

SBSYNCLRH
SBSYNCLRL
SBGLTRH
SBGLTRL
SBTESTTH
SBTESTTL
SBSYNCLR24H
SBSYNCLR24L
→ SBTIMEBUS<B..1> \I

SBCLKXL
SBDINXL
SBDONE_PROGXL
→ SBXLINX<3..1> \I

GND \G
VP5
VM5
VPB
VMB
VP24
VM24
→ POWER<7..1> \I

SBCLKADH
SBCLKADL
SBCLKSQH
SBCLKSQL
SBCLKMEMH
SBCLKMEML
→ SBCLOCKS<6..1> \I

SBESUMLT
SBESUMHT
SBESUMLB
SBESUMHB
→ SBETRIG<4..1> \I

THREE CLOCK VERSION -
SBCLKAD FOR ADCS
SBCKLSQ FOR SEQUENCER
SBCLKMEM FOR MEMORY

CONTY1 AND CONTY2 ARE CONNECTOR CONTINUITY TEST PINS

POWER IS:
+24V, -24V - ADCS, SOME OP AMPS/DACS, REFERENCES, TRIGGER
+B FOR BIPOLAR, DACS, -B FOR DACS
+5 FOR CMOS AND GENERAL LOGIC
-5.2 FOR ECL AND BIPOLAR

REFERENCES ARE:
VTRIGREF FOR CURRENT SUM BASE REFERENCES
VGTLREF FOR GTL TRANSCEIVER TERMINATIONS

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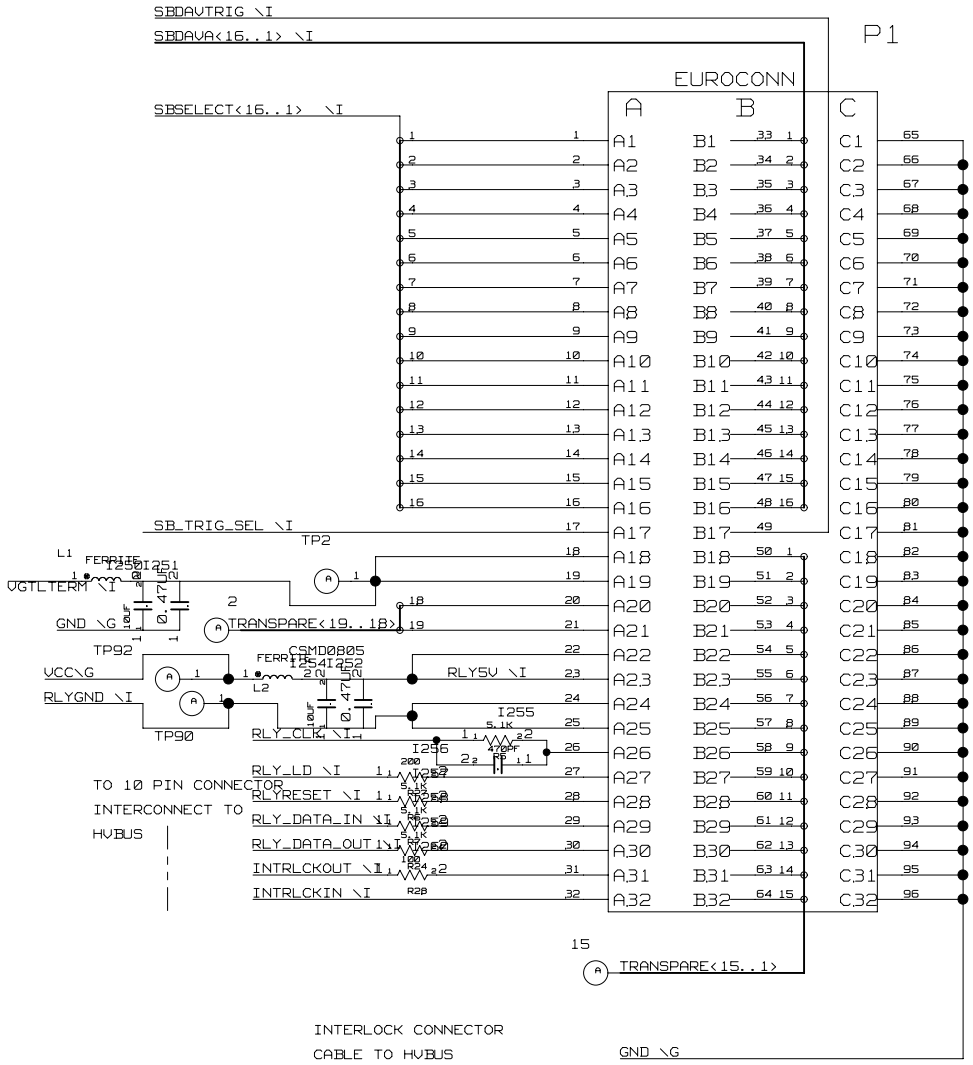
TITLE: TRANCONN	DATE:
LAST_MODIFIED=Thu Dec 16 15:10:27 2010	
ENGINEER: RVB	PAGE: 15 OF 17
ABBREV=TRANCONN	

TRANSLATOR J3 CONNECTOR



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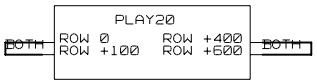
TITLE: TRANCONN LAST_MODIFIED=Thu Dec 16	DATE: 15:10:27 2010
ENGINEER: RVB TRANCONN	PAGE: 16 OF 17

PLAY AREA

ROOM FOR UP TO SIX 20 PIN DIPS.

PIN 41, 42 FOR GND, VCC
TRUE

SIZE=60



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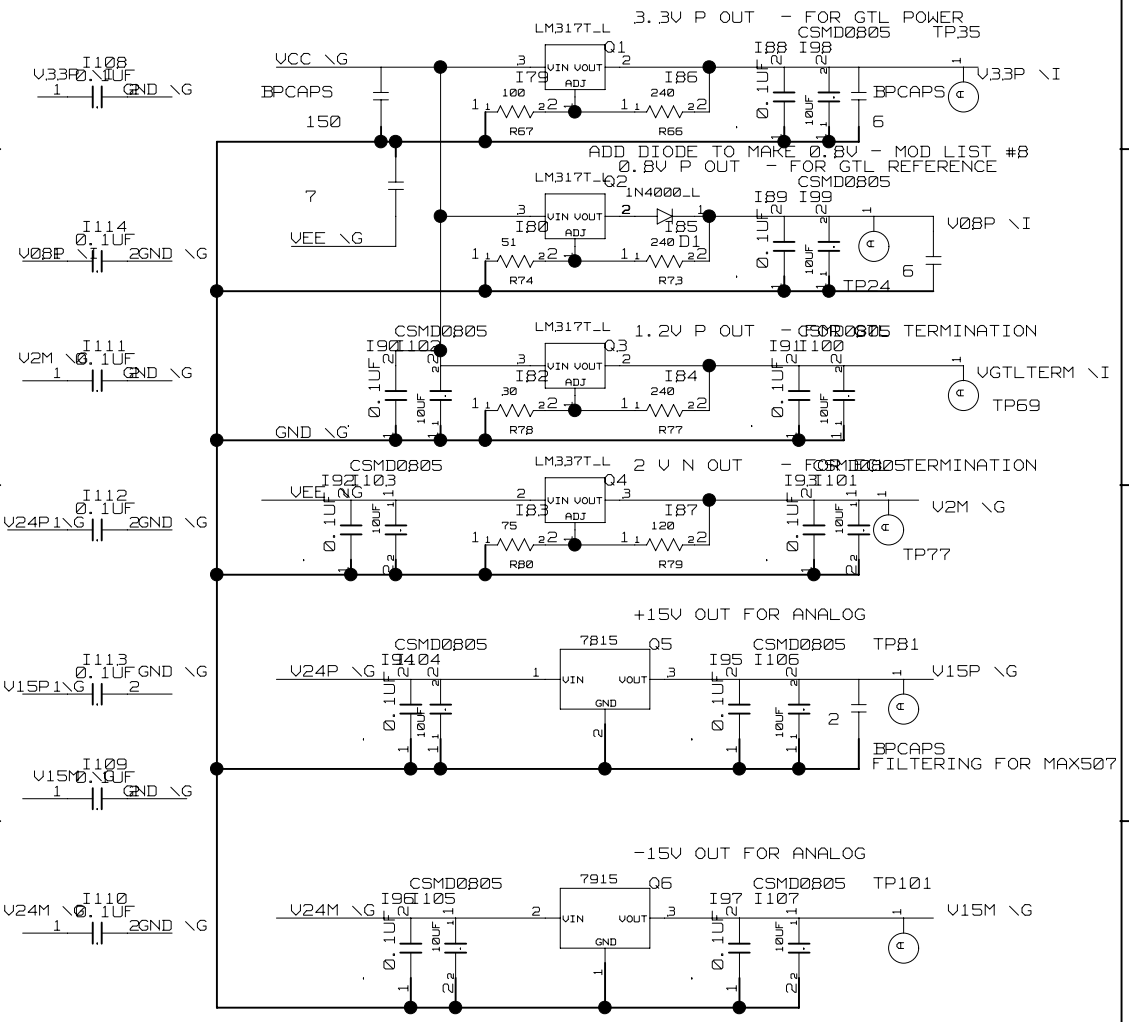
HIGH ENERGY PHYSICS

TITLE:	DATE:
TRANCONN LAST_MODIFIED=Tue Sep 21	13:47:20 2010
ENGINEER: RVB TRANCONN	PAGE: 17 OF 17

REGULATORS


3.3V P OUT - FOR GTL POWER
LM317T_L
CSMD0805
TP35
I108
V33P0.1UF
GND \G
VCC \G
BPCAPS
150
Q1
VIN VOUT
ADJ
I88 I98
I79
I86
100
240
R67
R66
0.1UF
10UF
V33P \I
BPCAPS
6
ADD DIODE TO MAKE 0.8V - MOD LIST #8
0.8V P OUT - FOR GTL REFERENCE
LM317T_L
Q2
1N4000_L
CSMD0805
I89 I99
I80
I85
D1
51
240
R74
R73
I114
0.1UF
V08P \I
GND \G
7
VEE \G
V08P \I
TP24
6
1.2V P OUT - FOR GTL TERMINATION
LM317T_L
CSMD0805
I111
V2M 0.1UF
GND \G
I90 I102
I91 I100
Q3
I82
I84
30
240
R78
R77
VGTLTERM \I
TP69
GND \G
2 V N OUT - FOR GTL TERMINATION
LM337T_L
CSMD0805
I112
V24P1\G
GND \G
I92 I103
I93 I101
Q4
I83
I87
75
120
R80
R79
V2M \G
TP77
+15V OUT FOR ANALOG
CSMD0805
7815
Q5
CSMD0805
TP81
I113
V15P1\G
GND \G
I94 I104
I95 I106
V24P \G
VIN
VOUT
GND
V15P \G
BPCAPS
FILTERING FOR MAX507
I109
V15M0.1UF
GND \G
-15V OUT FOR ANALOG
CSMD0805
7915
Q6
CSMD0805
TP101
I110
V24M \G
0.1UF
GND \G
I96 I105
I97 I107
V24M \G
V15M \G
PIN NAMES
V08P\I
V33P\I
VGTLTERM\I
24
24
GND \G
REPLICATE
A
FOUR OF THESE TESTPOINTS ARE 109 VME ASSEMBLY HOLES
LAST_MODIFIED=Thu Dec 16 15:10:28 2010
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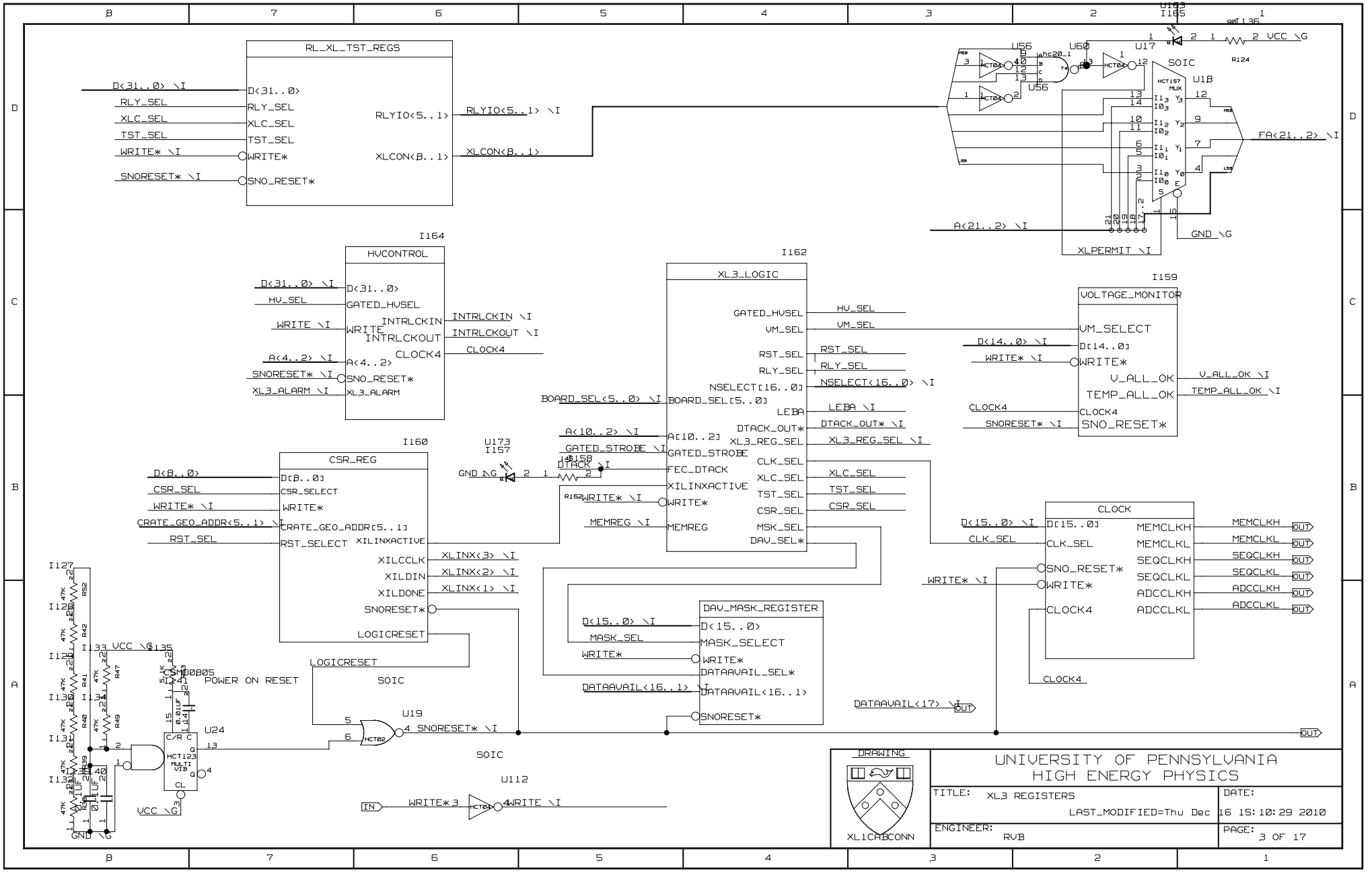
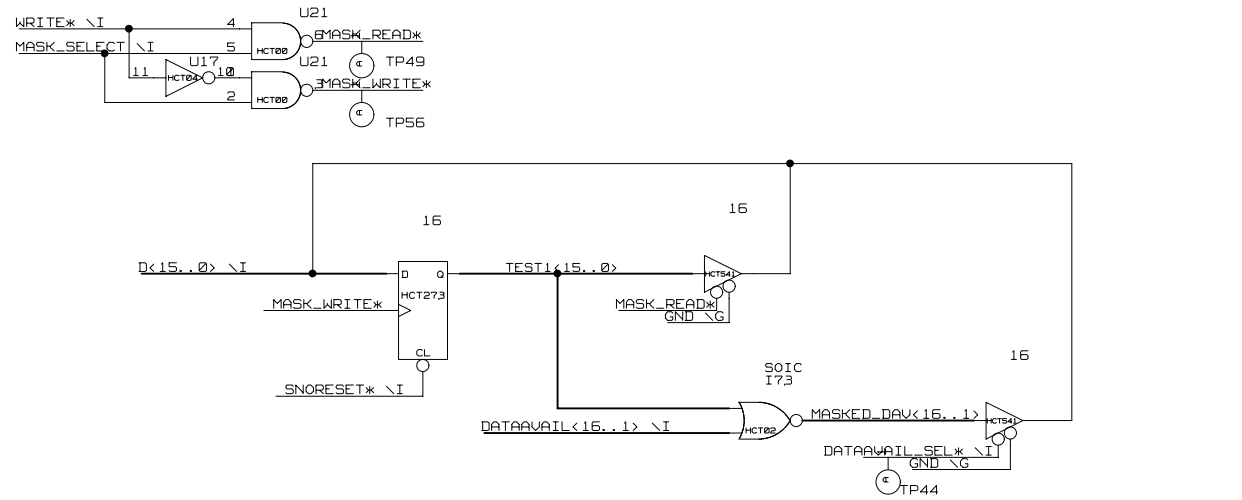
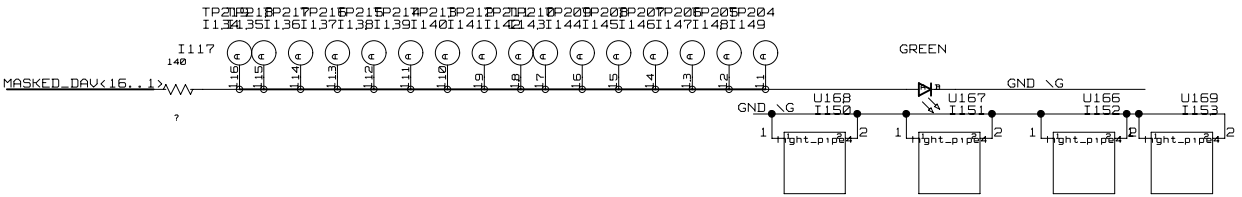
HIGH ENERGY PHYSICS
TITLE: REGULATORS
REGULATORS
DATE:
ENGINEER: RVB, PW
PAGE:
17A OF 17

XL3 REGISTERS



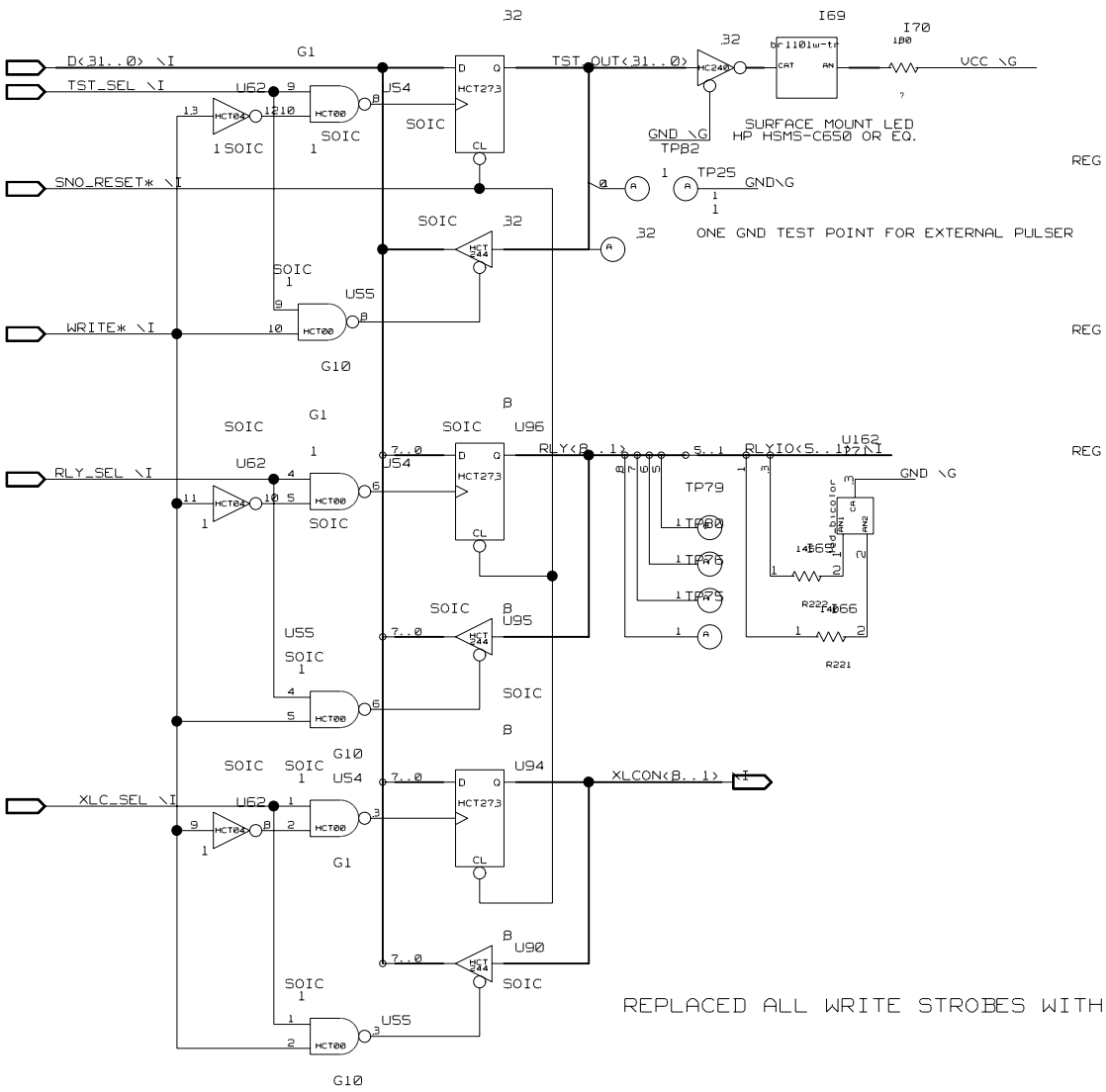
DATA AVAILABLE AND MASK REGISTER





DRAWING	UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
XL1CABCONN	TITLE: SELECT REGISTER LAST_MODIFIED=Thu Dec 16 15:10:30 2010	DATE:
	ENGINEER: RVB	PAGE: 3 OF 17

RELAY XILINX<LOAD> TEST REGISTERS



REG 5 - HV RELAY CONTROL
BIT 0 - RELAY CLOCK
BIT 1 - RELAY DATA
BIT 2 - RELAY RESET
BIT 3 - RELAY DATA OUT
BIT 4 - RELAY LOAD
BIT 5 - RELAY RESET

REG 6 - XILINX UBER CONTROL AND CHECK
BITS<8..5> - CONTROL - ENABLE XILINX LOAD IF = 0101
BITS<4..1> - ADDRESS LINE MODIFIERS <A<21..18>>
A<21> = 1 AND A<20> = 0 FORCES XILINX LOAD MODE ON MB

REG 7 - GENERAL READ/WRITE/DISPLAY TEST REGISTER
BITS<31..0> - DATA
USE ONE BIT FOR EXTERNAL PULSER.

REPLACED ALL WRITE STROBES WITH INVERTED TO MATCH CLOCK REG STROBE ASSERTION

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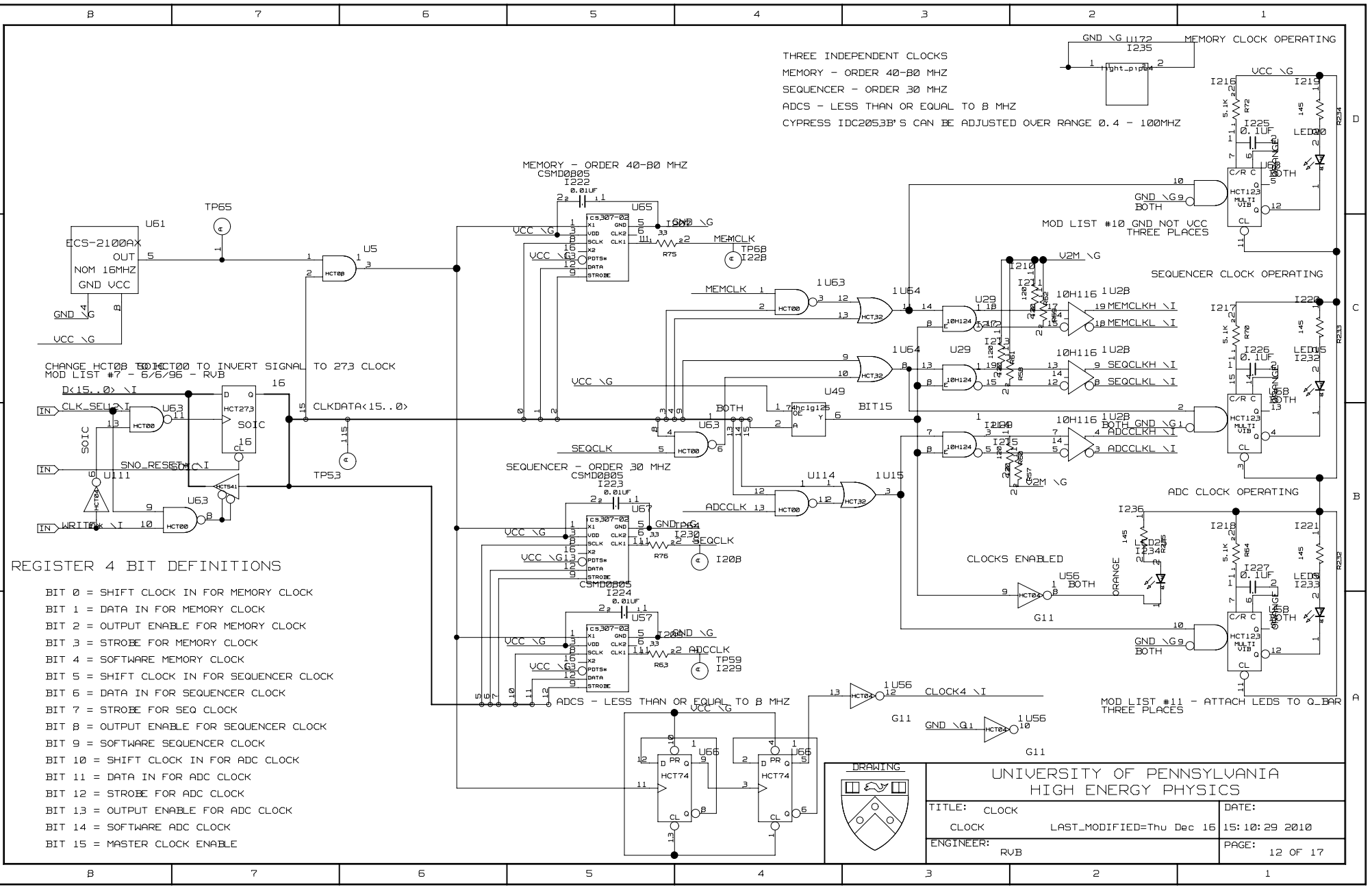
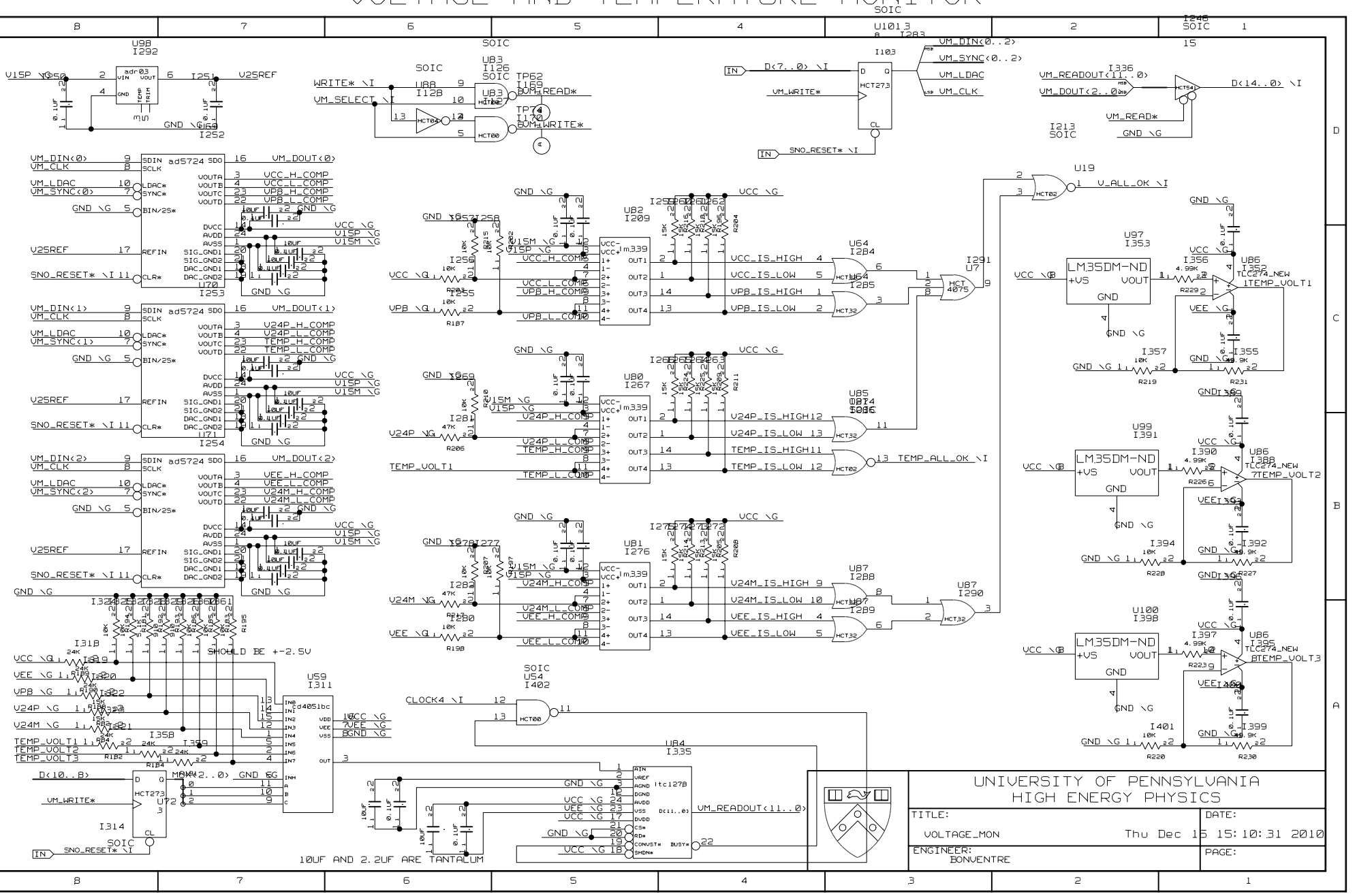
TITLE: RL_XL_TST_REGS	DATE:
RLXLTSTREG LAST_MODIFIED=Thu Dec 16 15:10:30 2010	
ENGINEER: RVB	PAGE: 1

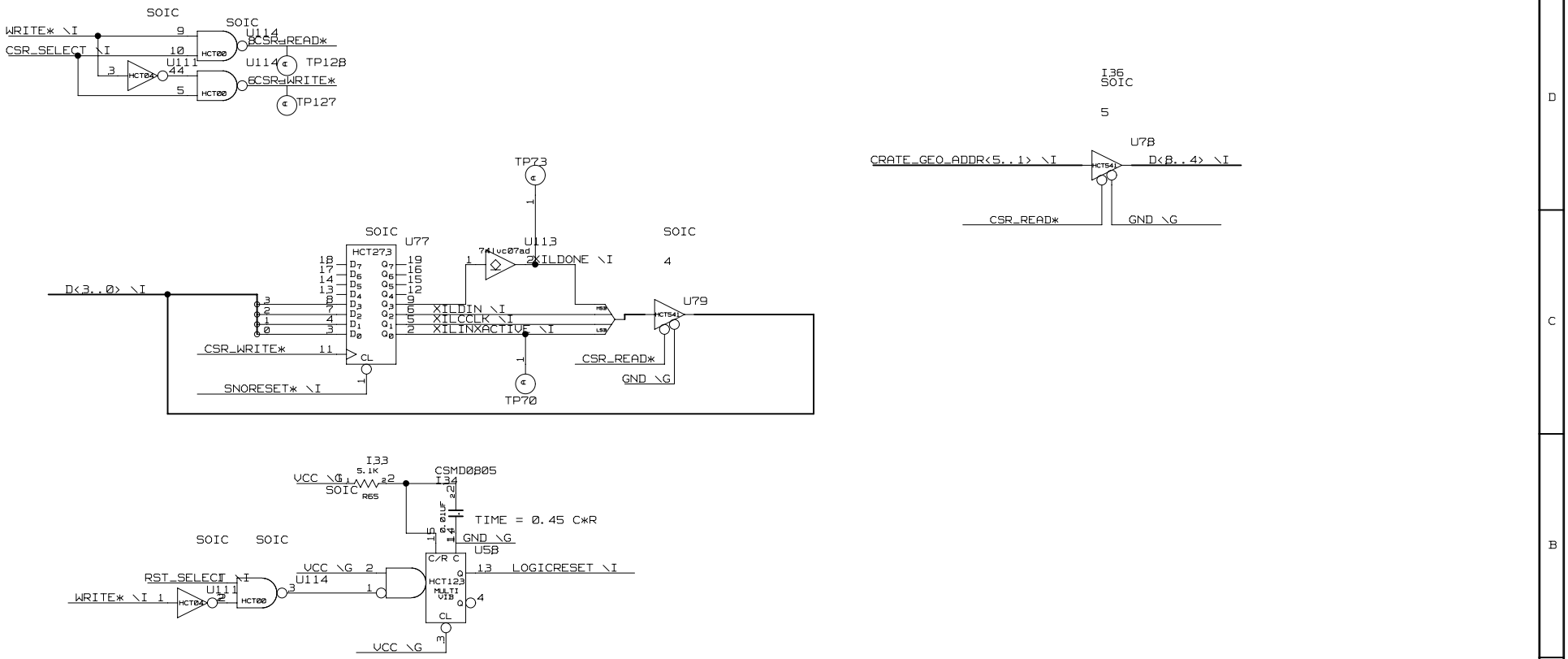
REGISTER 4 - CLOCK



VOLTAGE AND TEMPERATURE MONITOR



CONTROL AND STATUS REGISTER



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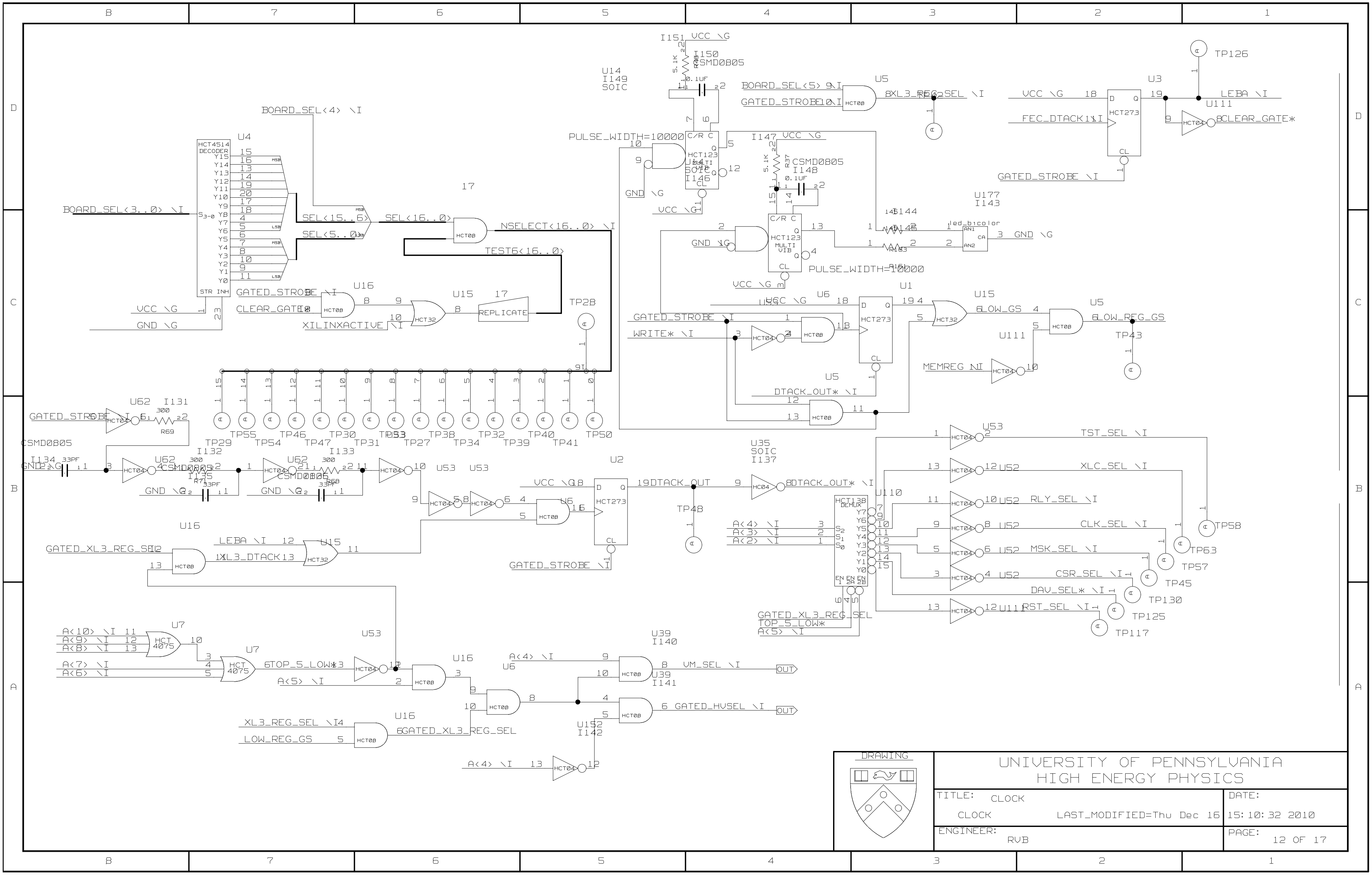
HIGH ENERGY PHYSICS

TITLE: CSR_REG VME EXTENDER SYSTEM	ABBREV=CSR_REG LAST_MODIFIED=Thu Dec 16 15:10:32 2010
ENGINEER: RVB, PW	PAGE: 6 OF 17

XL3 LOGIC AND ADDRESS DECODING



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HIGH ENERGY PHYSICS

TITLE: CLOCK

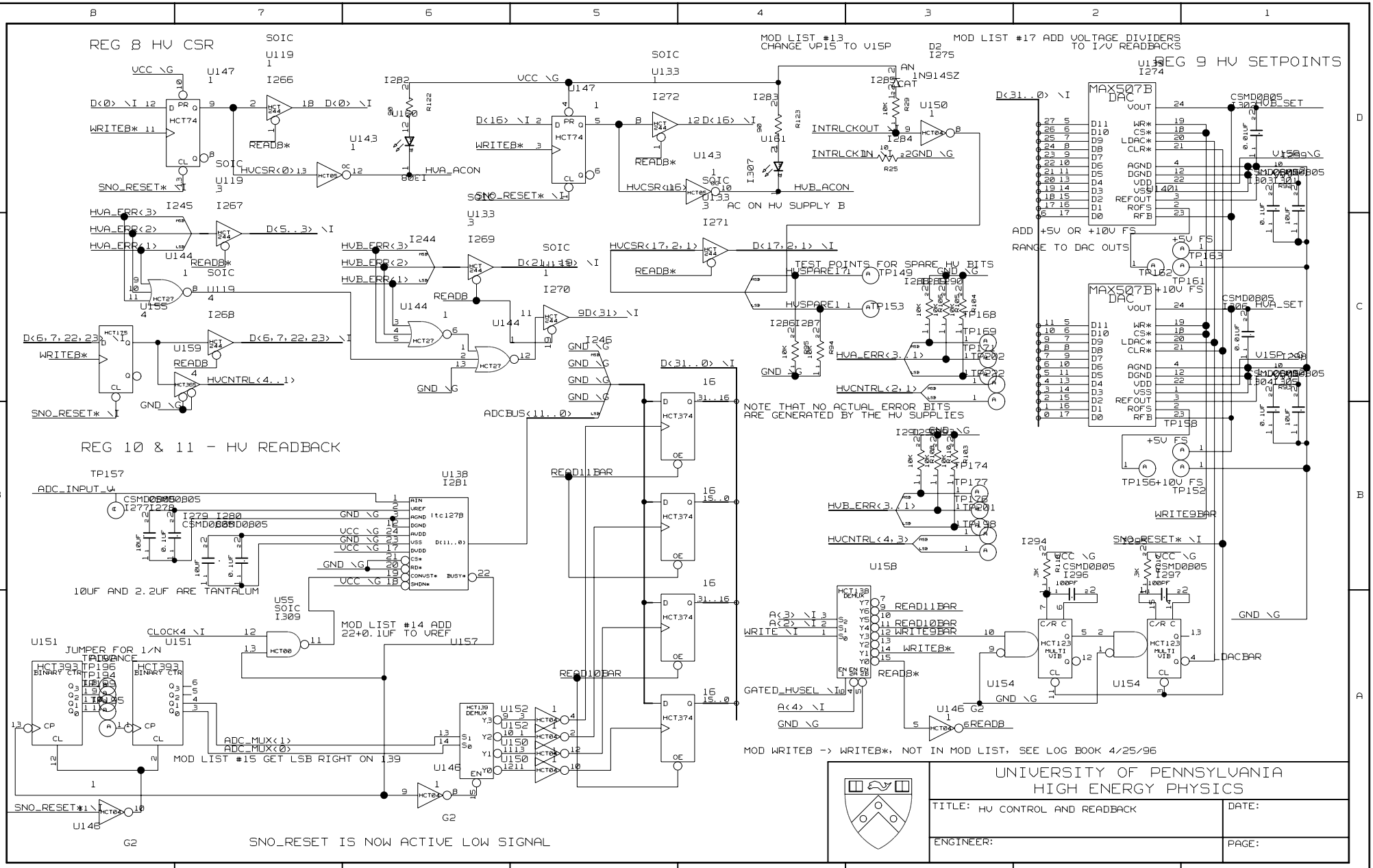
CLOCK LAST_MODIFIED=Thu Dec 16

DATE: 15:10:32 2010

ENGINEER: RVB

PAGE: 12 OF 17

HV CONTROL AND READBACK - MODS TO V2.0

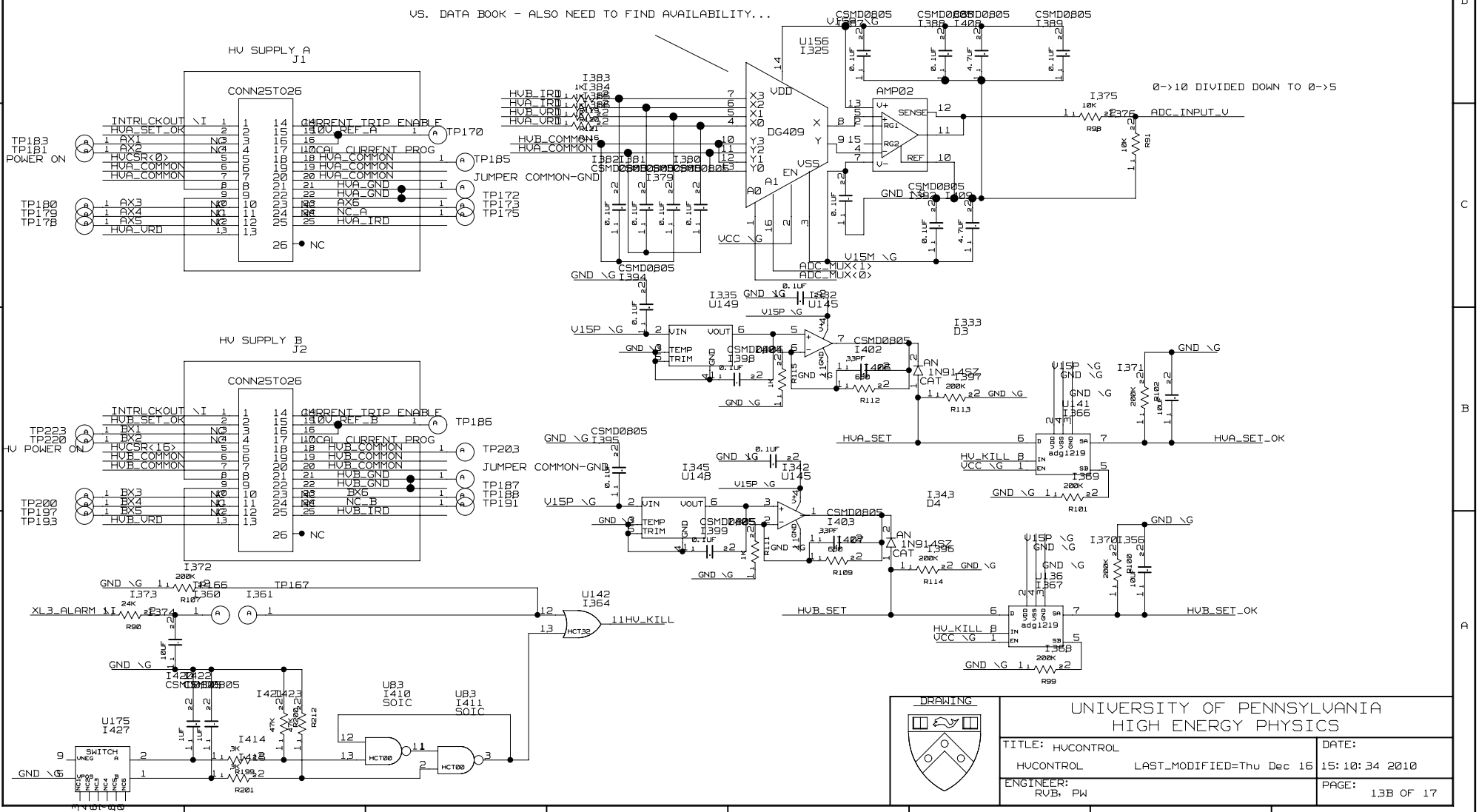


HV CONTROL AND READBACK - MODS TO V2.0

GLASSMAN MODEL MR CONNECTIONS AND SCALING

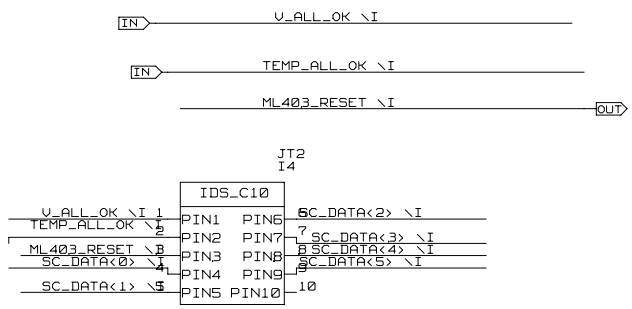
CAREFUL OF THIS PART - CHECK PHYSICAL AND LOGICAL DESCRIPTION
VS. DATA BOOK - ALSO NEED TO FIND AVAILABILITY...

DG409 TO ALLOW 0--> +10V SWING ON INPUT



DRAWING	UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS
TITLE: HVCONTROL HVCONTROL LAST_MODIFIED=Thu Dec 16	DATE: 15:10:34 2010
ENGINEER: RVB, PW	PAGE: 13B OF 17

XL3 LOGIC AND ADDRESS DECODING



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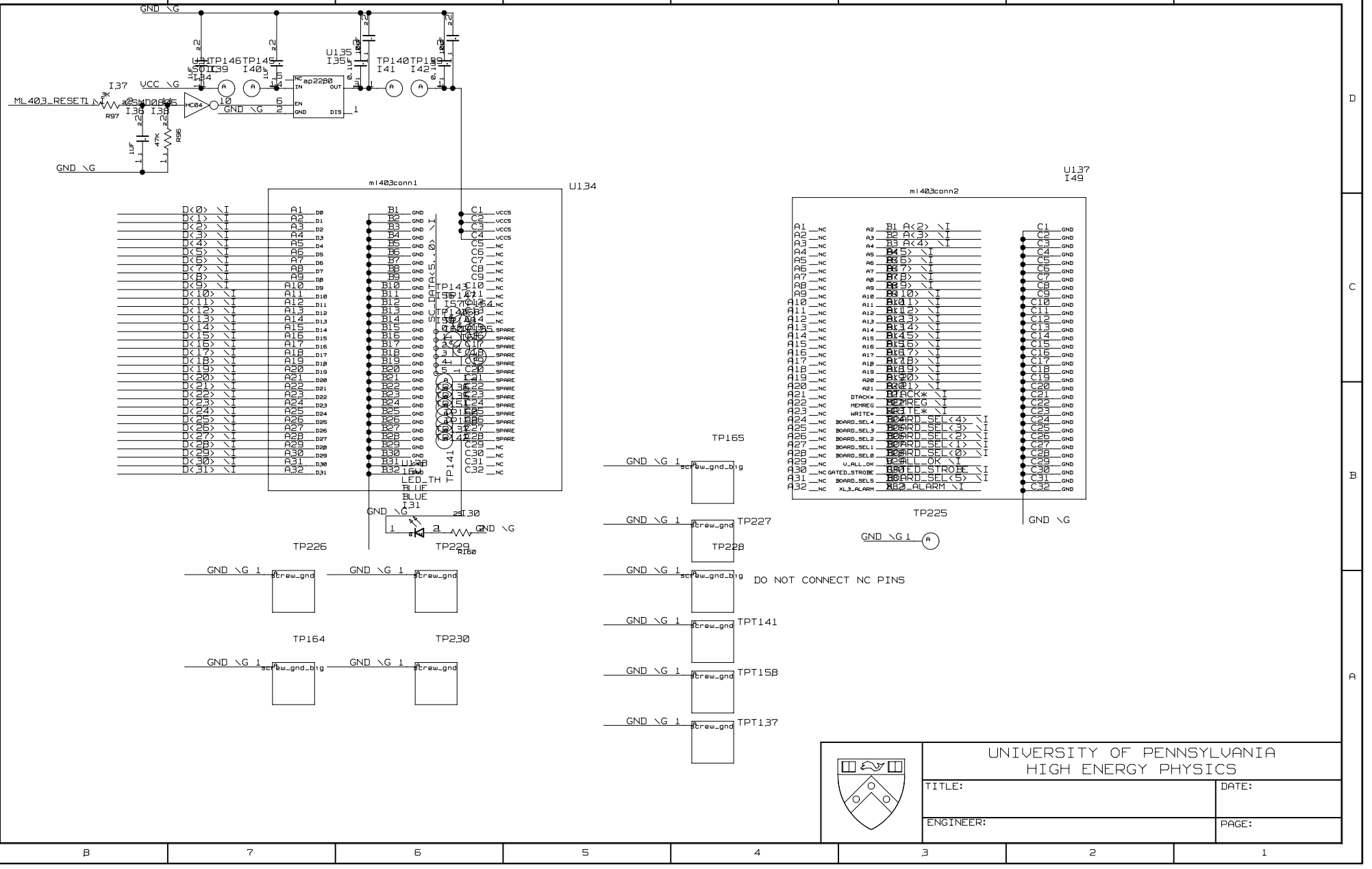
HIGH ENERGY PHYSICS

TITLE: CLOCK CLOCK LAST_MODIFIED=Thu Dec 16	DATE: 15:10:34 2010
ENGINEER: RVB	PAGE: 12 OF 17


GND \G
VCC \G
ML403_RESET1
R97
R96
ml403conn1
U1,34
ml403conn2
U1,37
I49
TP225
TP226
TP229
TP164
TP230
TP165
TP227
TP228
TPT141
TPT158
TPT137
DO NOT CONNECT NC PINS
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TITLE:
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