

This article was initially published in Planet Analog, a magazine supplement to EE Times, (c) CMP Media LLC.

## LVDS, CML, ECL-differential interfaces with odd voltages

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There are many differential signaling technologies available today. Some are defined by industry standard committees, such as the TIA, IEEE, or JEDEC groups. Others are more "vendor specific" flavors and may have unique electrical characteristics all their own. Both types were developed for different reasons, some focus on ultra speed such as ECL and CML, while others focused on two or more attributes. LVDS for example, focused on both high-speed and low-power operation. Here is what you should know about some of today's popular high-speed differential interface technologies.

The three popular high-speed differential interface technologies discussed are: LVDS - Low Voltage Differential Signaling, ECL - Emitter Coupled Logic, and PECL / LVPECL options CML - Current Mode Logic.

There are some additional variants of each of these, however they tend to be application specific or less common and are therefore beyond the scope of this article. There are also many other interface technologies that are not differential, thus they tend not to support high-speed (>1Gbps) operation and are typically limited by their small noise margins. Examples of these are standard logic swings (LVCMOS), HSTL, BTL, and GTL. An overview of these can be found in National's [Applications Note #1123](#) titled "Sorting out the Backplane Driver Alphabet Soup".

### Three for Speed: ECL - LVDS - CML

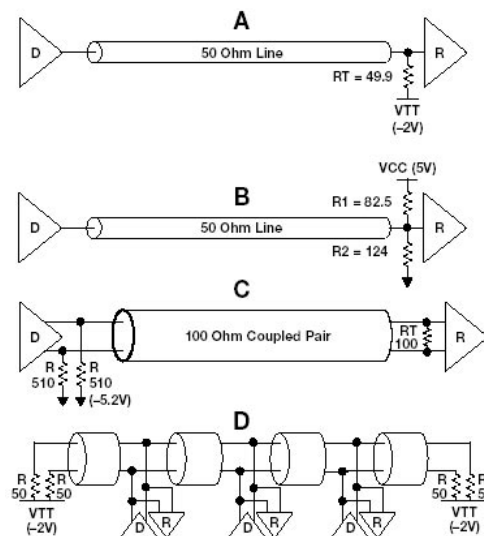
ECL - Emitter Coupled Logic - is the oldest of the three and dates back to the early 1960s. Motorola pioneered ECL with its MECL (Motorola ECL) family. Since then ECL has evolved into many enhanced families. These include the 10k, 100k, ECLinPS, and even some more recent flavours such as RSECL for Reduced Swing ECL, which features an LVDS-like 400mV, output swing. Fairchild, also an ECL pioneer brought out the first sub-nano second ECL parts in the early 1970s. The 100k family brought the critical feature of supply voltage and temperature compensation, providing a very stable output. ECL can be used single-endedly or differentially depending upon the application and noise margins needed. The drivers are low impedance open emitter outputs that generate a typical 700 to 800 mV output voltage. The output stage is operated in the active region, saturation is prevented, thus ECL's famous fast and balanced edge rates are obtained. The output is typically terminated with 50 Ohms to a termination rail that is two volts less than the more positive rail. ECL parts are commonly powered between ground and -5.2V. Due to the negative rail requirement and compatibility with other popular devices (logic, ASICs,  $\mu$ Ps...), the positive rail operation of ECL was promoted. PECL - Positive Emitter Coupled Logic, also sometime referred to as Pseudo ECL is really just operating the ECL devices between and positive voltage and ground, vs ground and a negative voltage. LVPECL - Low Voltage PECL - is the term used to describe PECL that is powered from a 3.3V power supply. There are even other versions available today that support operation from rails less than 3.3V.

ECL has been more of a defacto standard with major vendors providing different families. Within a few standards, ECL has been standardized as the physical layer. This includes the TIA's [ANSI/TIA/EIA-612](#) "Electrical Characteristics for an Interface at Data Signaling Rates to 52 Mbit/s". This standard defines the driver output and receiver input characteristics of 100k ECL. The '612 standard maybe used with the [ANSI/TIA/EIA-613](#) standard "High Speed Serial Interface (HSSI) for Data terminal Equipment and Data Circuit Terminating Equipment" which specifies the mechanical and functional requirements the HSSI interface. HSSI was developed by Cisco Systems and T3plus Networks and later standardized by the TIA.

ECL has also been standardized by ANSI in the HIPPI (High-Performance Parallel Interface) standards. The HIPPI standards are also complete standards defining all electrical, mechanical and functional parameters for various HIPPI applications. The TIA/EIA-612 standard is unique in that it partitions the electrical portion in its own standard allowing it to be referenced by other applications or standards.

Key points on ECL, are its fast and balanced output edges, a low output impedance, high drive capability, and differential or single-ended operation. Limiting factors of ECL have been the negative rails, compatibility with other devices, the need for the terminating rail (VTT), and typically higher power dissipation.

Several bus configurations are shown in figure 1 for ECL.



**Figure 1:** A: ECL terminated in 50 Ohms to VTT; B: PECL terminated by Thevenin network,  $R1/R2 = 50$  Ohms; C: Differential ECL terminated by 100 Ohm parallel termination; D: Differential ECL Multipoint bus terminated by 50 Ohms to VTT at each end of the bus.

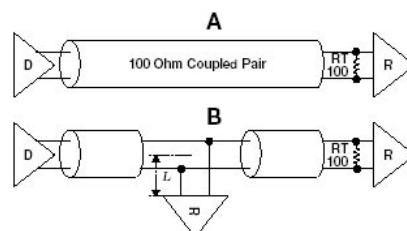
Figure 1A shows a common point-to-point application with a 50 Ohm termination to the VTT rail. Figure 1B is the same application but is PECL and uses a Thevenin termination to generate the VTT, with the penalty of increased power dissipation (8X). If only a few lines are required in the application this is typically the preferred implementation. If many lines are required, it is typically better to employ a dedicated VTT rail for termination purposes. If mixing PECL and CMOS devices, two separate power planes are recommended. Figure 1C shows the common differential point-to-point interconnection for ECL. Since a 100-Ohm parallel termination is used, pull

downs at the driver are required. Figure 1D shows a multipoint ECL backplane application.

**LVDS** - Low Voltage Differential Signaling - dates back to the early 1990s and was pioneered by National Semiconductor. National directly helped standardize LVDS at that time being the editor of both the IEEE and TIA projects. LVDS is standardized as an electrical layer standard by the TIA and is published as [ANSI/TIA/EIA-644-A](#). An IEEE project at that time was working on a standard known as SCI, which originally specified an ECL interface. An addendum was added that specified a lower swing, lower power alternative to ECL, which was the IEEE version of LVDS (a.k.a. IEEE 1596.3). Due to its vertical application, the generic TIA version of LVDS is more common today. In fact it has been specified as the physical layer in many applications ranging from flat panel notebook displays to frame grabbers to optical transceivers and many others.

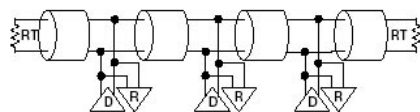
National developed and offered many industry firsts in LVDS which included FPD Link, Channel-Link, Military grade LVDS and even the first stand-alone line driver / receiver standard products.

LVDS is a high-speed and low-power differential interface for generic applications. It supports both point-to-point and also multidrop bus configurations as shown in figure 2. This flexibility makes it very versatile. The driver provides a typical 350mV differential output voltage centered at about +1.25V. The receiver is specified with a 100mV threshold over the receiver's input range of ground to +2.4V. This allows for the nominal active signal to shift up or down 1V in common-mode due to ground potential differences or coupled noise. The driver is intended to be used with 100-Ohm interconnects terminated in 100-Ohms. Data rate is device and application specific but it tends to be in the DC to 2.5Gbps range. Power is minimized in three ways. The load current is limited to 3.5mA, the current mode driver tends to limit dynamic power dissipation, and static current is minimized by the use of sub-micron CMOS processes. LVDS is unique in that it delivers high-speed operation while consuming little power.



**Figure 2:** A: LVDS terminated by 100 Ohm parallel termination; B: Multidrop LVDS terminated by 100 Ohm parallel termination at the far end only, stubs off the main line (1) should be minimized in length.

A newer related LVDS standard is the [ANSI/TIA/EIA-899](#) standard known as M-LVDS. This version supports a multipoint bus with double terminations. Due to the bus configuration and stub lengths, M-LVDS is limited to 500 Mbps or less. A multipoint M-LVDS bus is shown in figure 3. There are several other vendor specific flavors of LVDS, such as National's BLVDS. Details on these flavours can be found in the [National Edge](#) titled "The Many Flavours of LVDS".

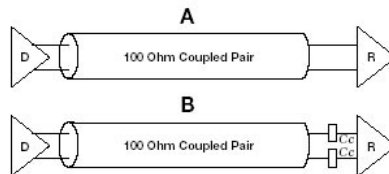


**Figure 3:** Multipoint LVDS bus terminated by two parallel terminations which are equal to 100 Ohms or the effective loaded impedance of the bus - typically in the 54 to 100 Ohm range.

LVDS and M-LVDS provide true odd mode transmission and equal and opposite currents flow within the pair. This and the small output current (3.5mA) tends to make LVDS low in EMI. LVDS is a very versatile technology, and supports a variety of bus configurations.

**CML** - Current Mode Logic - The origins of CML are more difficult to track. CML tends to be mainly a vendor implementation with less official standardization. This makes its roots more difficult to track. Some state that it predates ECL with origins at General Electric, others note that it grew out of I<sup>2</sup>L, (Injection Current Logic), or CCSL (Compatible Current-sinking logic) in the 1980s. Still others state some work in the early 1990s as its source. Many others see it as simply upside-down ECL. Today CML has become very popular due to its simplicity and speed especially for multi-gigabit SerDes applications.

CML is a high-speed point-to-point interface as shown in figure 4. A unique feature of CML is that it typically does not require any external resistors as termination is provided internally by both the driver and the receiver devices. CML supports data rates above 10 Gbps depending upon the process for the drivers and receivers. CML may be DC coupled or AC coupled if encoding is used. CML uses a passive pull up to the supply rail, which is typically 50 Ohms. CML tends to be vendor specific, so a careful review of datasheets is recommended to determine inter-operation especially in DC coupled applications.



**Figure 4:** A: Point-to-Point CML with internal source and load terminations - 50 Ohm pull ups to the positive rail; B: AC coupled Point-to-Point CML with internal source and load terminations - driver and receiver may be powered from different rails.

While not explicitly standardized, CML implementations can meet the requirements of Clause 47 of the IEEE 802.3 standard that defines the physical layer of the XAUI interface. Most implementations of XAUI SerDes parts feature a CML interface on the high-speed side.

Limitations of CML are mainly in the point-to-point bus configuration. However for ultra high-speed (>1Gbps) applications, a restriction to point-to-point is already required.

#### Comparing and contrasting -

Now that we have reviewed the origins and basics of ECL, LVDS, and CML, we can review a few specifications and compare them. Key electrical specs are shown in the table 1 and graphically in figure 5.

**Table 1: Key specifications table.**

Parameter	LVDS	PECL (5V)	LVPECL (3.3V)	CML*
TX VOH	1.425V	4.0V	2.3V	VCC
TX VOL	1.075V	3.2V	1.6V	VCC - 0.8V
TX VOD	350mV	800mV	0.7V	800mV
TX VOS	1.25V	3.6V	1.95V	VCC - 0.4V
TX RT	100 Ohm	50 Ohm	50 Ohm	50 Ohm
RX VTH	±100mV	±100-200mV	±100mV	±50mV
RX VIN	GND to 2.4V	Depends	Depends	Limited

\*CML numbers are shown for an 800mV output example; 400mV is also common.

LVDS provides the smallest swing of 350mV and a robust common-mode range of +/-1V around its VOS. It is mainly for point-to-point or multidrop applications with certain flavors supporting multipoint. Due to the output current and edge rates, LVDS is targeted more for the DC to 2Gbps range. It also tends to be the lowest power of the three.

ECL (PECL/LVPECL) provides a 700 to 800mV output swing. Depending upon the receiver used, it may have similar thresholds and common-mode range as LVDS, but tends to be more restrictive. It is also versatile and can support point-to-point, multidrop, or multipoint applications. ECL operates from DC to >10Gbps depending upon the family.

CML provides an 800mV swing in certain implementations. Being highly vendor specific, many parts offer control of the output swing and the 800mV may be adjustable down to a few hundred millivolts to minimize crosstalk. CML is for point-to-point links only and provides matched source and load terminations. This greatly simplifies the interconnect and stub lengths (termination to RX input) are minimized, thus signal quality is optimized. Due to the fact that one side is pulled to the rail, both the driver and receiver should be powered from the same supply potential for DC coupled applications. This is one reason that AC coupling is popular with CML interfaces. It provides common-mode tolerance, fault protection and also supply independency.

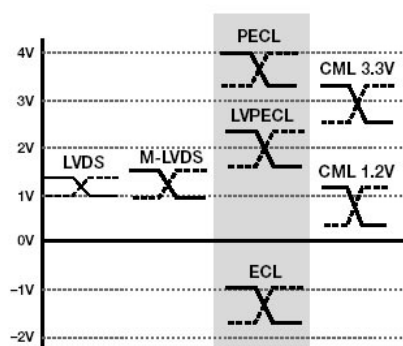


Figure 5: Signal swing comparisons showing differential output voltage and driver offsets of LVDS, ECL and CML.

Table 2 summarizes the more unique attributes of the three. Common application space is noted. Special parts or special flavors may address certain features or limitations.

Table 2 - Unique attributes.

	ECL	LVDS	CML
Bus Structure	Point-to-Point, Multidrop, Multipoint	Point-to-Point, Multidrop, Multipoint*	Point-to-Point
Power Dissipation	high	low	med
Speed	DC to >10Gbps	DC to >2Gbps	DC to >10Gbps
Coupling	DC or AC	DC	DC or AC
Process	Bipolar	CMOS, BiCMOS	Bipolar, CMOS

\* = Multipoint is supported with M-LVDS

#### Eye Opening extensions -

Signal conditioning may further enhance all three technologies. This includes signal modification at the source end with either pre-emphasis or de-emphasis. Or post equalization at the load end with special amplifier stages and or equalizer (analog or digital) circuits in the front-end of the receiver device. The information sent may also be "optimized" for data transmission. Encoding of the data can be done to lessen the ISI effects and improve signal quality. One example of this is the popular 8b/10b encoding that guarantees a minimum number of transitions per frame, and DC balance of the data; these two attributes also lessen ISI effects. This of course also makes the transmission compatible with AC coupling but requires 20% overhead.

#### Inter-Operation of different technologies

In some applications an interface between different technologies may be desired. Before making the connection, a review of the two interfaces needs to be made. First check that the mechanical (connector) and the functional (protocol) are compatible. Once this is done, the electrical compatibility should be checked. The following items should be checked: driver output level and offset, termination, and receiver input threshold and input range. Depending upon the interface, there may be wide variability between specific vendors implementations - therefore a careful review of each device's datasheet is recommended. For example some PECL inputs support an input range that is less than the supply rail, while others allow input voltages outside of the device's rails.

#### Driver

Note the following for the driver: minimum and maximum output differential voltage, the offset of the output swing and also the intended termination impedance. For LVDS this would be the following: VOD of 250 to 450 mV, and an offset of 1.25V. The LVDS driver is intended to be loaded with a 100-Ohm load connected across the pair.

## Receiver

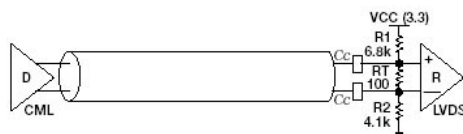
Note the following for the receiver: threshold sensitivity, input voltage range, and also check if there is a limitation on the maximum input voltage. For LVDS this would be the following: 100mV thresholds, a Ground to 2.4V input range, and a 2.4V maximum input voltage. These receiver numbers are based on ANSI/TIA/EIA-644-A requirements, however some receivers may offer extended performance. For example, National's DS90CP22 2X2 Crosspoint switch supports input voltages up to 3.3V allowing for direct LVPECL inter-operation..

With the above information noted, a simple comparison of compatibility needs to be done. Does the minimum driver output differential voltage exceed the receiver threshold level with enough noise margin? Does that maximum output swing of the driver fall within the input voltage range of the receiver taking into account the offset and maximum differential output voltage? Does the driver see its intended termination load? If the answer to these questions is yes, then a direct connection is typically possible.

If the answer to one for more of these questions was no, then a connection may still be possible but with the use of passive components. Level shifting can be accomplished by the use of resistors, and isolation can be accomplished with capacitors. Two examples are provided next. A more detailed generic discussion on inter-operation can be found in National's [Applications Note #972](#) titled "Inter-Operation of Interface Standards".

## CML - LVDS Interoperation

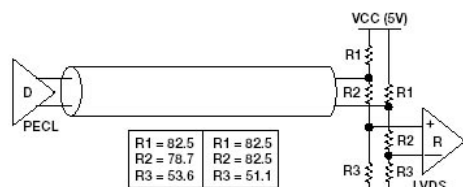
A CML driver will typically be AC coupled. The line will want to be terminated at the far end in its termination impedance. A failsafe network can be used to protect for when the driver is off and to also provide a bias point due to the AC coupling. In this example a +30mV failsafe bias is provided.



**Figure 6:** CML to LVDS - RT presents a line termination, Cc isolates the driver from the termination, R1-RT-R2 network provides an operating bias and also a  $\pm 30\text{mV}$  failsafe bias for the LVDS receiver.

## PECL - LVDS Interoperation

A 5V PECL driver will provide a signal with too high of an offset voltage for most LVDS receivers. In this case a passive divider can be used to provide a termination and also offset divider. The three-resistor ladder should be located close to the receiver inputs to minimize the stub length between them and the input. The first drop provides the bias point for the PECL driver at 3V, the second drop bias the inputs to the nominal LVDS offset voltage (1.25V). Standard value resistor have been used and selected such that the PECL line is terminated into 50 Ohms, and a +50mV failsafe bias is also provided for the LVDS receiver.



**Figure 7:** PECL to LVDS-R1-R2-R3 divides down the higher offset voltage of the PECL (5V) driver to levels compatible with the LVDS receiver -  $R1/(R2+R3) = 50 \text{ Ohms}$  for line termination and +50mV failsafe bias provided.

## Summing it up -

ECL, LVDS, and CML all offer high-speed capability and will coexist due to unique features they each provide. In some applications both may be employed. For example multiple LVDS lines could be used between large ASIC devices feeding a SerDes device that muxes this up into a higher speed serial CML link. This has the advantage of not burdening the core ASIC with the higher speed I/O or the power dissipation of the output. In lowering power, and minimizing crosstalk the trend to lower swings started by LVDS will continue in the years to come.

## References:

- [AN-972](#), Inter-Operation of Interface Standards, National Semiconductor, November 1994
- [AN-1123](#), Sorting Out Backplane Driver Alphabet Soup, National Semiconductor, September 2002
- [The Many Flavours of LVDS](#), National Semiconductor, September 2002
- [AN-1406](#), Designing with PECL (ECL at +5.0V), ON Semiconductor, September 1999
- [AN-1568D](#), Interfacing Between LVDS and ECL, ON Semiconductor, April 2001

## Standards -

- [ANSI/TIA/EIA-612](#), Electrical Characteristics for an Interface at Data Signaling Rates to 52 Mbit/s, Telecommunications Industry Association
- [ANSI/TIA/EIA-644-A](#), Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, Telecommunications Industry Association. February 2001
- HIPPI, High-Performance Parallel Interface, ANSI, T11, [www.hippi.org](http://www.hippi.org)

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