## MASTER TRIGGER CARD/DIGITAL

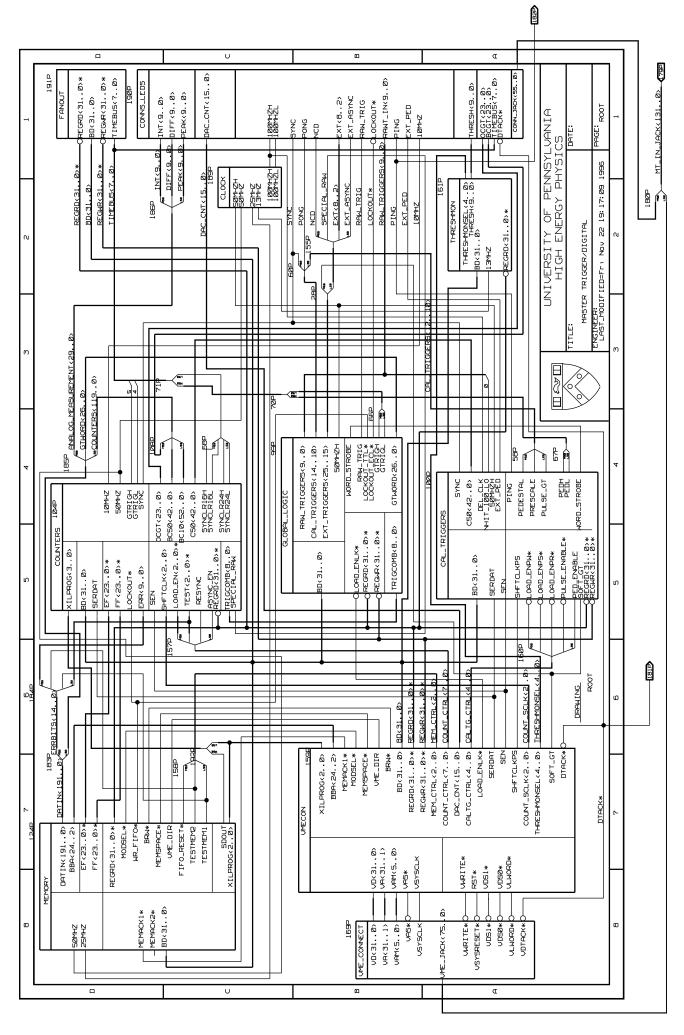
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5. MEMORY 5. B MEMSIMMS) 5. C MEMFIFO (FIFO MEMORIES) 5. C MEMFIFO (FIFO CONTROL FOR WRITING TO DRAM SIMMS) 5. C X X X X X X X X X X X X X X X X X X	6 THRESHMON (MONITOR OF TRIGGER THRESHOLDS)  7 UME_CONNECT(UME CONNECTORS)  7.B. I POWER_IN (INPUT VOLTAGES)  8.A BNC_CONNECT (RANUT, TIMEBUS, DAC CONNECTOR),  8.B DIGOUT_CONNECT (FANOUT, TIMEBUS, DAC CONNECTOR),  8.B DIGOUT_CONNECT (FANOUT, TIMEBUS, DAC CONNECTOR),  8.C THRESH_CONNECT (FANOUT, TIMEBUS, DAC CONNECTOR),  8.C THRESH_CONNECT (FANOUT, TIMEBUS, DAC CONNECTOR),  8.C THRESH_CONNECT (FANOUT OF IMMINE CLOCK)  10.A FANOUT_REG (PED AND GTRIG CRATE MASK REGISTERS),  10.B FANOUT_REG (PED AND GTRIG CRATE MASK REGISTERS),  10.B FANOUT_CONNS (FANOUT CONNECTORS),	10.C FANOUT_MASK  UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS FITLE:  ENGINEER:  A BAGE:  A 1
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F CONTENTS  AND CONTROL REGISTERS; WIFFFERE,	WE INTERFACE, WHE STALL BATH COUNTERS, GLOBAL_LOGIC, THRESHOLD MONITORING, CALIBRATION TRIGGERS, FOR SERIAL DATA, CLOCKS, FOR SERIAL DATA ADAGES, STER FOR MEMORY READ ADDRESS, STER FOR XILINX PROGRAMMING, AN COUNTER, AND COUNTER,	1 TRIGGER 5
	1.9. X XVMETRIGS (XLLINX VMETRIER FOR)  1. B CONTROL (CONTROL REGISTERS FOR COUNTERS, GLOBAL_LOGI MEMORY, THRESHOLD MONITORING, CALIBRATION TILC SERIAL (REGISTER FOR SERIAL DATA, CLOCKS)  1. C SERIAL (REGISTER FOR SERIAL DATA, CLOCKS)  1. D DAC_CONTROL (CONTROL REGISTERS FOR DACS)  1. F MEM_RDADD (REGISTER FOR MEMORY READ ADDRESS)  1. F MEM_RDADD (REGISTER FOR MEMORY READ ADDRESS)  1. F XILPROG_REG (REGISTER FOR XILINX PROGRAMMING)  2. A COUNTERS  2. C COUNTER (GLOBAL TRIGGER COUNTER)  2. C COUNTS (GLOBAL TRIGGER COUNTER)  3. A GTWORD (GLOBAL TRIGGER MASK AND WORD)  3. B GTGEN (GENERATION OF GLOBAL TRIGGER)  3. B GTGEN (GENERATION OF GLOBAL TRIGGER)  3. B GTGEN (GENERATION OF GLOBAL TRIGGER)	GENERATOR) DELAY THE OF LOW N
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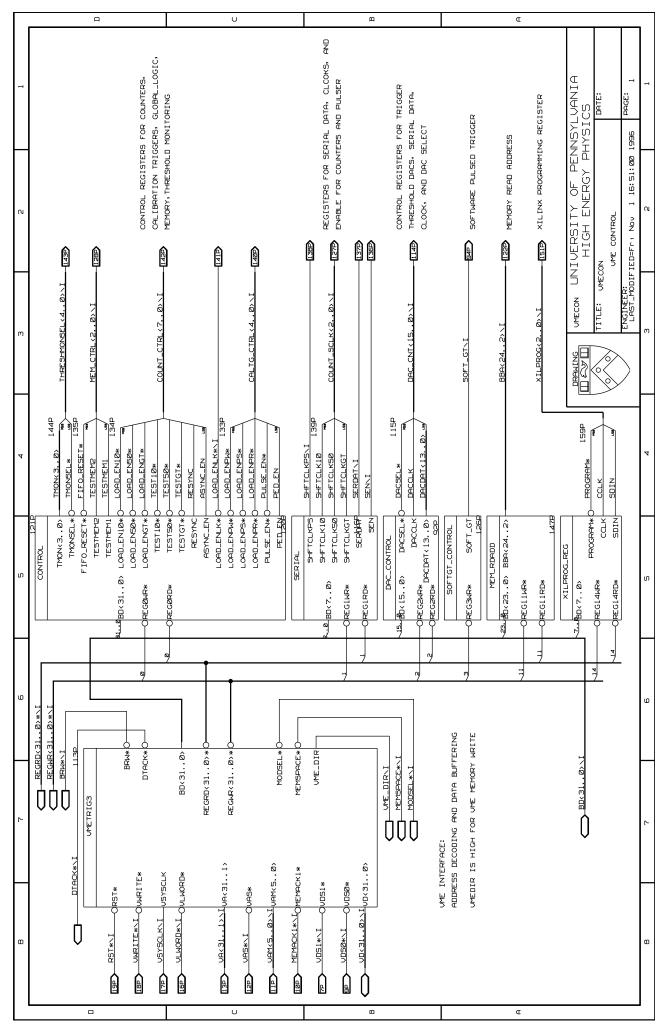
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	REGISTER		REGISTER		
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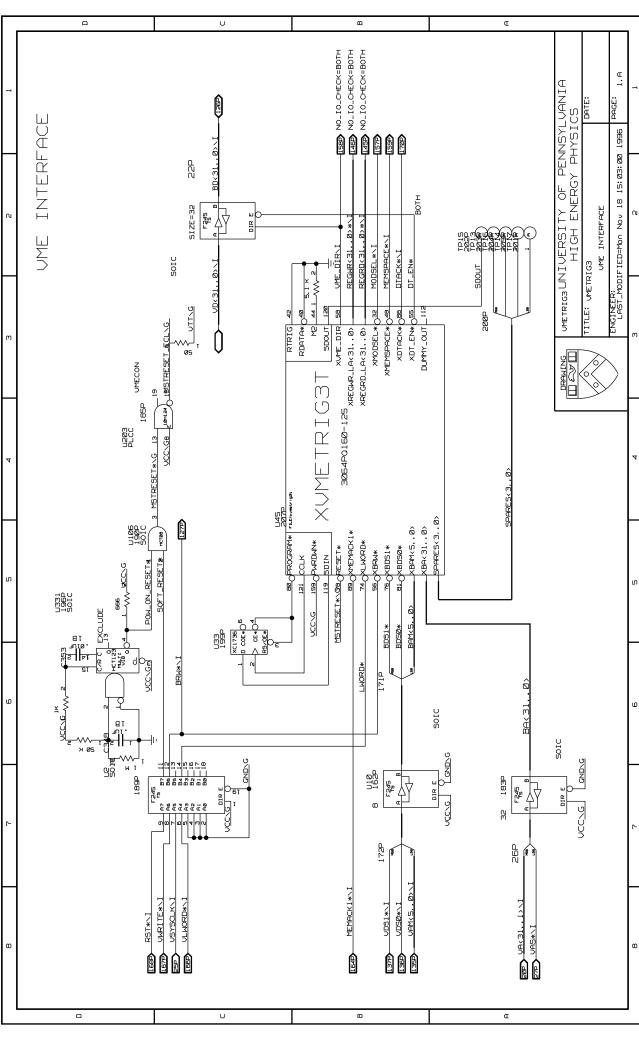
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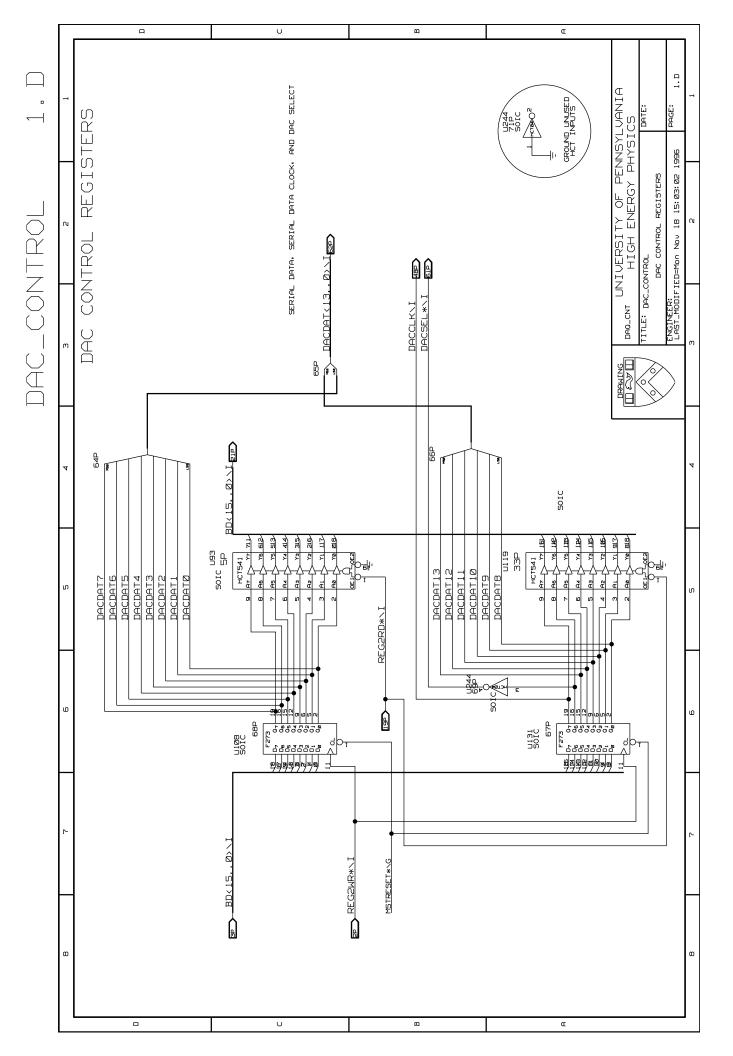
MASTER TRIGGER CARD/DIGITAL







CONTROL 1. B

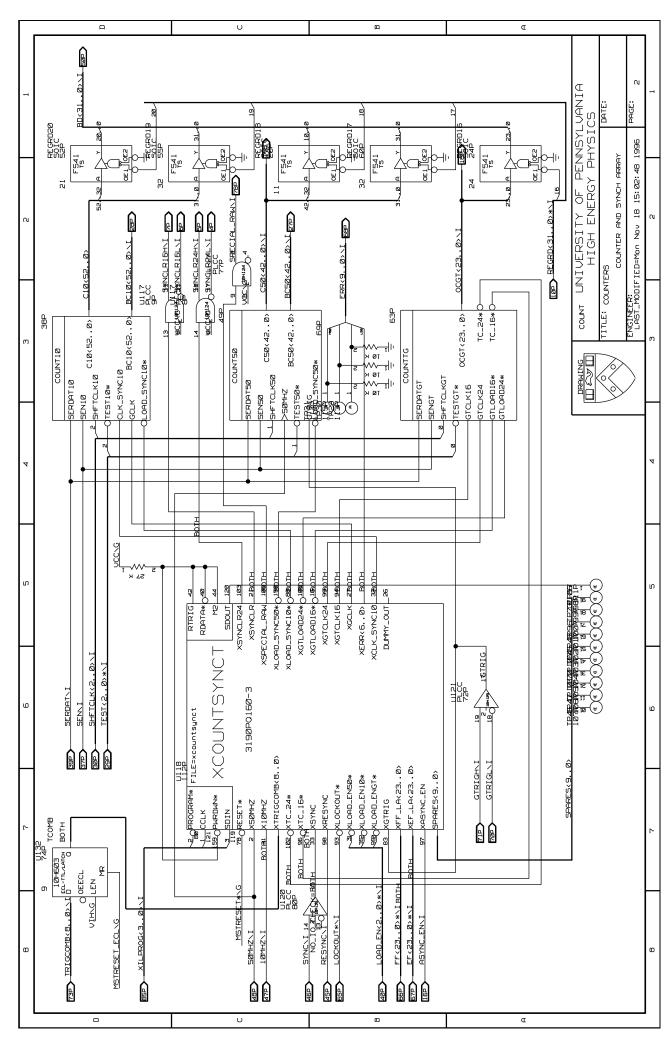


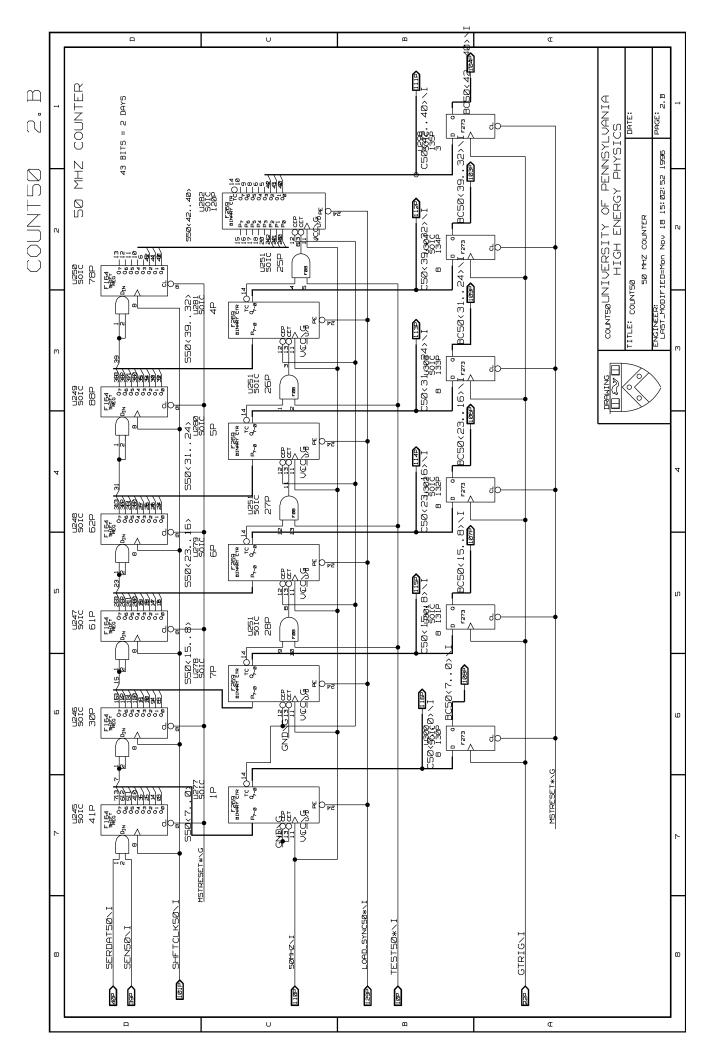
SOFTGT\_CONTROL 1. E

П U ш Φ REGISTER ₽.; UNIVERSITY OF PENNSYLUANIA MEM\_RDADD HIGH ENERGY PHYSICS NGINEER: LAST\_MODIFIED=Mon Nov 18 15:03:08 1996 MEMORY READ ADDRESS REGISTER ADDRESS 83P 201C 73PC HCT541 MEM\_RDADD READ 85P MEMORY U54 SOIC 65P 244 SOIC SP USS SOIC 33P HCT541 HCT541 86P 87P ω ω REG11RD\*/I 52P 199 REGIIMR\*/I MSTRESET\*\G ω  $\Box$ U ш Φ

MEM\_RUPDU 1. F

XILPROG\_REG



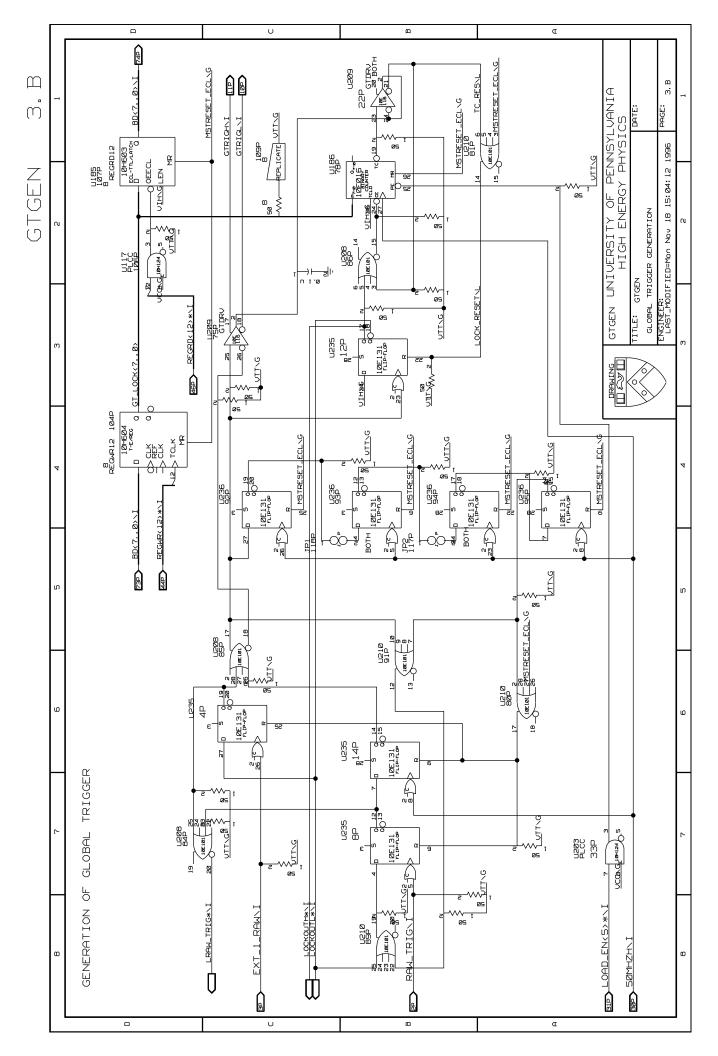


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GTWORD 3. A



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PULSER3 4. A

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4. B

ENGINEER: LAST\_MODIFIED=Mon Nov 18 15:02:46 1996

PULSE DELAY/PEDESTAL GENERATOR

DELPUL2

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10H604 1-E/REG

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REGRD4

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UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS

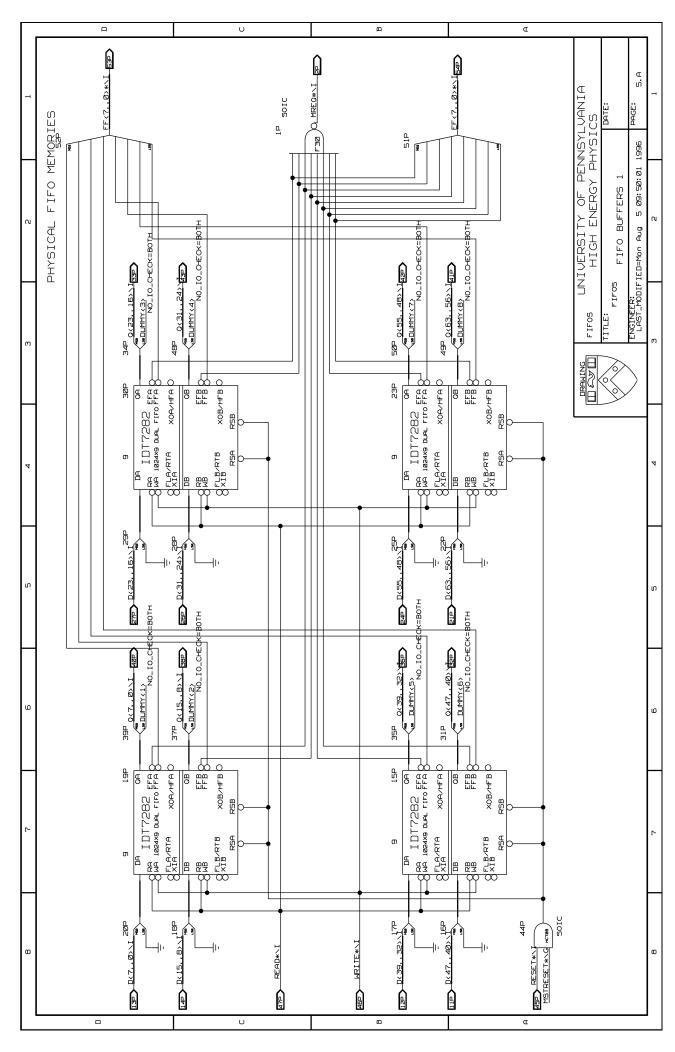
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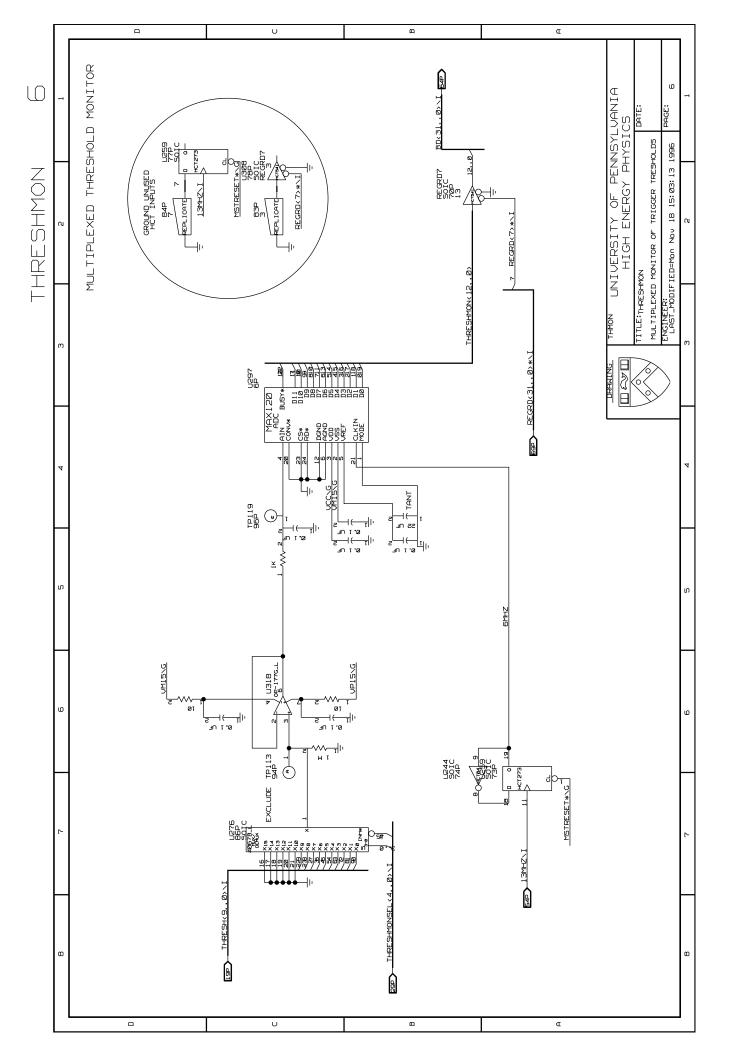
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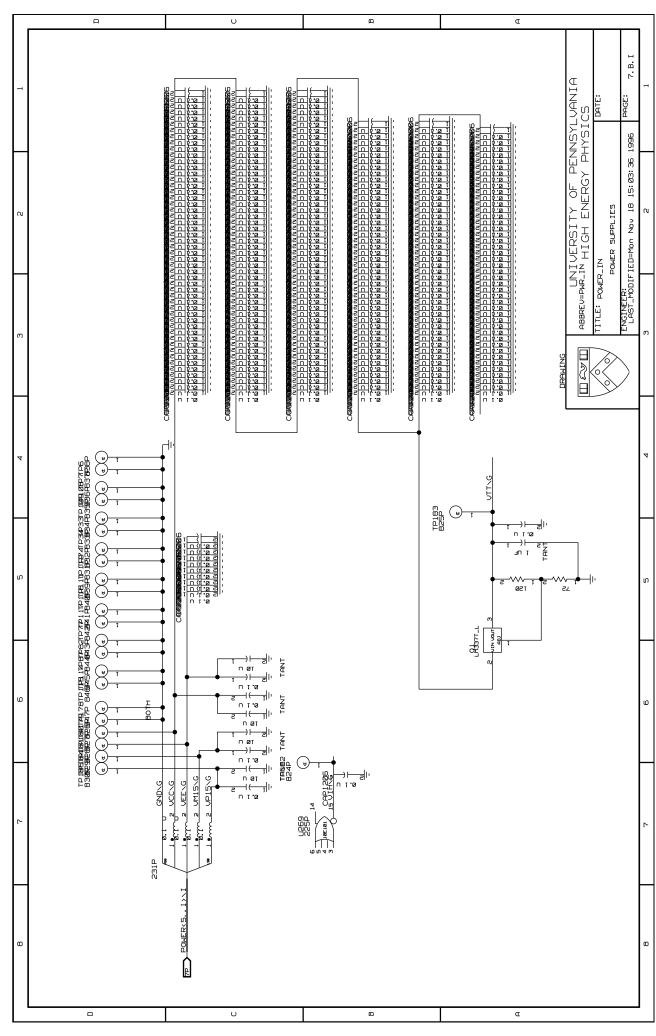
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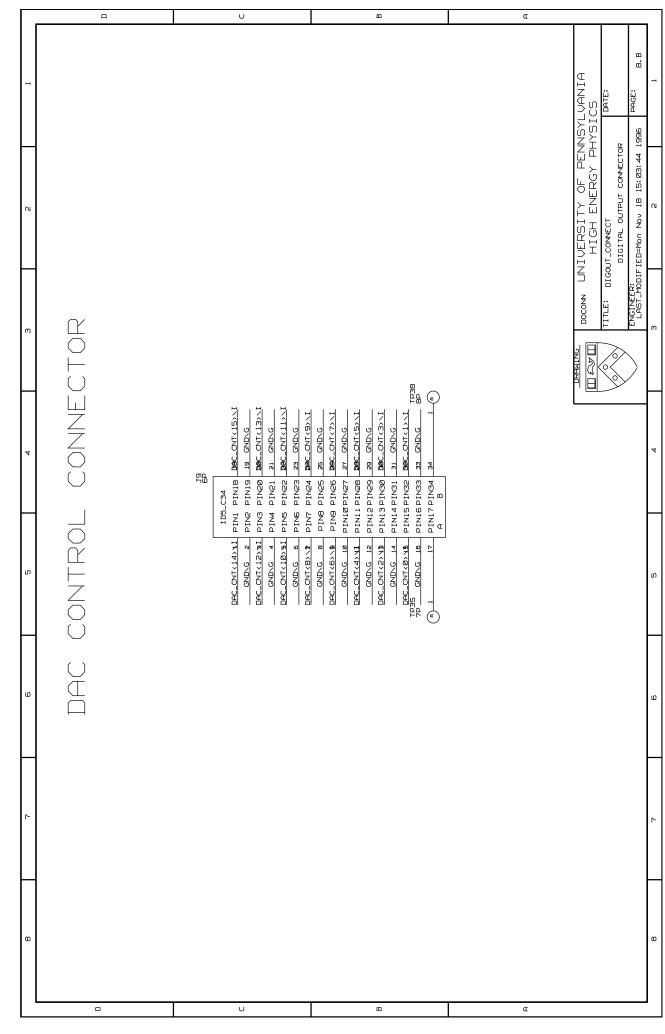




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	υ 		ULMORD#\1 UDS@#\1 UDS1#\1 USYSKESTT#\1 USYSCLK\1 USYSCLK\1	URKS. 8>1	POWER.5.1> POWER.5	



ω CONNLED UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS ENGINEER: LAST\_MODIFIED=Mon Nov 18 15:03:42 1996 CONNECTORS AND LEDS CONNS\_LEDS CONN\_JACK<55..0>\I BCGT<23..Ø>\I BCGT < 23.. Ø> CGT < 23.. Ø> JTACK\* ONG YNC. DIFF<9..0>\I IBED TIMEBUS<7..Ø>\I EXT\_ASYNC\I INT<9..0>\I LOCKOUT\*\I ZEIP OCGT<23..Ø>\I EXT\_PED\I PONG PING\I NCDVI 10MHZNIP Ú Ú Û (O U  $\Box$ U ш Φ



FANOUT\_REG

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9		10S_C10   581G_c20>1   10S_C10   581G_c20>1   10S_C10   581G_c20>1   10S_C10   10S_C	-C10 PIN6 GBGGCC33NI PIN7 PEDI-C23NI PIN9 B'BYCLRLC23NI PIN10 B'BYCLRLC23NI		SPARE FANOUT CONNECTORS	۵
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FANOUT\_MASK 10. C