TUBii Proposal

ver 3.8

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Contents

1 Requirements: aka Designer's Paradise

In roughly priority order:

1. Communication with the CAEN board

   - GT: ECL to NIM conversion to trigger the CAEN board
   - SYNC and SYNC24: ECL to LVDS conversion to flag bits in the CAEN header for synchronisation with PMT bundled events
   - External Trig: NIM to ECL conversion for synchronisation

2. Delayed GT

   For the MTCA+.

   → One 8-bit register to program the delay counter.

3. Generic programmable delays

   - Synchronous
   - Semi-asynchronous i.e. using a higher rate clock

- Truly asynchronous

→ One 8-bit register per delay to program delay counter.

?? How many delays?

?? What range of ΔT?

4. Ext Trig fan-in

   - Fan in of additional external trigger signals to a single spigot on the MTCD
   - Latching of new external triggers in sync with MTCD
   - Programmable trigger mask for new ext triggers
   - Fan in of external async triggers (EXTASY+)

5. Clock options

   - External input of TUB clock
   - New clock: 200MHz LVPECL
   - OR of above:
     Default: new clock
     Switch in TUB clock if:
     - n clock ticks missed
     - manually
     - ORCA controlled
   - LED to ID clock
   - Bit stored in register (written to datastream?) to identify clock

   → One 8-bit register to program counter for controlling clock switch-over.

6. Communication with ELLIE

   - Synchronous pulse generation to drive ELLIE: 1 HZ — 10 kHz
   - Return pulse delay ∼600 ns

   → Three 8-bit registers for pulse generation.

   → One 8-bit register for delay.

7. ECAL set-up AND of GT with a control signal, fed back into the ExtPed (with a fan-in to allow something else to be connected?)

8. Translations

   - ECL to TTL
   - TTL to ECL

- ECL to NIM
- NIM to ECL
- ECL to LVDS
- LVDS to ECL
- Other?

9. Additional trigger options

   - Prescale trigger
   - Burst trigger
   - Sychronous trigger ("TUBii GT")

10. Pulse generation

    - Synchronous
    - Semi-asynchronous (higher rate clock)
    - Truly asynchronous

    → Three 8-bit registers for synchronous pulse generation (per instance).

    → One 8-bit register for semi-async / truly async delay to sync pulses (per instance).

    ?? How many instances?

    ?? Do semi/truly-async by generating sync pulses and delaying them..?

11. Tunable retriggerable discriminator circuit

    - Trigger using DIY ECL one-shot (F/F + RC delay a-la-Klein)
    - Maximise dynamic range (V)
    - Minimise time delay (ns)
    - Retriggerable: on DGT AND LO*
    - Allow for neg- and pos-going pulses – use differential comparator output → 2 circuits

    2 options:

    (a) $[-3.3, +5]$ V range ; 2.5 ns delay on comparator (6.5 ns total)
    (b) $[-2.0, +3]$ V range ; 250 ps delay on comparator (4.25 ns total)

12. Pulse Inverter

13. Pulse Scaler

14. Speaker Equivalent to TUB plus

    - option to listen to individual triggers

- listen to analogue trig sum??
- prescale
- audio filter

15. LEDs Pretty colours
16. Gated charge run set-up
17. Powers: -5.2V, -2V, +3.3V, +5V
18. Ribbon cable delay
19. ML403...

2 ML403

2.1 Minimal requirements

Ethernet communication with ORCA a la XL3, allowing remote control of TUBii settings, which requires:

- Data bus on TUBii
- Registers to hold info
- input- and output-enable lines to load/read registers

2.2 Preferred Capabilities

Inclusion of TUBii info in datastream, which requires:

- GT counter on ML403 to keep events in sync
- Redundancy check on event count..?? Ideas:
  - SYNC and SYNC24 already come onto TUBii: check every 2^{16} and 2^{24} event
  - ??

2.2.1 ML403 Processing Requirements

1. GT counting to mimic CMOS chips (including missed GTs etc)
2. Ext trigger processing
   - Apply trigger mask to external trigger signals
   - Generate raw trig (if required)
   - latch ext trig signals on receipt of LatchedRawTrig signal
   - *Is this fast enough using direct i/o, or does it need to be discretes?*

3. Prescale triggers
    - Generate output raw trig for every n^{th} input raw trig
4. Burst triggers
    - Generate output raw trigs for each input raw trig during a fixed window of T ns (equiv to N clock ticks)
5. ECAL
    - AND of GT with control signal
6. Additional programmable delays
    - Generate output pulse m clock ticks after input pulse (sync to TUBii clock?)
7. Combined Trigger Logic
    - Option to generate raw trigs on specified combination of other trigger signals?
8. MTCA+ threshold monitoring
    - Not sure how we do this yet...

2.2.2 Info to be included in datastream

1. GT count
2. Ext Trig signals
    - Mask for new ext trigger signals
    - TUBii trigger word (of ext trig signals)
3. Prescale triggers
    - Prescale factor per trigger
4. Burst triggers
    - Burst length
    - Burst frequency
5. Additional programmable delays
    - Delay period
6. Clock ID bit

2.3 Dream-like Ambitions

- LCD screen displaying funky stuff (GT count, captain neutrino, ext trig word...)

2.4 ML403 I/O Pin Count

32 pins will be used as bus I/O, with registers to set counters etc. This will be used for anything that only needs to be set once per run, or is not time critical.
Individual pins will be used for anything that needs to be synchronous with the clock, or needs to be prompt *i.e.* we don't want the additional delay of a register.

Purpose	**I/O**	**Pins**
GT	I	1
Ext trig signals	I	16
Latched raw trig	I	1
Ext raw trig	O	1
Trigger signals for prescale	I	4
Prescaled triggers	O	4
Trigger signals for burst	I	4
Same inputs as prescale trigs?		
Bursted triggers	O	4
Same outputs as prescale?		
ECAL validation signal	O	1
Trigger signals for combination	I	4
Same as prescale / burst inputs?		
Combo raw trig	O	1
Delayable pulse	I	2
Delayed pulse	O	2
TUBii clock?	I	2
Do we need any for th monitoring?		
Registers / Data bus	IO	32
Inc all counter settings etc		
Addresses	O	4
Total		**83+**

3 Front Panel

- Connector translations (BNC, SMB, LEMO)
- Cable delay
- All necessary I/O for everything mentioned above (that's a lot - I haven't made the full list yet, since it keeps expanding, but suffice to say TUBii won't be losing weight anytime soon).
- ...

- Infinite other stuff.