Termination Schemes and Design Guidelines for 3.3V LVPECL Driver

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Introduction

With the demand for higher clock and data rates, single-ended signals have begun to reach their limitation. As a result, designers are forced to seek alternative routes. This demand for higher speed has shifted the industry from single-ended signaling to differential signaling. In general, differential signals offer a compelling alternative to single-ended signals. Differential signals offer higher speed, better noise rejection, lower EMI, and much lower power consumption over single-ended signals.

But as differential signals prevail over single-ended signals at high-speed, they do require special termination in order to realize the benefits of differential signals. A proper termination scheme is required to ensure proper signal integrity and functionality of the device.

This application note will provide the termination schemes for 3.3V LVPECL drivers. There are multiple termination schemes for LVPECL; however, this application note will only focus on the more commonly used DC coupling and AC coupling schemes. It should be noted that these recommendations are not fixed, but can vary depending on the system's requirements. The application note will also provide some design recommendations to obtain optimal performance for LVPECL devices.

DC Termination

The standard 3.3V LVPECL termination is shown in Figure 1. This termination scheme is mainly used in characterization test since it is not easily implemented in system designs. The problem with the standard termination approach is that it would require an additional power supply of VCC- 2V = 1.3V, which can complicates system design.

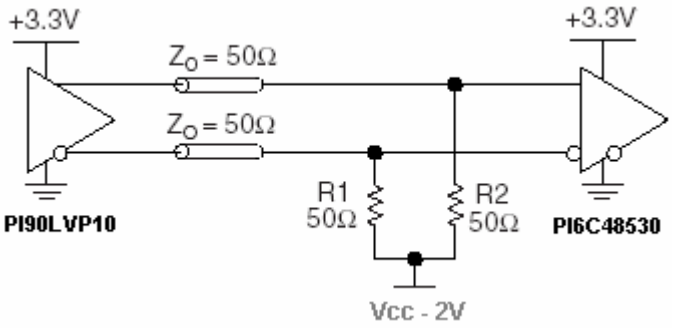

Figure 1. Standard LVPECL Termination Scheme

A more simplified approach, which eliminates the need of an additional 1.3V power supply is shown in Figure 2. The circuit shown in Figure 2 is a widely used termination scheme for 3.3V LVPECL drivers. Another common approach is shown in Figure 3. The 3-resistors termination scheme is slightly better in terms power saving while reducing one extra component compared to a 4-resistors termination. It should be noted that the termination resistors should be placed as close as possible to the receiver when using the 4-resistor or 3-resistors termination schemes as shown in Figure 2 and Figure 3 respectively.

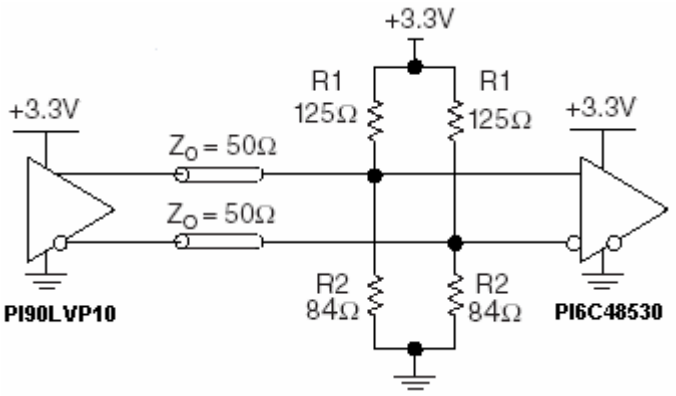

Figure 2. Most Commonly used termination scheme for 3.3V LVPECL

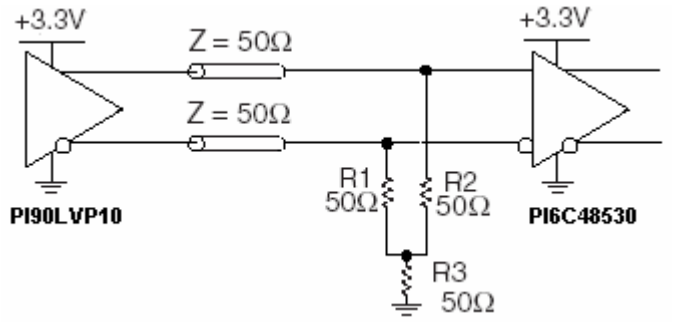

Figure 3. Equivalent 3.3V LVPECL Termination

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AC Termination

In certain applications where interconnections between different layers are needed, AC coupling is implemented. The purpose of AC coupling is to change the common-mode voltage level by adding a series capacitor. The capacitor in AC coupling will remove the DC component of the signal, which is the common-mode voltage while retaining the AC component, which is the voltage swing. In high-speed applications, AC-coupling is only recommended for DC-balanced signals such as 50% duty cycle clock, Manchester-coded data, and 8B/10B encoded data. Figure 4 and Figure 5 provide two types of AC-coupling termination scheme with a 1.3V and 2V common-mode, respectively. The resistors R1 are placed before the transmission line and should be placed as close as possible to the driver. Since AC-coupling no longer provides a DC path, the resistors R1 are required to provide a DC part for the falling edges. Resistors R2 and R3 are after the transmission line and should be placed as close as possible to the receivers.

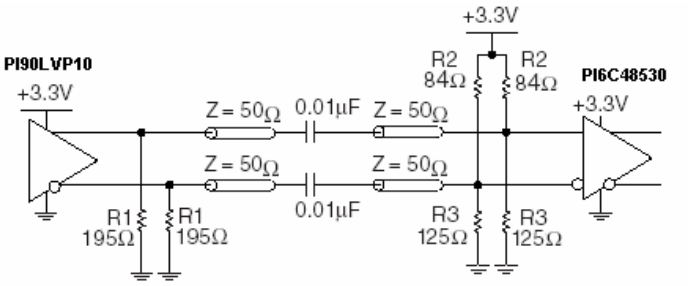

Figure 4. AC coupled with bias offset at VCC – 1.3V

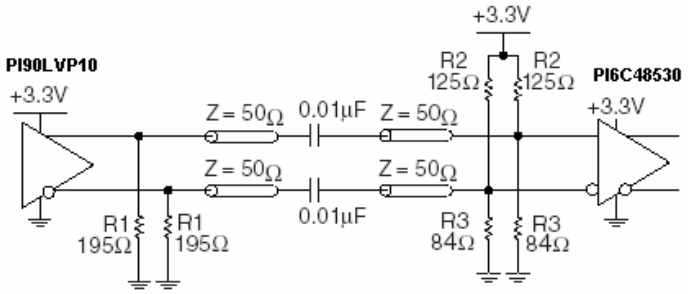

Figure 5. AC coupled with bias offset at VCC –2V

Design Note

As with any design, some basic steps should be taken into consideration to gain the best performance from a device. The following recommendations below will provide a few design guidelines. Note that the suggestions can vary depending on the application.

Recommendations

1. A 0.47µF and a 0.01µF decoupling capacitors should be used between all VCC and GND pins of the device. Placement of decoupling capacitors should be as close as possible to the VCC pin of the device.
2. In addition to the 0.47µF and a 0.01µF, there should also be sufficient amount of decoupling capacitors distributed throughout the main power supply.
3. Selection of resistor values should be taken into account for noise-related issues and power consumption issues.
4. Resistors after the transmission line should be placed as closed as possible to the receiver. Resistors before the transmission line should be placed as closes as possible to the driver.
5. Use controlled impedance traces with proper termination to match the trace impedance.
6. Minimized trace length to be as short as possible. Have equal differential trace lengths to avoid skew differences between the two differential signals.
7. To minimized reflections and maintain the receiver's common-mode noise rejection, differential traces should run as close as possible after leaving the device.
8. Avoid looping the signals if possible. If serpentine technique is required to provide equal trace length, use arcs or 45° turns rather than 90° turns to avoid impedance discontinuities.
9. Use minimal vias to avoid impedance discontinuity, which may introduce more skews and reflections.
10. Keep high-speed buses and logic signals away from the clock device to prevent noise from coupling onto the clock signals.
11. If working with both single-ended and differential signals, isolate the differential signals from single-ended signals by using different planes separated by the power and ground planes.
12. Placement of the clock device should be at the center of all other components so that the clock signal traces are kept to a minimum.
13. Use solid VCC and GND planes.

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