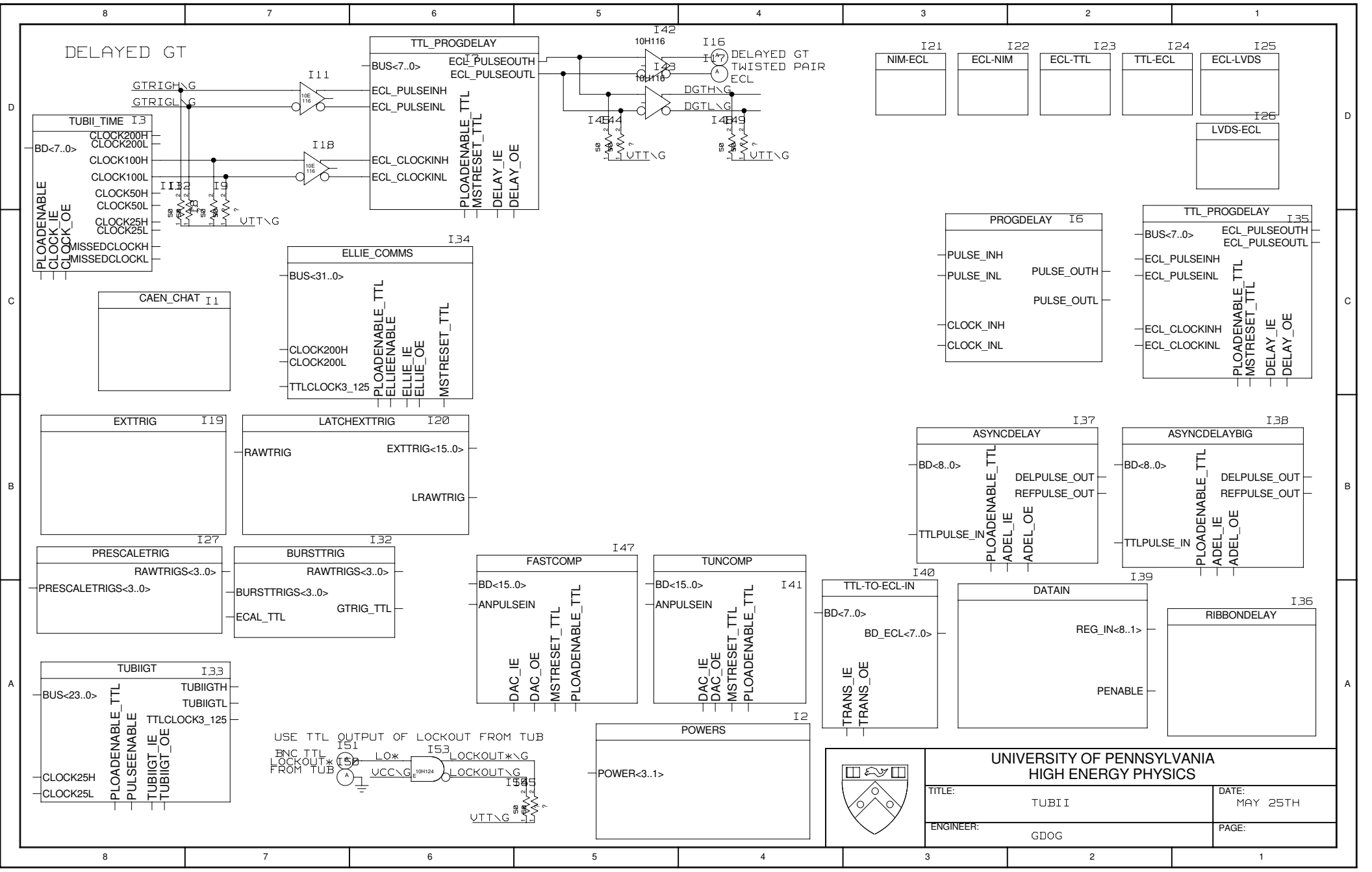
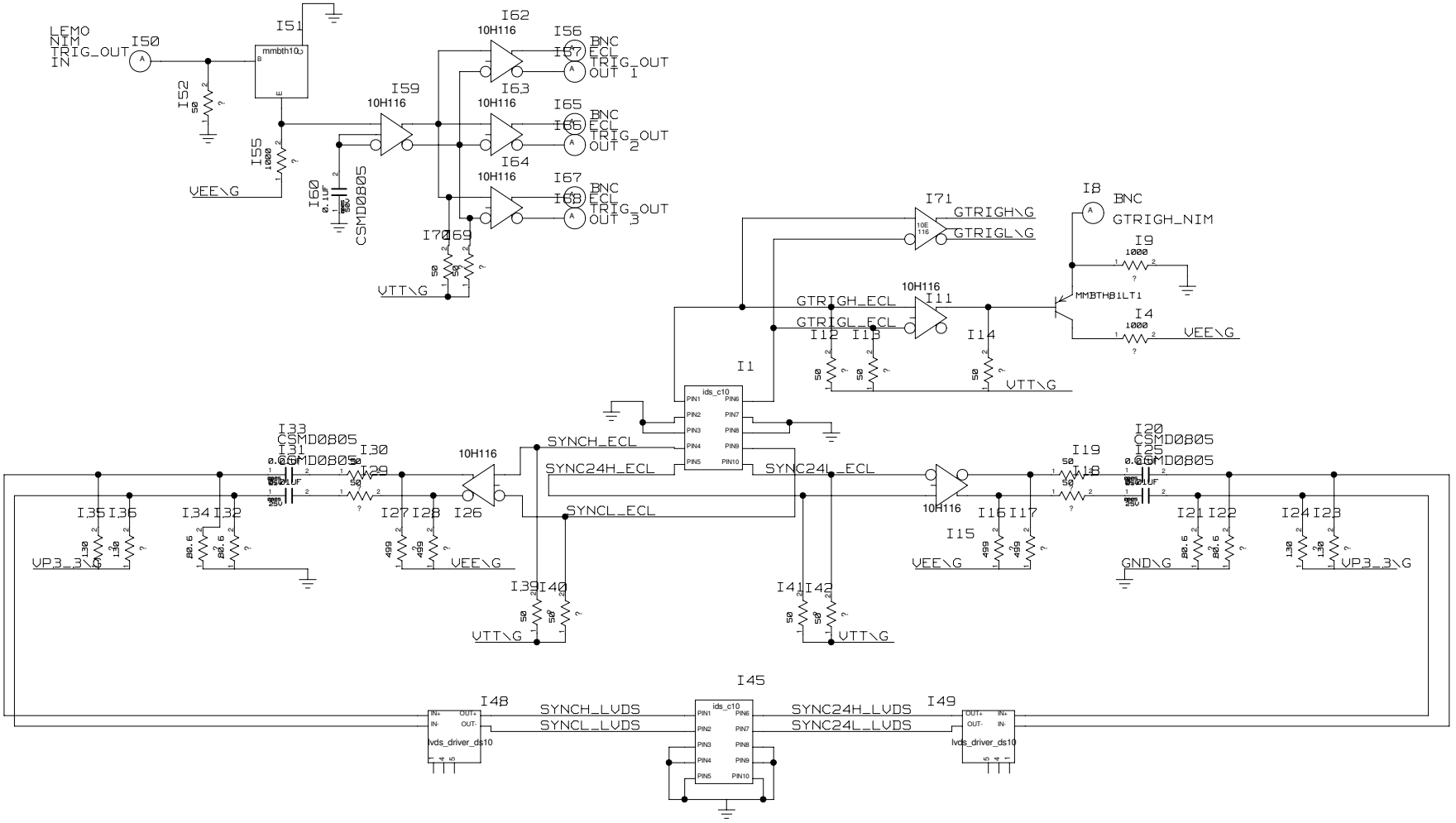
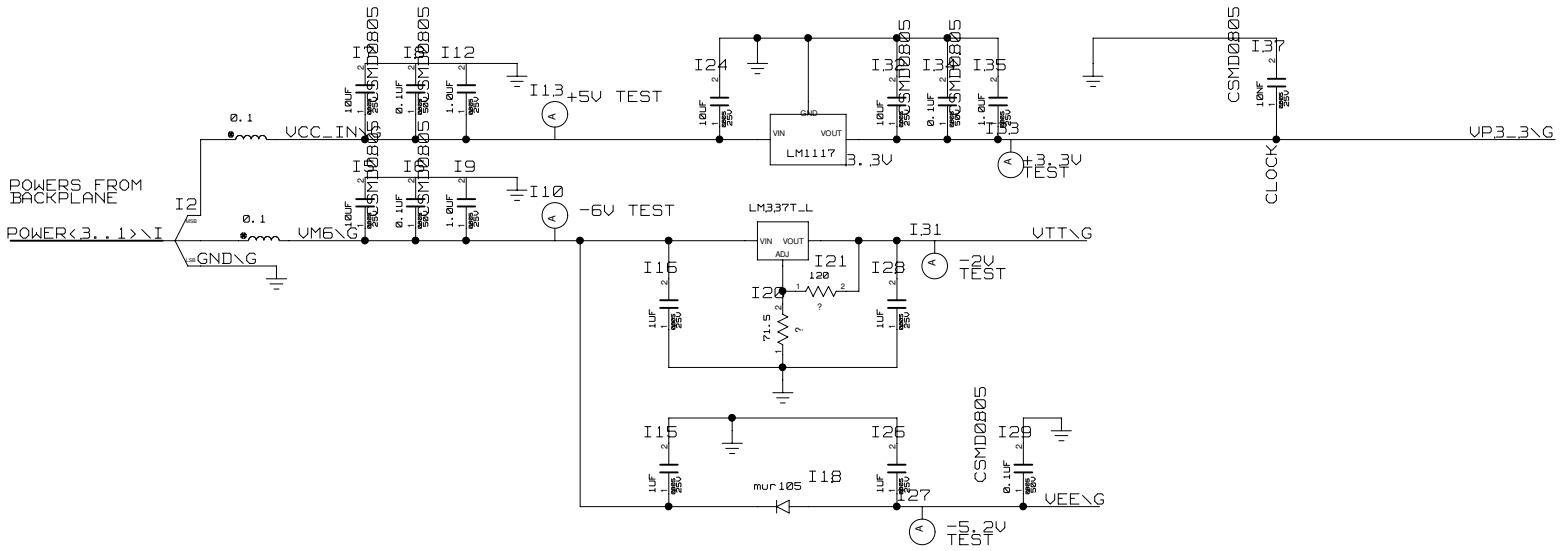

DELAYED GT
TTL_PROGDELAY
BUS<7..0>
ECL_PULSEOUTH
ECL_PULSEOUTL
ECL_PULSEINH
ECL_PULSEINL
ECL_CLOCKINH
ECL_CLOCKINL
PLOADENABLE_TTL
MSTRESET_TTL
DELAY_IE
DELAY_OE
I42
10H116
I16
DELAYED GT TWISTED PAIR
ECL
I43
DGTH\G
DGTL\G
I44
I45
VTT\G
GTRIGH\G
GTRIGL\G
I11
I18
I12
I13
I9
I10
TUBII_TIME I3
CLOCK200H
CLOCK200L
CLOCK100H
CLOCK100L
CLOCK50H
CLOCK50L
CLOCK25H
CLOCK25L
MISSEDCLOCKH
MISSEDCLOCKL
PLOADENABLE
CLOCK_IE
CLOCK_OE
I21
NIM-ECL
I22
ECL-NIM
I23
ECL-TTL
I24
TTL-ECL
I25
ECL-LVDS
I26
LVDS-ECL
CAEN_CHAT I1
ELLIE_COMMS I34
BUS<31..0>
CLOCK200H
CLOCK200L
TTLCLOCK3_125
PLOADENABLE_TTL
ELLIEENABLE
ELLIE_IE
ELLIE_OE
MSTRESET_TTL
PROGDELAY I6
PULSE_INH
PULSE_INL
PULSE_OUTH
PULSE_OUTL
CLOCK_INH
CLOCK_INL
TTL_PROGDELAY I35
EXTTRIG I19
LATCHEXTTRIG I20
RAWTRIG
EXTTRIG<15..0>
LRAWTRIG
ASYNCDELAY I37
BD<8..0>
DELPULSE_OUT
REFPULSE_OUT
TTLPULSE_IN
ADEL_IE
ADEL_OE
ASYNCDELAYBIG I38
PRESCALETRIG I27
RAWTRIGS<3..0>
PRESCALETRIGS<3..0>
BURSTTRIG I32
BURSTTRIGS<3..0>
GTRIG_TTL
ECAL_TTL
FASTCOMP I47
BD<15..0>
ANPULSEIN
DAC_IE
DAC_OE
TUNCOMP I41
TTL-TO-ECL-IN I40
BD<7..0>
BD_ECL<7..0>
TRANS_IE
TRANS_OE
DATAIN I39
REG_IN<8..1>
PENABLE
RIBBONDELAY I36
TUBIIGT I33
BUS<23..0>
TUBIIGTH
TUBIIGTL
TTLCLOCK3_125
PULSEENABLE
TUBIIGT_IE
TUBIIGT_OE
CLOCK25H
CLOCK25L
USE TTL OUTPUT OF LOCKOUT FROM TUB
BNC TTL LOCKOUT* FROM TUB
I51
I50
LO*
I53
LOCKOUT*\G
VCC\G
LOCKOUT\G
I54
I55
POWERS I2
POWER<3..1>
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
TITLE:
TUBII
DATE:
MAY 25TH
ENGINEER:
GDOG
PAGE:

CAEN CONVERSATIONS

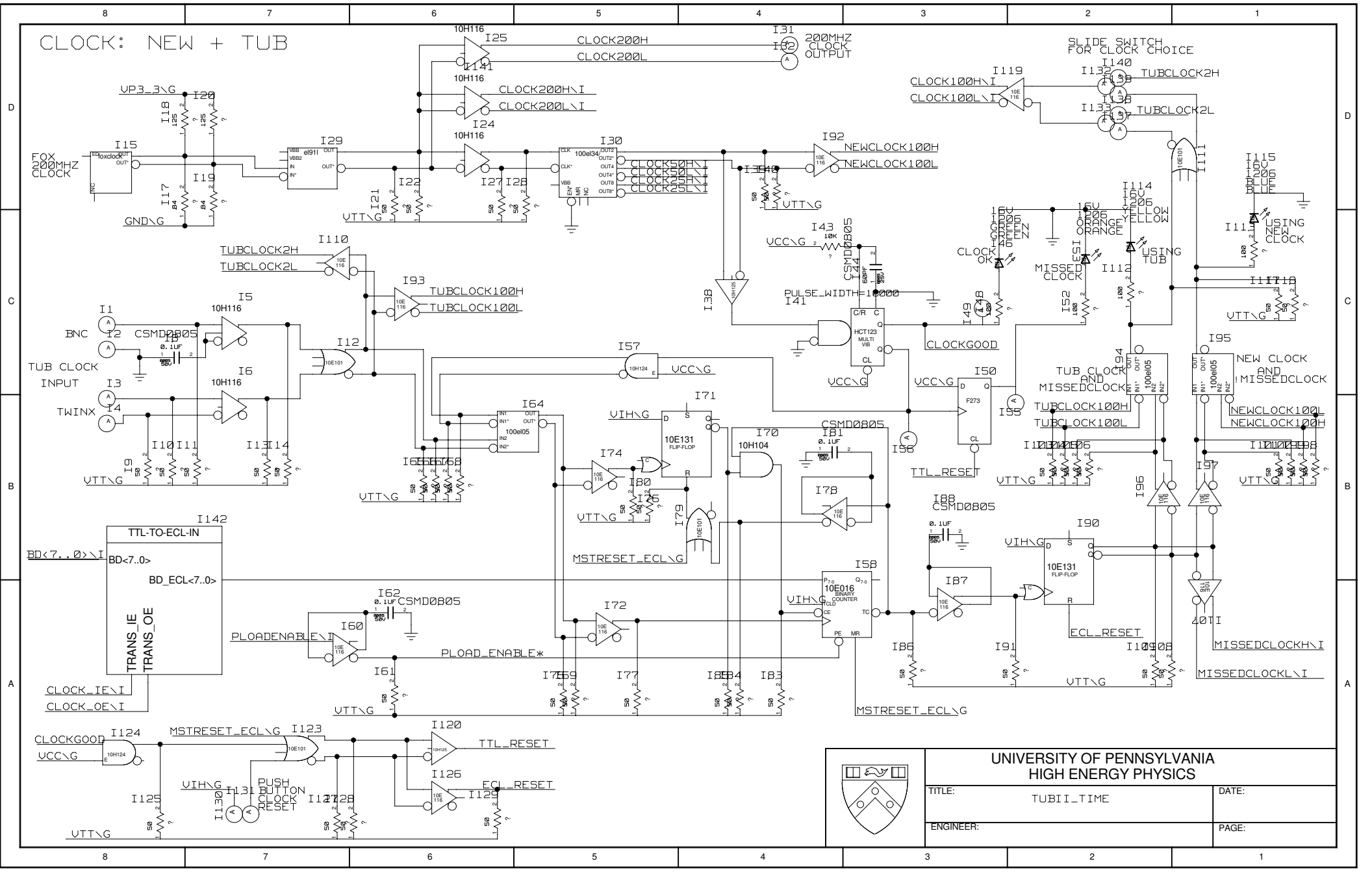


UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE:	DATE:
ENGINEER:	PAGE:

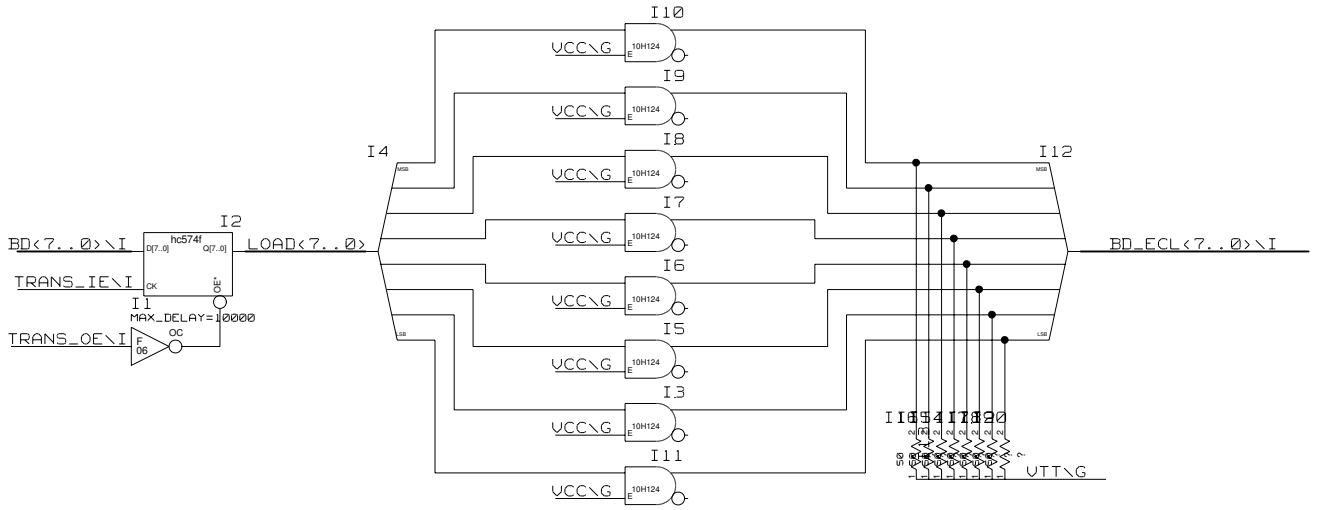


UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

TITLE:	DATE:
ENGINEER:	PAGE:

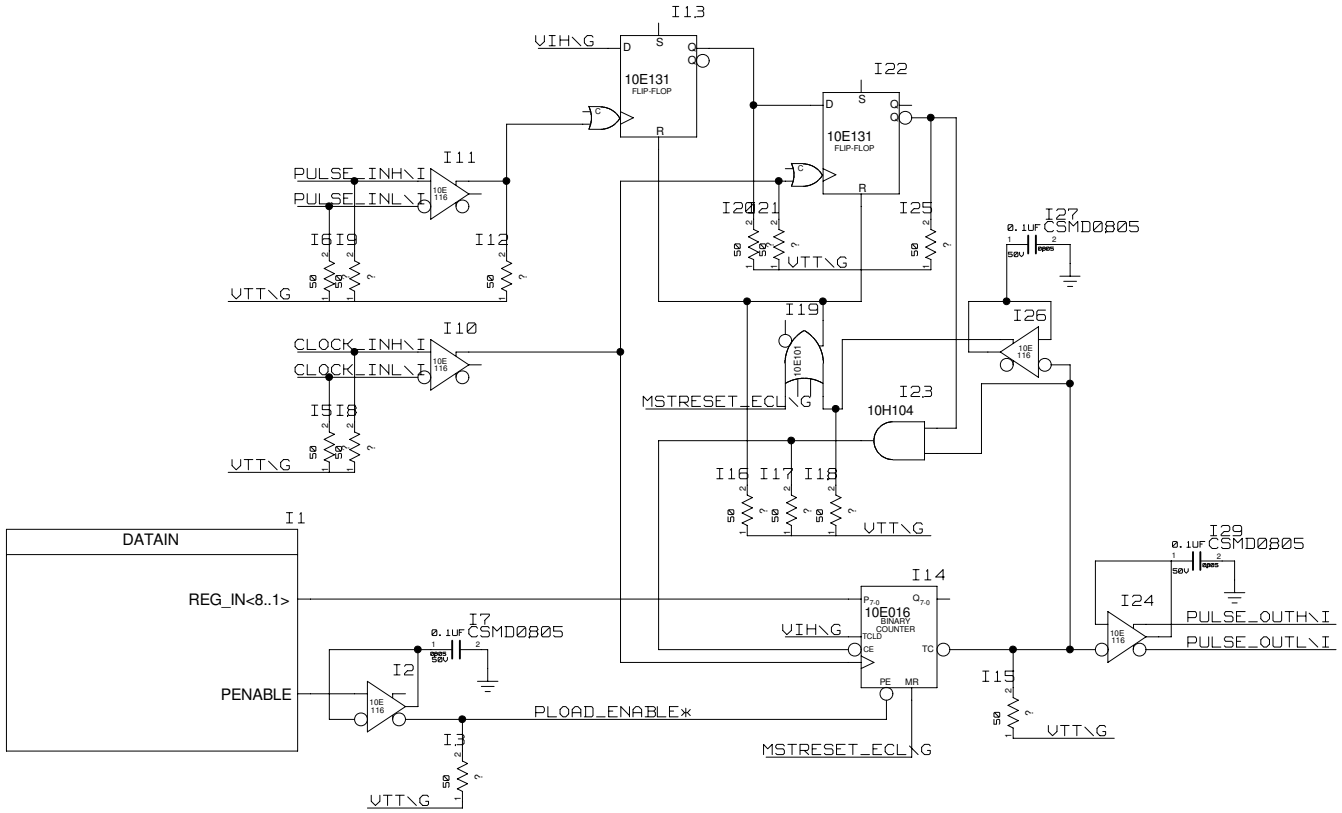

CLOCK: NEW + TUB
FOX 200MHZ CLOCK
CLOCK200H
CLOCK200L
200MHZ CLOCK OUTPUT
SLIDE SWITCH FOR CLOCK CHOICE
TUBCLOCK2H
TUBCLOCK2L
TUBCLOCK100H
TUBCLOCK100L
NEWCLOCK100H
NEWCLOCK100L
CLOCK50H\I
CLOCK50L\I
CLOCK25H\I
CLOCK25L\I
CLOCKGOOD
PULSE_WIDTH=10000
CLOCK OK
MISSED CLOCK
USING TUB
USING NEW CLOCK
TUB CLOCK AND MISSEDCLOCK
NEW CLOCK AND MISSEDCLOCK
MISSEDCLOCKH\I
MISSEDCLOCKL\I
BNC
TUB CLOCK INPUT
TWINX
TTL_RESET
ECL_RESET
MSTRESET_ECL\G
PLOADENABLE\I
PLOAD_ENABLE*
BD<7..0>\I
BD<7..0>
BD_ECL<7..0>
TRANS_IE
TRANS_OE
CLOCK_IE\I
CLOCK_OE\I
PUSH BUTTON CLOCK RESET
TTL-TO-ECL-IN
10H116
10E131 FLIP-FLOP
10E016 BINARY COUNTER
HCT123 MULTI VIB
F273
100el05
CSMD0805
VTT\G
VCC\G
VIH\G
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
TITLE: TUBII_TIME
DATE:
ENGINEER:
PAGE:

TTL CONTROL OF 8-BIT ECL INPUTS



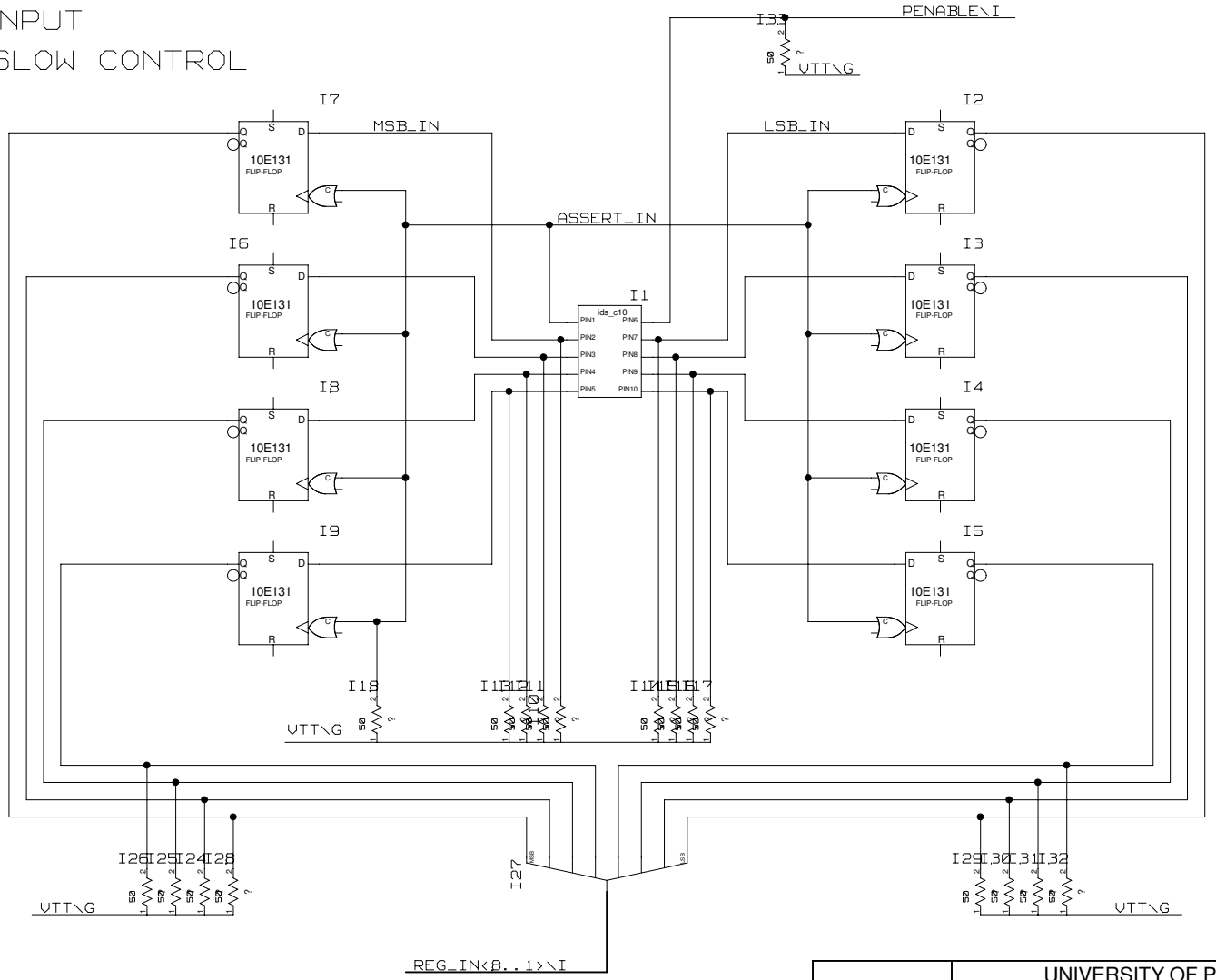
UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS		
TITLE: TTL TO ECL DATA INPUT		DATE:
ENGINEER:		PAGE:

GENERIC PROGRAMMABLE DELAY

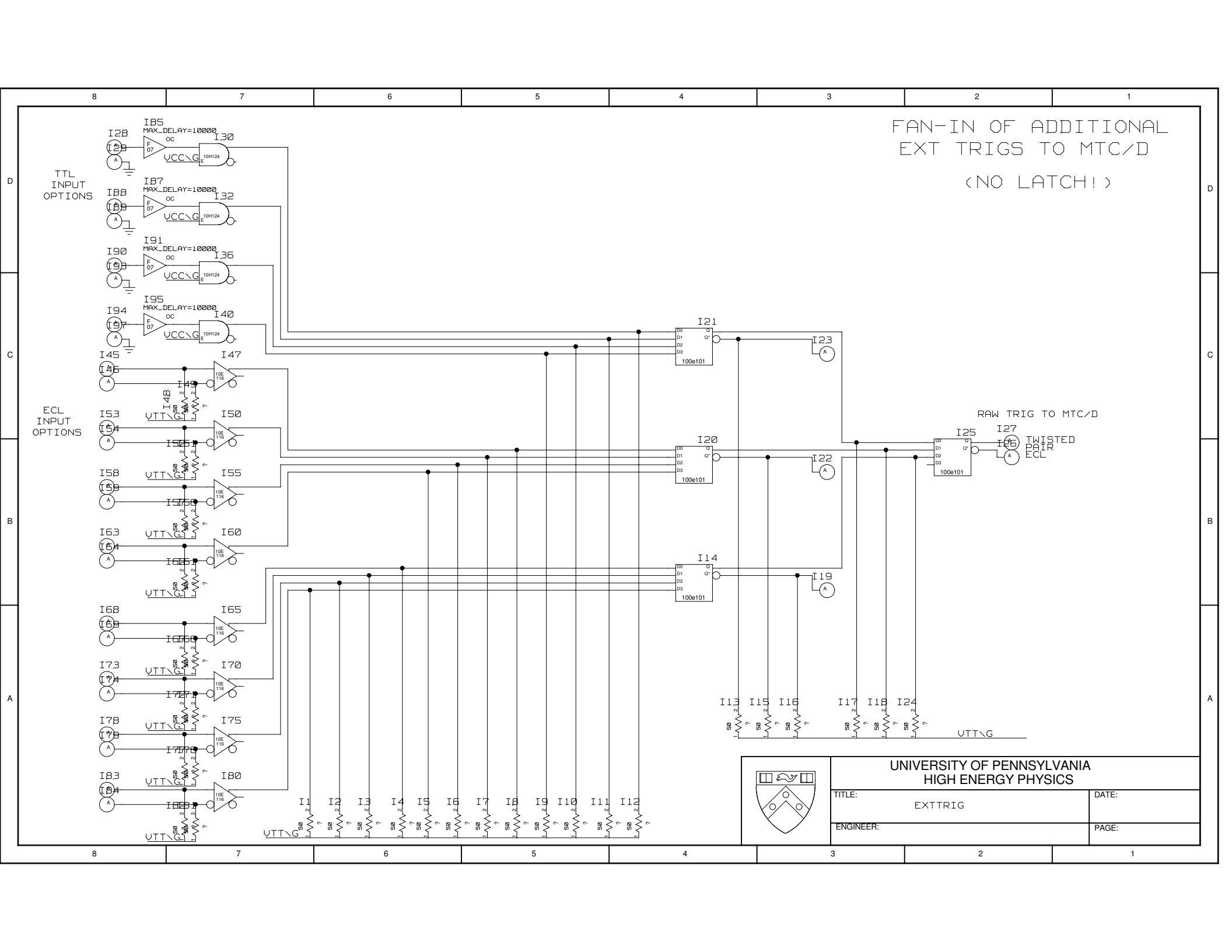


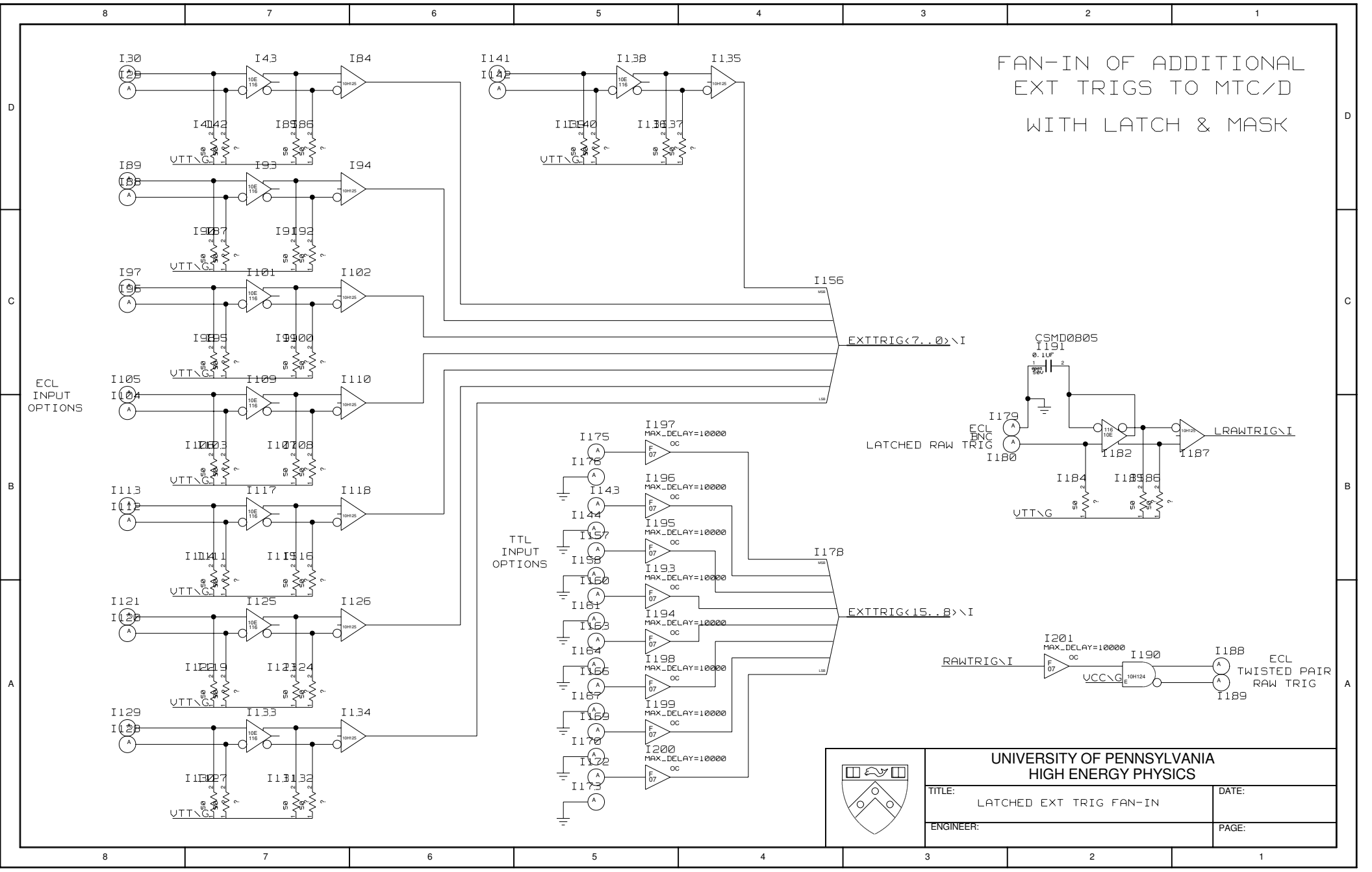
UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: PROGDELAY	DATE:
ENGINEER:	PAGE:

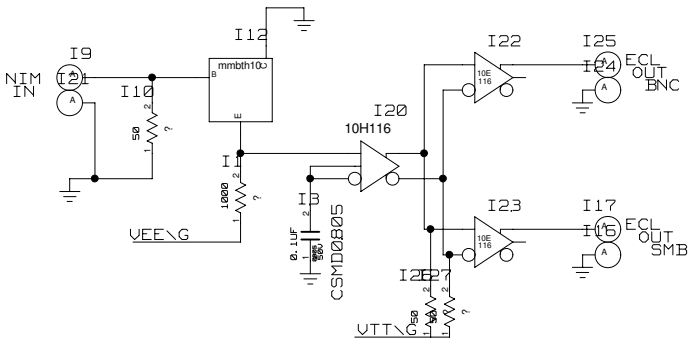
DATA INPUT
FROM EG SLOW CONTROL



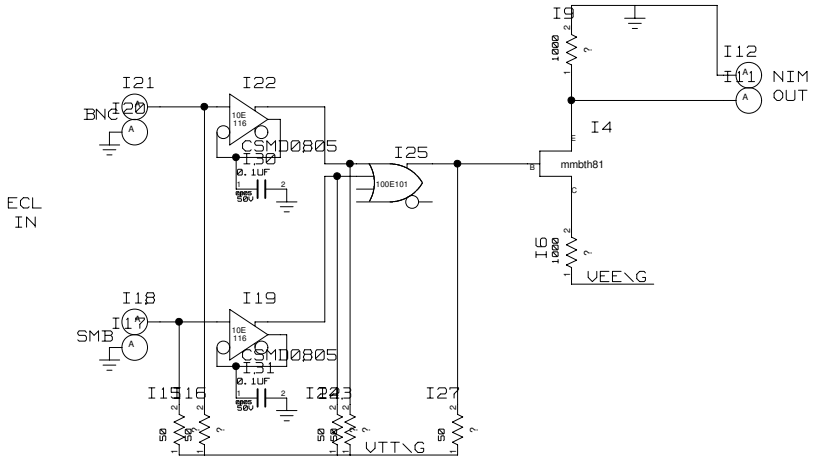
UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: DATAIN	DATE:
ENGINEER:	PAGE:


FAN-IN OF ADDITIONAL
EXT TRIGS TO MTC/D
(NO LATCH!)
TTL
INPUT
OPTIONS
ECL
INPUT
OPTIONS
RAW TRIG TO MTC/D
TWISTED
PAIR
ECL
VTT\G
100e101
10H124
10E
116
F
07
OC
MAX_DELAY=10000
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
TITLE:
EXTTRIG
DATE:
ENGINEER:
PAGE:

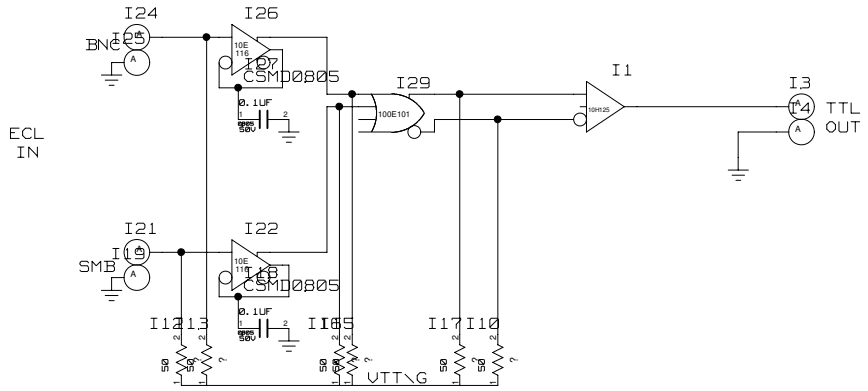

FAN-IN OF ADDITIONAL
EXT TRIGS TO MTC/D
WITH LATCH & MASK
ECL
INPUT
OPTIONS
TTL
INPUT
OPTIONS
EXTTRIG<7..0>\I
EXTTRIG<15..8>\I
LATCHED RAW TRIG
ECL
BNC
CSMD0805
0.1UF
LRAWTRIG\I
RAWTRIG\I
VCC\G
VTT\G
MAX_DELAY=10000
OC
ECL
TWISTED PAIR
RAW TRIG
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
TITLE:
LATCHED EXT TRIG FAN-IN
DATE:
ENGINEER:
PAGE:



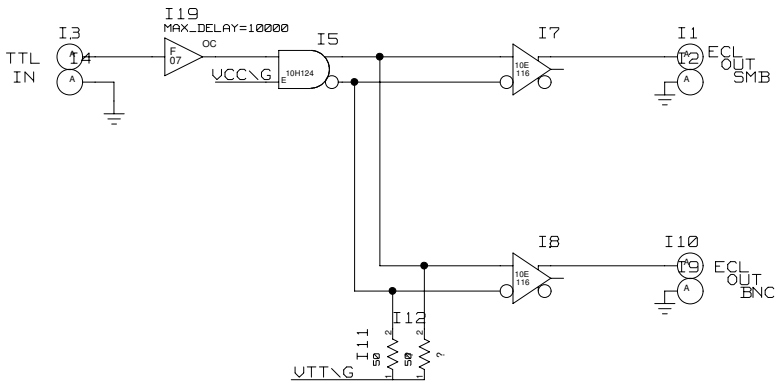
UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS		
TITLE: NIM-ECL CONVERSION		DATE:
ENGINEER:		PAGE:



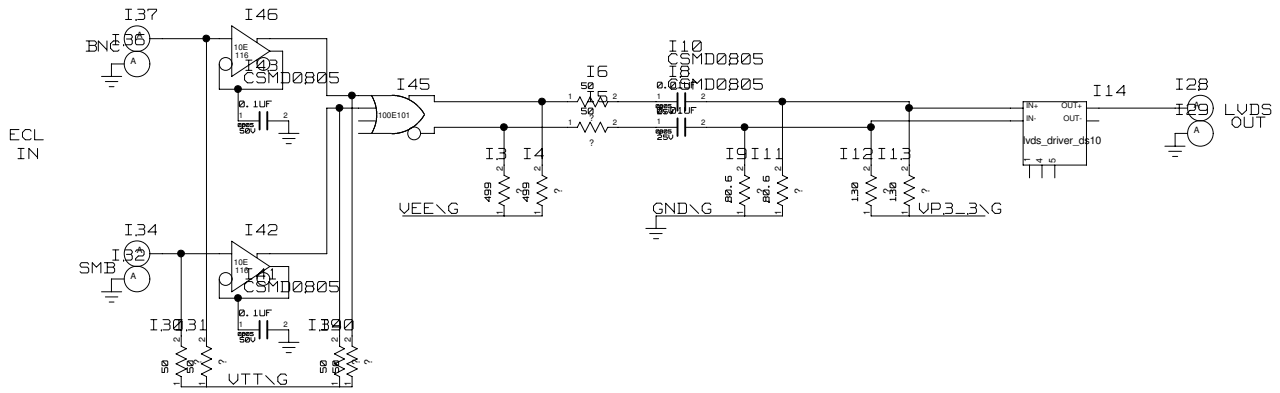
UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: ECL-NIM CONVERSION	DATE:
ENGINEER:	PAGE:



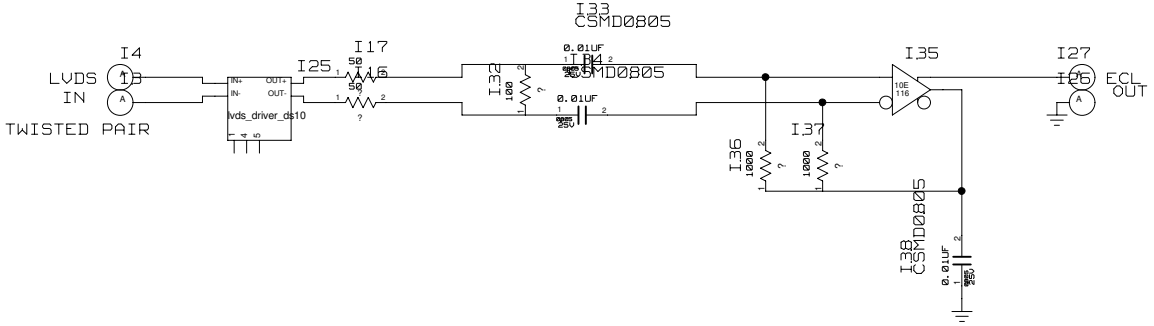
	UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: ECL-TTL CONVERSION		DATE:
ENGINEER:		PAGE:



UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS		
TITLE: TTL-ECL CONVERSION		DATE:
ENGINEER:		PAGE:



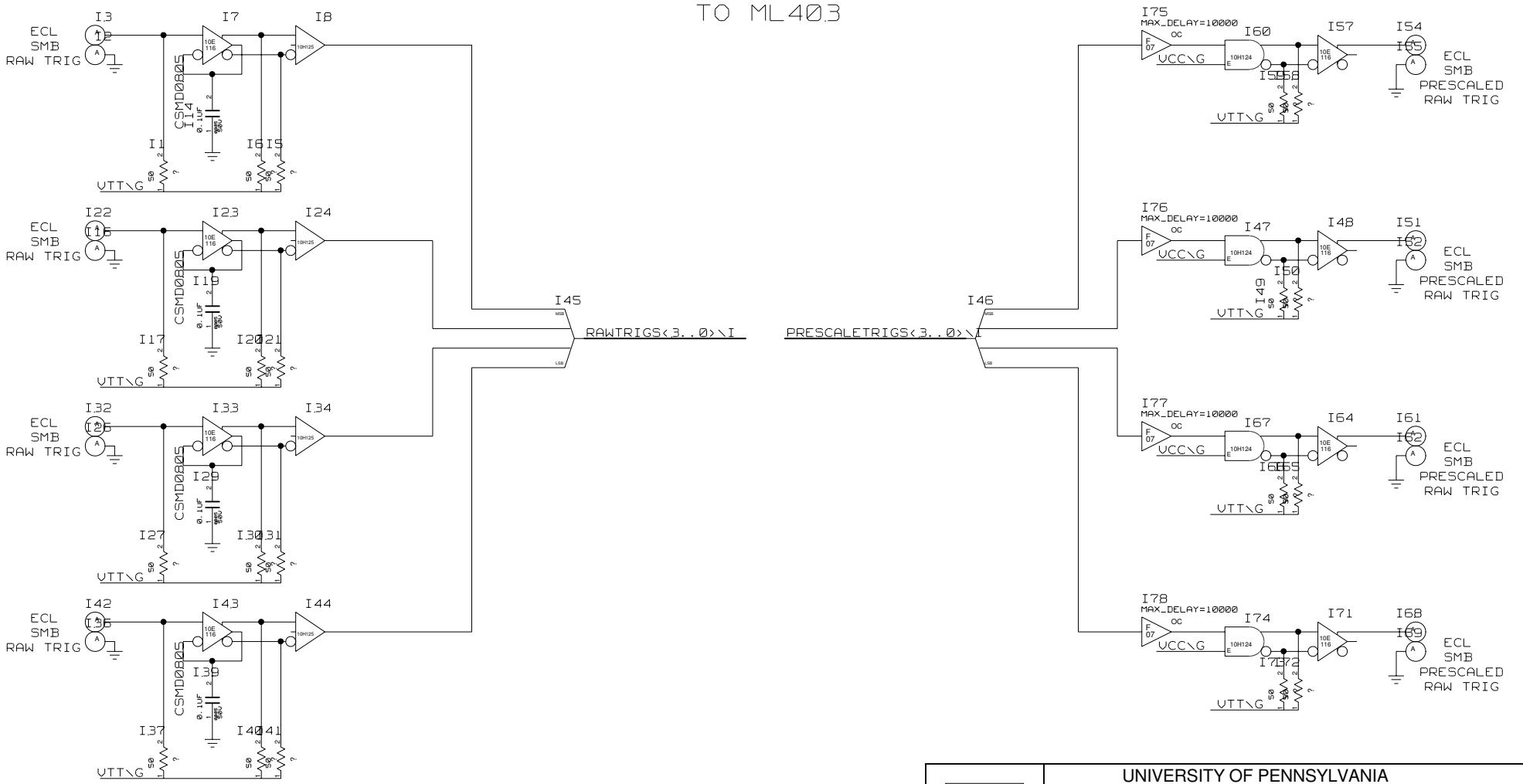
UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: ECL-LVDS CONVERSION	DATE:
ENGINEER:	PAGE:



UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

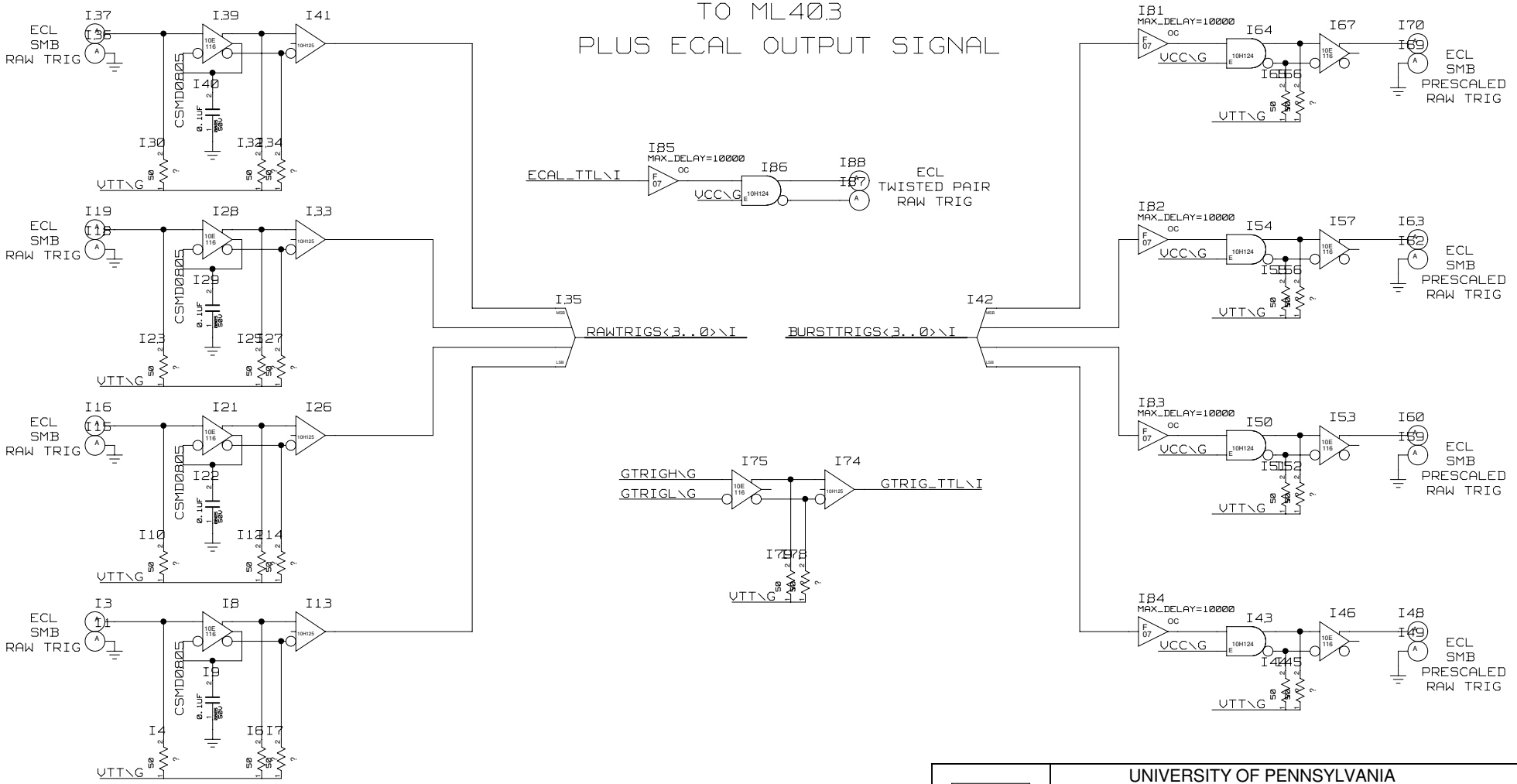
TITLE: LVDS-ECL CONVERSION	DATE:
ENGINEER:	PAGE:

PRESCALE TRIGGER:
INPUTS AND OUTPUTS
TO ML403

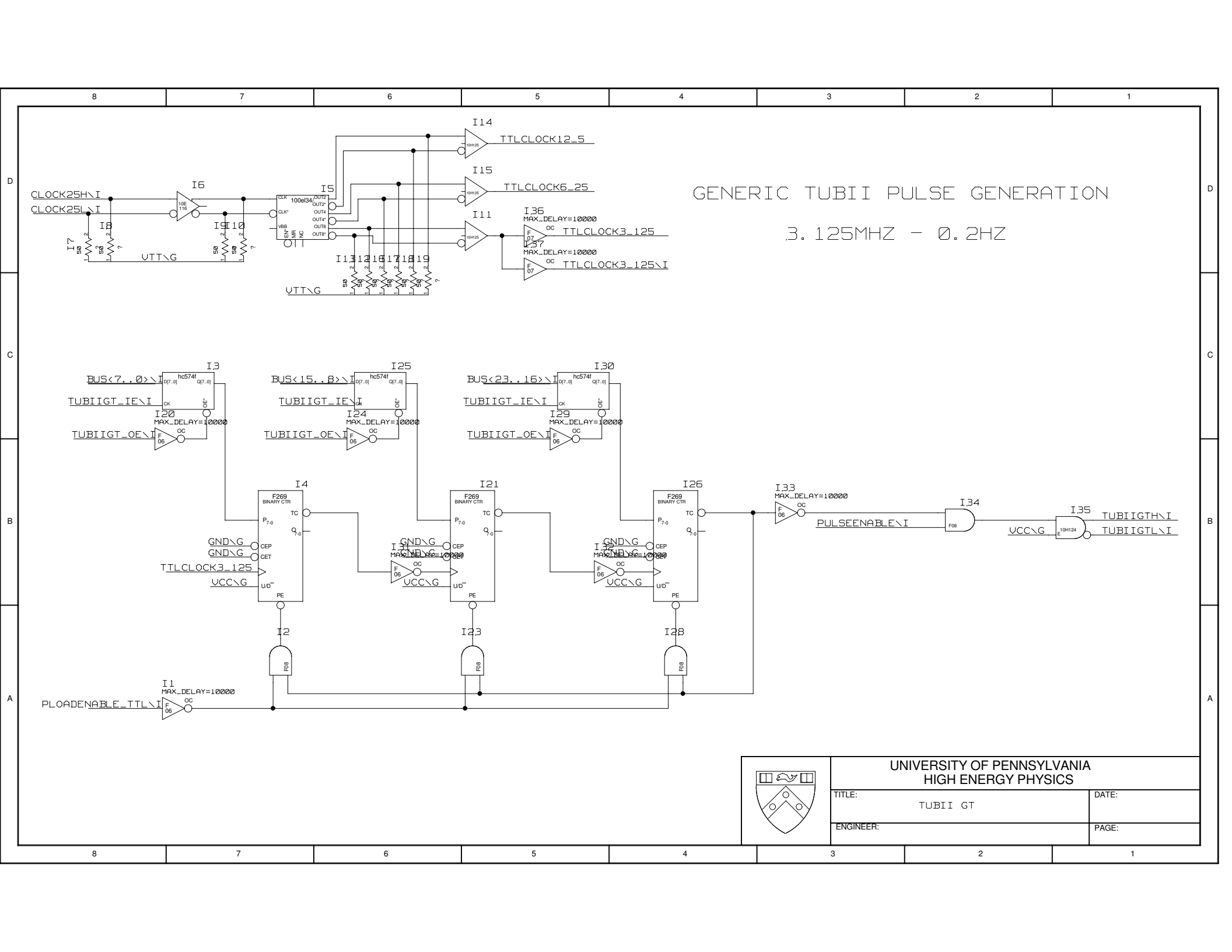


UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: PRESCALETRIG	DATE:
ENGINEER:	PAGE:

BURST TRIGGER:
INPUTS AND OUTPUTS
TO ML40.3
PLUS ECAL OUTPUT SIGNAL

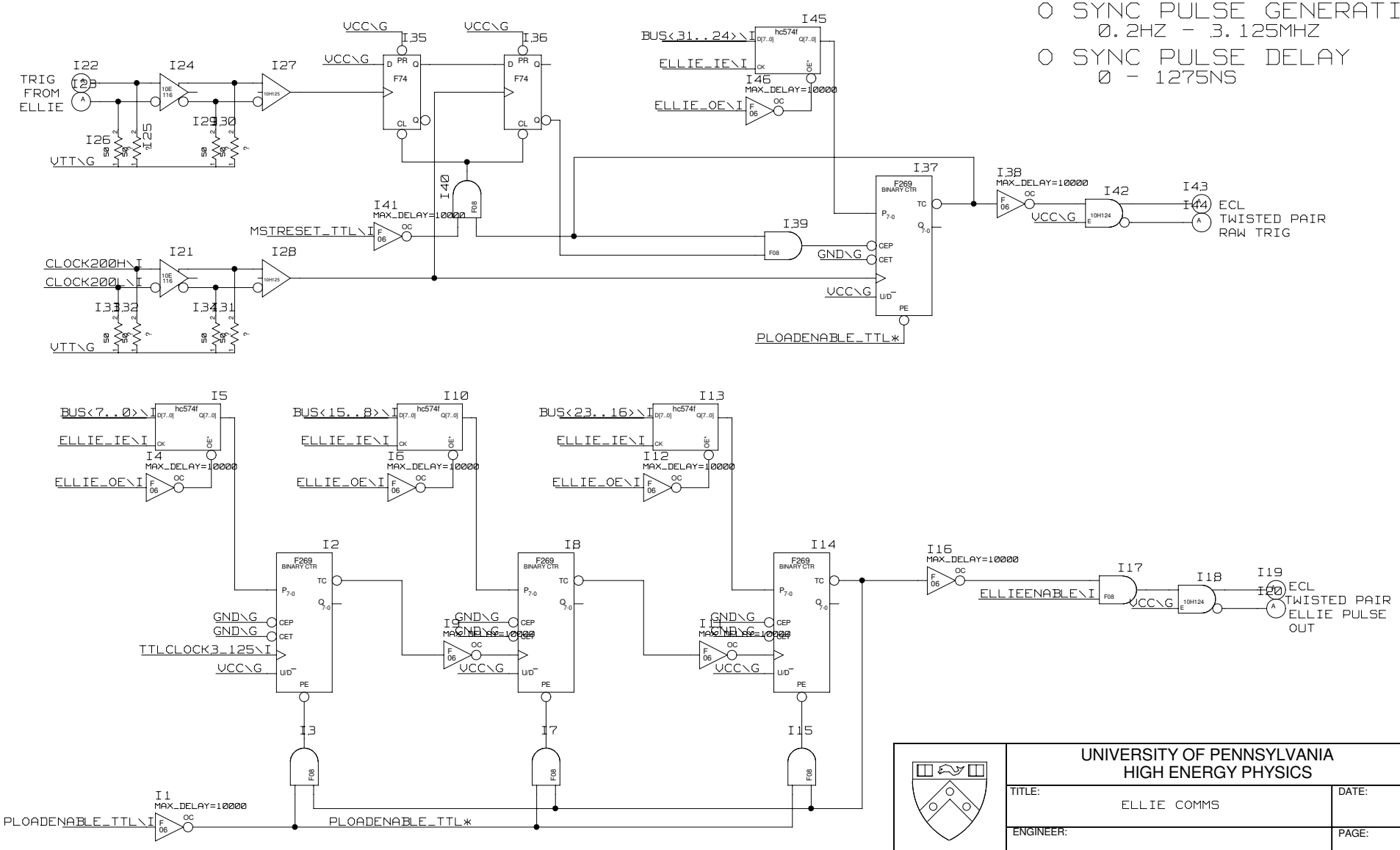


UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: BURST TRIGGER	DATE:
ENGINEER:	PAGE:


GENERIC TUBII PULSE GENERATION
3.125MHZ - 0.2HZ
CLOCK25H\I
CLOCK25L\I
VTT\G
TTLCLOCK12_5
TTLCLOCK6_25
TTLCLOCK3_125
TTLCLOCK3_125\I
MAX_DELAY=10000
BUS<7..0>\I
BUS<15..8>\I
BUS<23..16>\I
TUBIIGT_IE\I
TUBIIGT_OE\I
GND\G
VCC\G
PULSEENABLE\I
PLOADENABLE_TTL\I
TUBIIGTH\I
TUBIIGTL\I
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
TITLE:
TUBII GT
DATE:
ENGINEER:
PAGE:

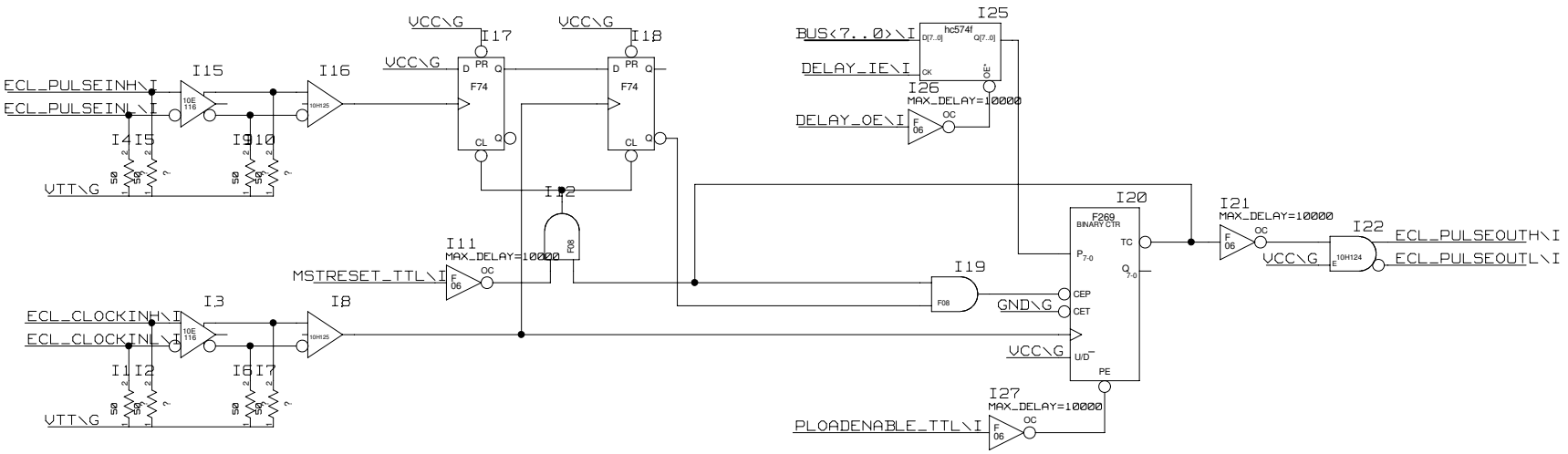
ELLIE COMMS

- SYNC PULSE GENERATION
  0.2HZ - 3.125MHZ
- SYNC PULSE DELAY
  0 - 1275NS



UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: ELLIE COMMS	DATE:
ENGINEER:	PAGE:

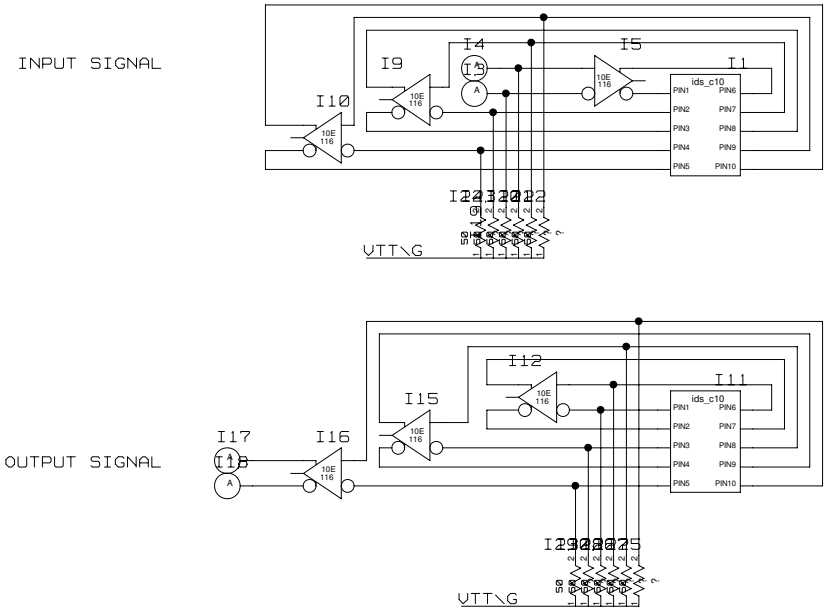
PROGRAMMABLE DELAY
IN TTL
(CONTROLLED BY ML40.3)



UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

TITLE: TTL PROGRAMMABLE DELAY	DATE:
ENGINEER:	PAGE:

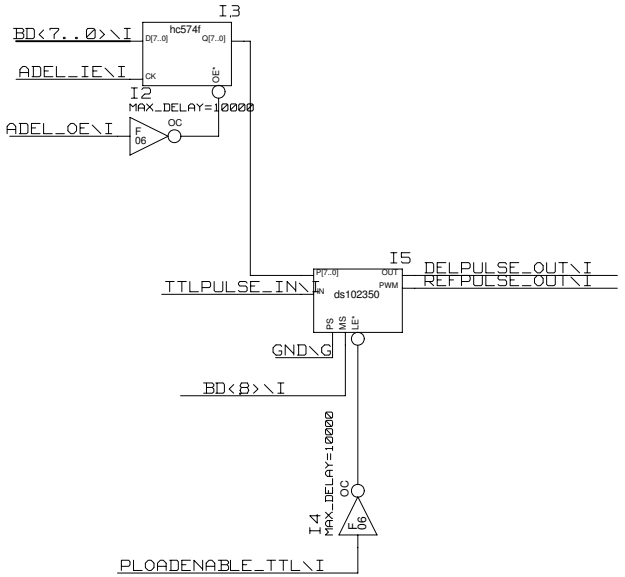
RIBBON-CABLE DELAY



UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: RIBBON DELAY	DATE:
ENGINEER:	PAGE:

ASYNCHRONOUS DELAY

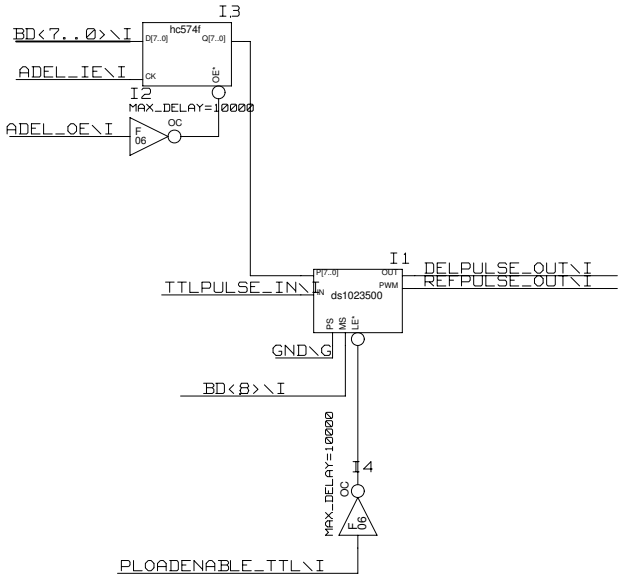
0 – 127.5 NS DELAY
IN 0.5NS STEPS



UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS		
TITLE: ASYNC DELAY		DATE:
ENGINEER:		PAGE:

ASYNCHRONOUS DELAY

0 - 1275 NS DELAY
IN 5.0NS STEPS



UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: LARGER ASYNC DELAY	DATE:
ENGINEER:	PAGE:

TUNABLE COMPARATOR CIRCUIT

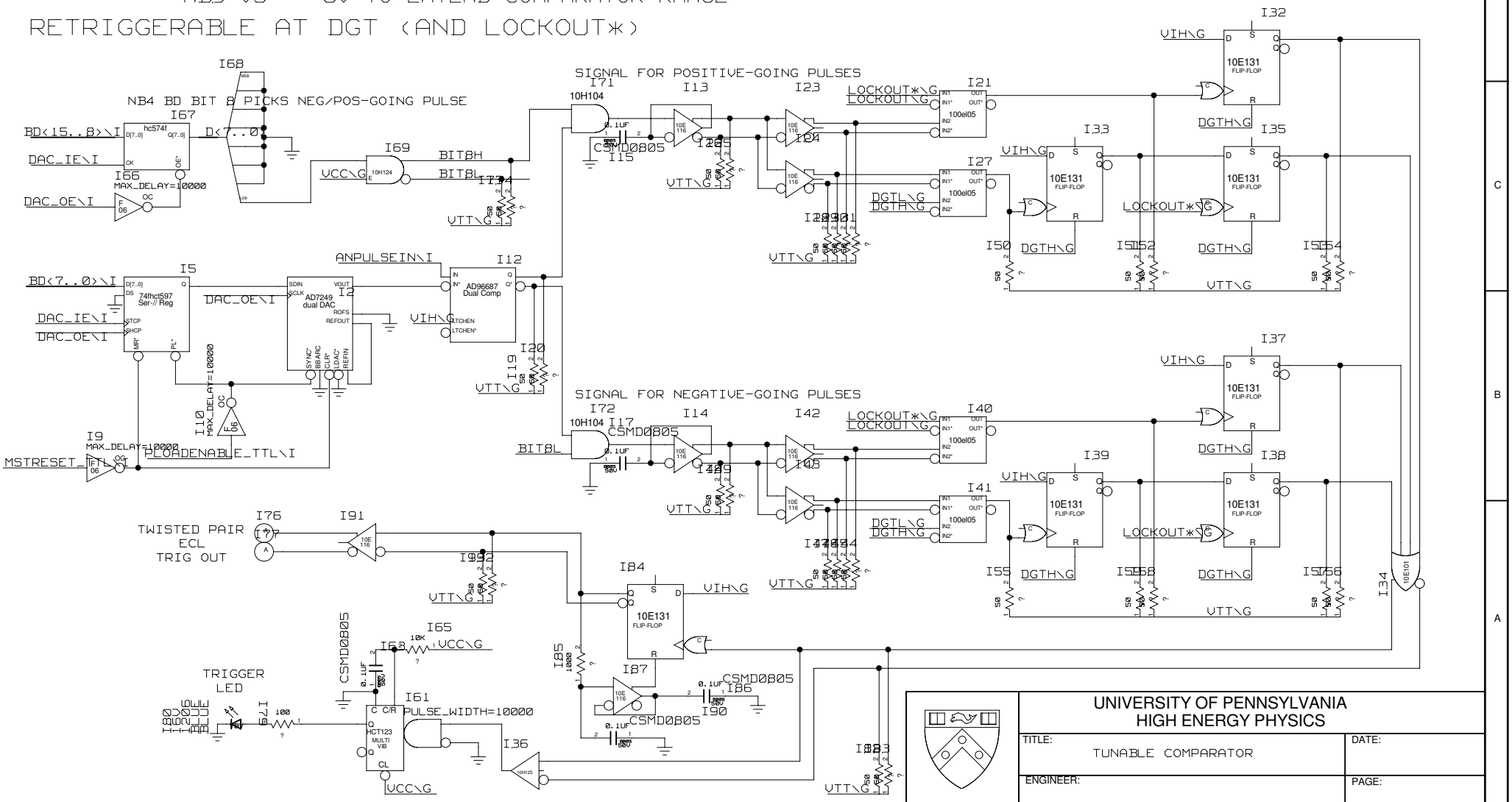
RANGE: −3.3 TO +5 V; 6.5 NS DELAY (2.5NS FROM COMPARATOR)

NB DAC_OE NEEDS TO CLOCK THE SERIAL DATA AT <50MHZ (PREF 25MHZ)

NB2 VDD = +15V VSS = −15V TO SUPPLY DAC

NB3 VS = −6V TO EXTEND COMPARATOR RANGE

RETRIGGERABLE AT DGT (AND LOCKOUT*)



UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: TUNABLE COMPARATOR	DATE:
ENGINEER:	PAGE:

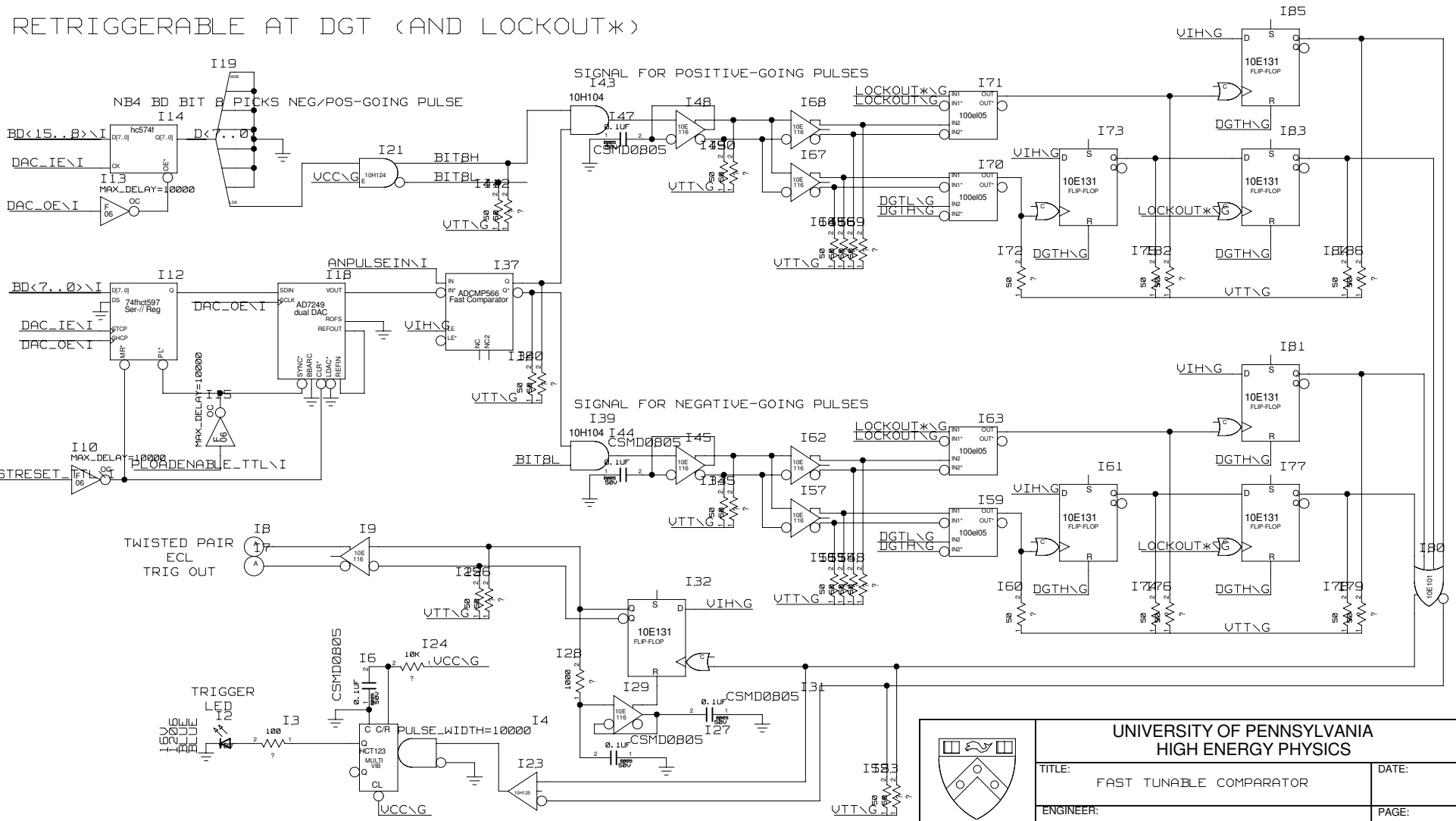
EXTRA SPEEDY TUNABLE COMPARATOR CIRCUIT

RANGE: −3.3 TO +5 V; 4.25 NS DELAY (250PS FROM COMPARATOR)

NB DAC_OE NEEDS TO CLOCK THE SERIAL DATA AT <50MHZ (PREF 25MHZ)

NB2 VDD = +15V VSS = −15V TO SUPPLY DAC

RETRIGGERABLE AT DGT (AND LOCKOUT*)



UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
TITLE: FAST TUNABLE COMPARATOR	DATE:
ENGINEER:	PAGE: