Tubii: The Proving Ground

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Abstract

- Make Testing Document

1 Powers

- Use multimeter check that there are no shorts between the various powers. (VCC,GND,V3P3,VEE,VTT,VCCIO,V15,V15M)

- Plug in the board to each power if they're availible

- Test regulators (note the VCCIO regulators output should be 0V until the enable pin is used) (Or maybe on second thought the output will be 3.3V when b/c the enable pin is disconnected,I'm not sure, but you can test that the output turns on/ off when the enable pin is low/high)

2 MicroZed

- Stuff the lv06a that will control the VCCIO regulator. Then stuff and plug in the MicroZed (MZ)

- Make sure the MZ turns on (LEDs light up and all)

- Make sure the VCCIO banks get 3.3V

- Check that the various lv07a/lvc07a's all work and that outputs from the MZ make it through them with decent gain (ie 3.3V signals go to 5V signals)(Note the shift register CLK/Data line may be an excpetion here, more on that later)

- MZ Happy light is on when MZ is plugged in and turned on

- MZ Hppy light is off when MZ is unplogged and or off

3   Multiplexer

- Check that each the multiplexer turns on/off appropriately

- Check that each line can be addressed as expected

4   ControlRegister

- The 74hct164 can be loaded with arbitrary 8bits.

- These 8bits don't showup at the various parts they feed into until the data ready line is strobed.

- The 8bits can be read back in in a non-destructive manner

5   GlobalTriggering and GT Delays

- Confirm that the GT shows up on TUBii and looks alright (squarish)

- Check that it gets delayed (at all) by the two DS1023s in GT_Delays section

- Check that these delays can be changed by loading their shift registers.

- Check that the daisy chainging of their shift registers works

- Check that the GT gets to the MZ

- Check that the MZ is able to count GTs and keep a running GTID

- The Microzed can choose between DDGT and LO_MTCD

- Check the all pulses (GT,DGT,DDGT,LO*) are down-going or up-going as they should be. NOTE TO SELF, FIGURE OUT HOW THEY SHOULD BE GOING

6   Clocks

6.1   Default Clock Select

- Some surgery is needed to get the clock in place. Check that a 200MHZ signal comes out of it at all.

- Check the the LVPECL pull-down is working well

- Check that the 200MZ signal gets divided to 100MHZ

- Clock divider's reset button is working

- Clock divider reset signal from MZ is working

- Quality of external TUB clock is good

- One clock becomes Default and the other becomes backup

- The clock that is default can be switched with backup and vice versa

6.2 Fault Detection

- The DefaultClock (DefCLK) signal's frequency gets divided and the various jumpers can pick between frequencies.

- No DefCLK signal makes output of the HCT123 changed.

- Some noticable change in the system happens when the DefCLK output is missing

- You can count how many clock pulses get missed. (ie you get 100mhz pulses while the DefCLK is gone and they go away when DefCLK shows up again)

- The mc10e016 emits a signal if many clock pulses are missed

- The MC10e016's shift register can be loaded and this allows you to pick how many pulses until TC does something

- The output of that fucking rats nest that hangs off of TC makes at least some sense, good fucking luck buddy.

- The MZ gets told when the clocks should be changed

6.3 Change Clocks

- When physical switch is thrown one way the clock at output is exactly the same as back up clock

- When thrown the other way the output clock is the DefCLK unless DefCLK ChangeCLK signal is high.

- The various LEDs light up in a way that makes some sense/is useful

7 Ecal Control

- The control register outputs an ECAL_ACTIVE signal that can be actively changed by the MZ.

- The LED corresponding the the ECAL_ACTIVE signal works

- When ECAL_ACTIVE is high the output is GT

- When ECAL_ACTIVE is low the output is EXT_PED_IN

8 ELLIE

9 CAEN Interface

9.1 CAEN Digital

9.2 CAEN Analog

- This will never work, give up

10 Baseline Monitoring

- I'm not exactly sure how to test this...figure it out

11 MTCA_MIMIC

- DAC can be set by the MZ to output a sensible volatage value

- The stupid pot can be tuned to output equally sensible voltage values

- Comparator outputs signal appropriate signal when Analog Pulse is over/under DAC threshold

- Comparatoroutputs signal appropriate signal when Analog Pulse is over/under POT threshold

- GT DGT, and LO* all show up as expected.

- The DGT_Gate signal makes sense.

11.1 Trigger Logic

- Comparator outputs high when a signal goes over the DAC value AND the physical switch is thrown such that positive going pulses are selected

- Comparator outputs high when a signal goes over the POT value AND the physical switch is thrown such that positive going pulses are selected

- Comparator outputs high when a signal goes under the DAC value AND the physical switch is thrown such that negative going pulses are selected

- Comparator outputs high when a signal goes under the POT value AND the physical switch is thrown such that negaitve going pulses are selected

12 General Utilities

12.1 Generic Delays

- Emits a TTL that can be delay by a tuneable amount that roughly matches the input signal

- Blinks an LED that matches the delay

12.2 Generic Pulser

- Emits a TTL pulse at a frequency that can be chosen by the user.

12.3 Pulse Inverter

- Analog pulses can be changed from upward going to downward going

- Analog pulses can be changed from downward going to upward going

12.4 Ribbon Delay

- ECL pulses can be delayed by an amount that makes physical sense (i.e. a meter long cable leads to a few ns of delay)

12.5 Pulse Scaler

- The MZ can output signals that increment the the display

- The display can show the frequency (in Hz) of signals

- lead zero blanking can be turned on/off by control register

12.6 Translation

- TTL pulses go to ECL pulses

- ECL pulses go to TTL pulses

- LVDS pulses go to ECL pulses

- ECL pulses go to LVDS pulses

- NIM pulses go to ECL pulses

- ECL pulses go to NIM pulses

13 Speaker

- Speaker clicks when told to do so by MZ

- Speaker is loud enough

- Speakers loudness can kinda be tweaked by speaker pot

- Speaker outputs a signal that can be recorded by a computer

14 Shift Registers

Below is a list of all the shift registers on the TUBII. The LE MUX is the chip described in **??**. More specifically it is an hct238. For exact information on how to address each pin refer to the hct238's datasheet.

14.1 Control Register

- 8 bits. Serial in, parallel out
- Connected to pin 13 of LE MUX
- Designed to be programmed once at start up.
- Output gated by flip flops. Toggle $CNTRL\_RDY$ once programming is finished
- Each output acts as an input for the Read Control Register

14.2 Read Control Register

- 8 bits. Parallel in, serial out
- Used to read state of the Control Register non-destructively
- MZ toggles reads it serially by toggling Read_Enable pin (pin 1) each time it wants to see the next bit.
- The register is circular. So reads should be done 8 at a time.

14.3 CAEN Register

- 16 bits. Serial in, parallel out
- Connected to pin 15 of LE MUX
- The bits 0-3 select between analog pulses for the CAEN
- The 4-7 bits do nothing
- The bits 8-15 choose if analog pulses go to the CAEN or the scope outputs
- Bits 8-15 are gated by flip-flops. Toggle $CAEN\_RDY$ once programming is finished

14.4 GT Delays Register

- 16 bits. Serial in. No output
- Connected to pin 14 of LE MUX
- The data sets the delay length for the two delays
- Bits 0-7 set the time between GT and DGT
- Bits 8-15 set the time between GT and DDGT (LO)
- Bits 0-7 are for a DS1023200 and bits 8-15 are for a DS1023500. See their respective datasheets for programming information.

14.5 Generic Async Pulse Register

- 8 bits. Serial in. No output
- Connected to pin 7 of LE MUX
- The data sets the delay length for the generic pulser.
- The delay length should not exceed the time between pulses. I.e it should not try to delay a 1GHz pulse by 10ns.
- The delay chip is a ds102350. See it's datasheet for programming information.

14.6 Generic Async Delay Register

- 8 bits. Serial in. No output
- Connected to pin 9 of LE MUX
- The data sets the delay length for the generic delay.
- The delay length should not exceed the time between pulses. I.e it should not try to delay a 1GHz pulse by 10ns.
- The delay chip is a ds102350. See it's datasheet for programming information.

14.7 Comparator DAC Register

- 12 bits. Serial in. No output
- Connect to pin 11 of LE MUX
- The data sets the output voltage value for a DAC which acts as a threshold for one of the Comparators.
- The DAC is a AD7243. See datasheet for programming information.

14.8 Missed Clock Count Register

- 8 bits. Serial in, parallel out
- Connected to pin 10 of LE MUX

• Data is gated. Toggle *TubiiTime_Data_Time* once programming is finished.

• Outputs the value for how many missed counts are allowed before clock switch over