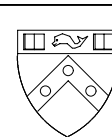


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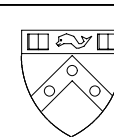
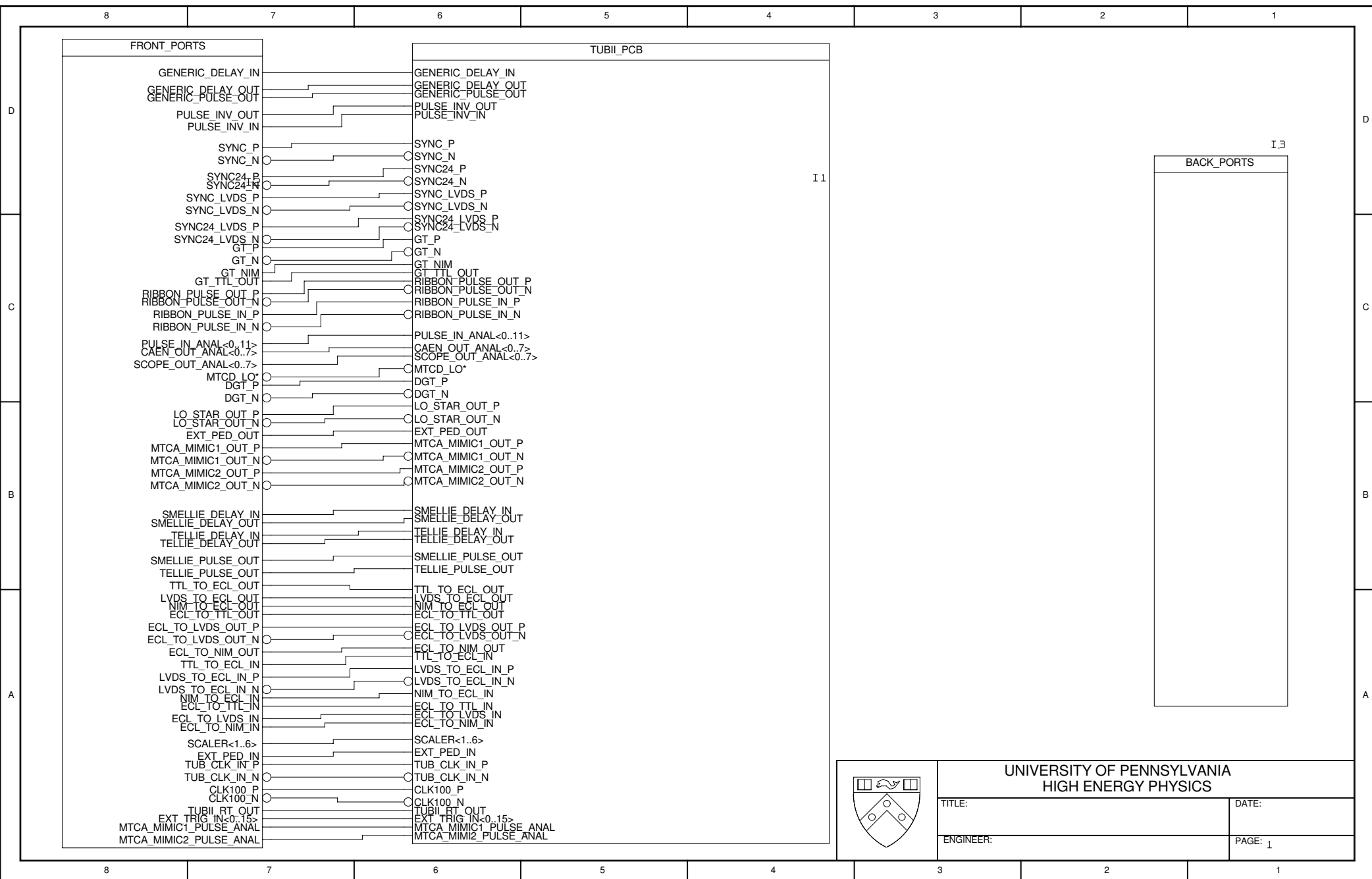
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HIGH ENERGY PHYSICS

TITLE: TUBII

DATE: 5-3-15

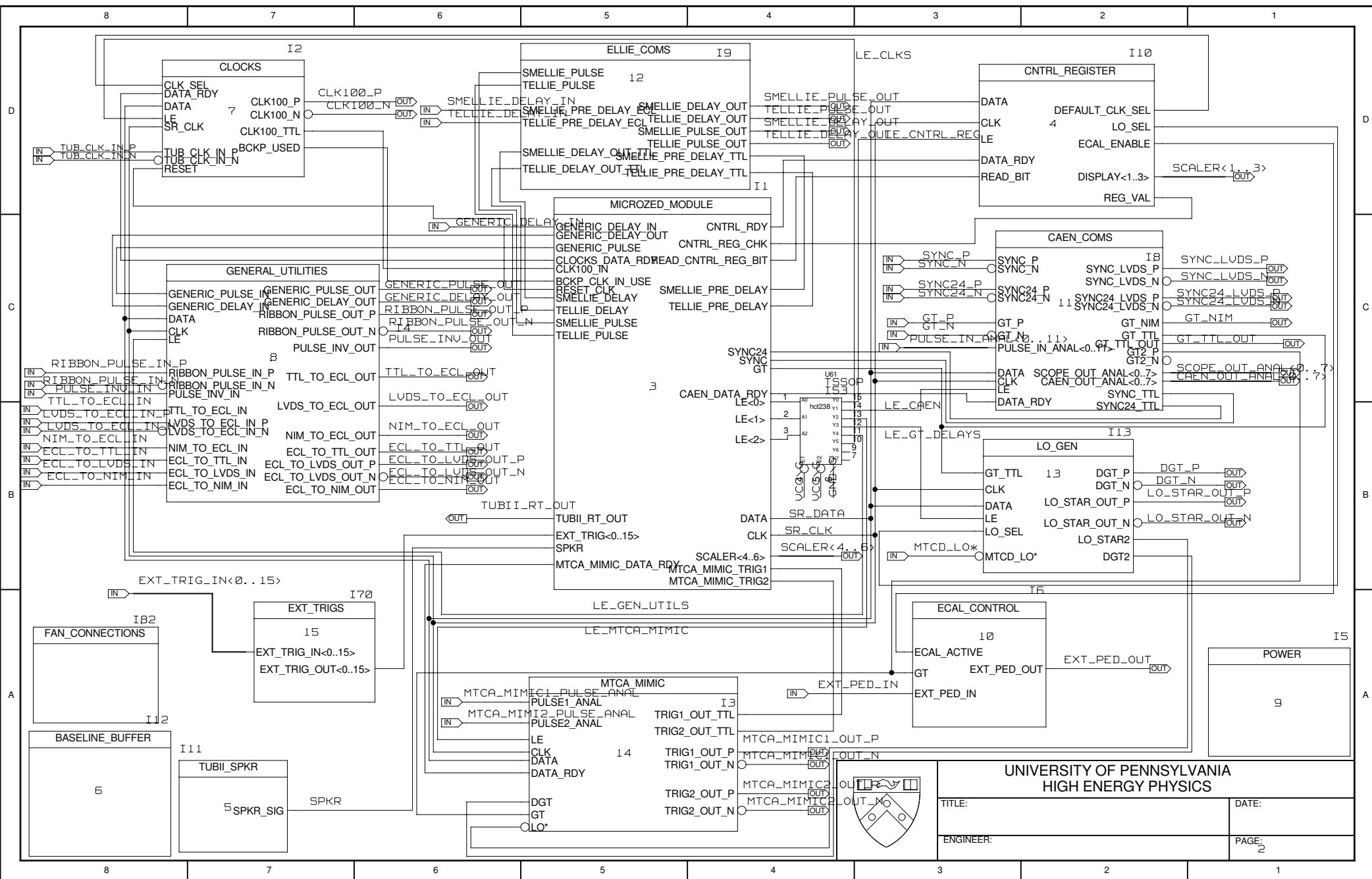
ENGINEER: ERIC MARZEC

PAGE:

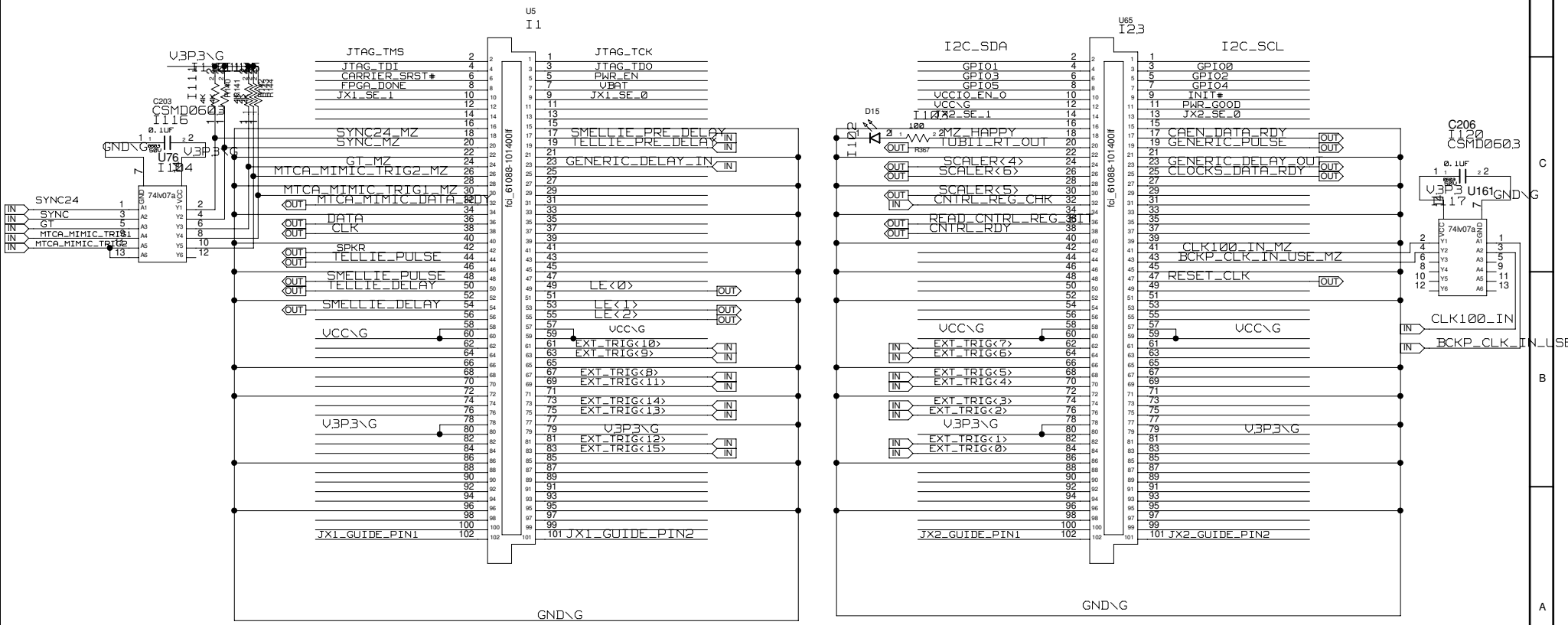


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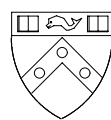
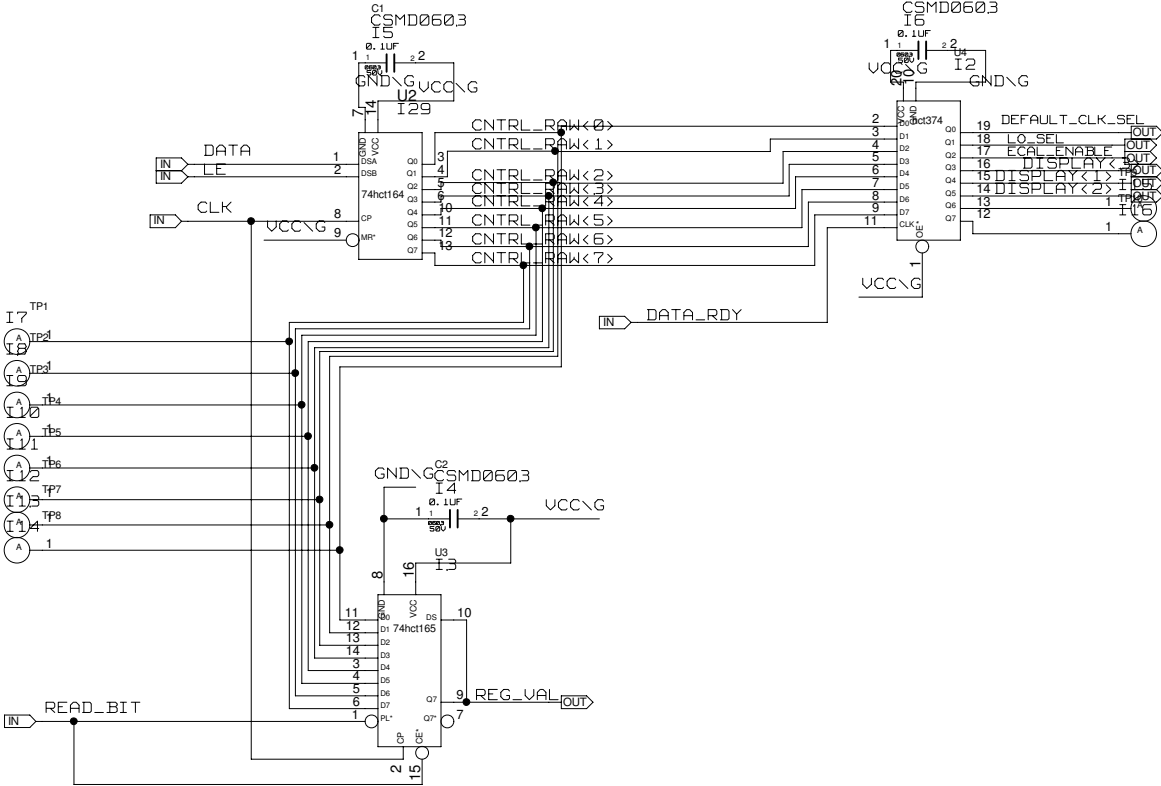
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MICROZED CONNECTION



CNTRL REGISTER



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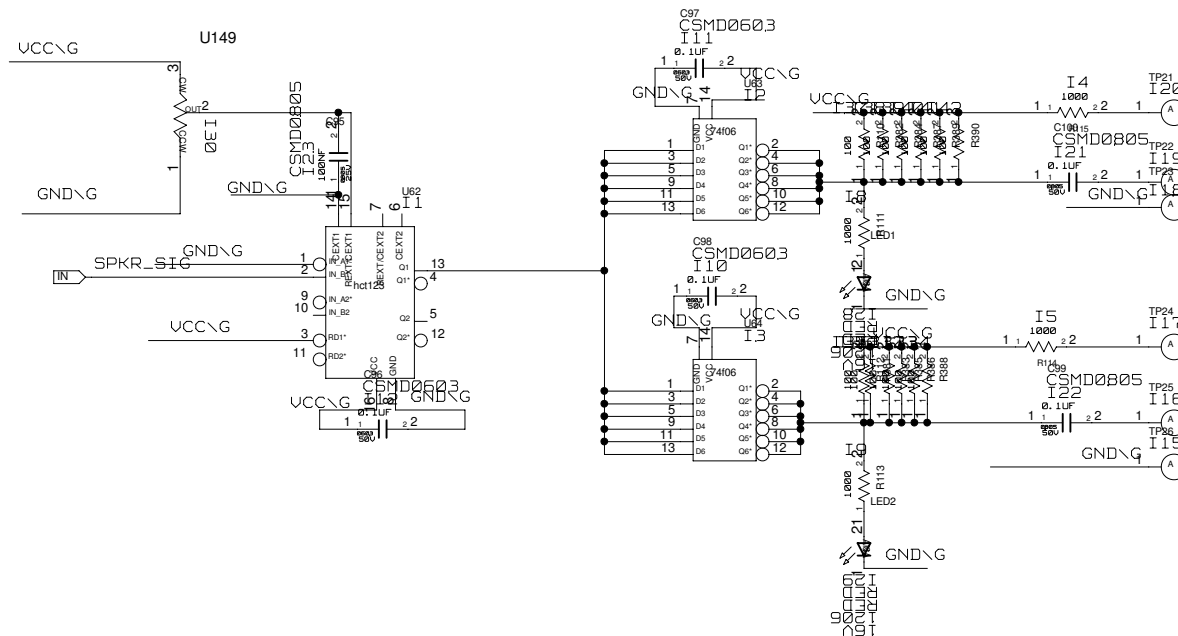
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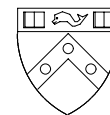
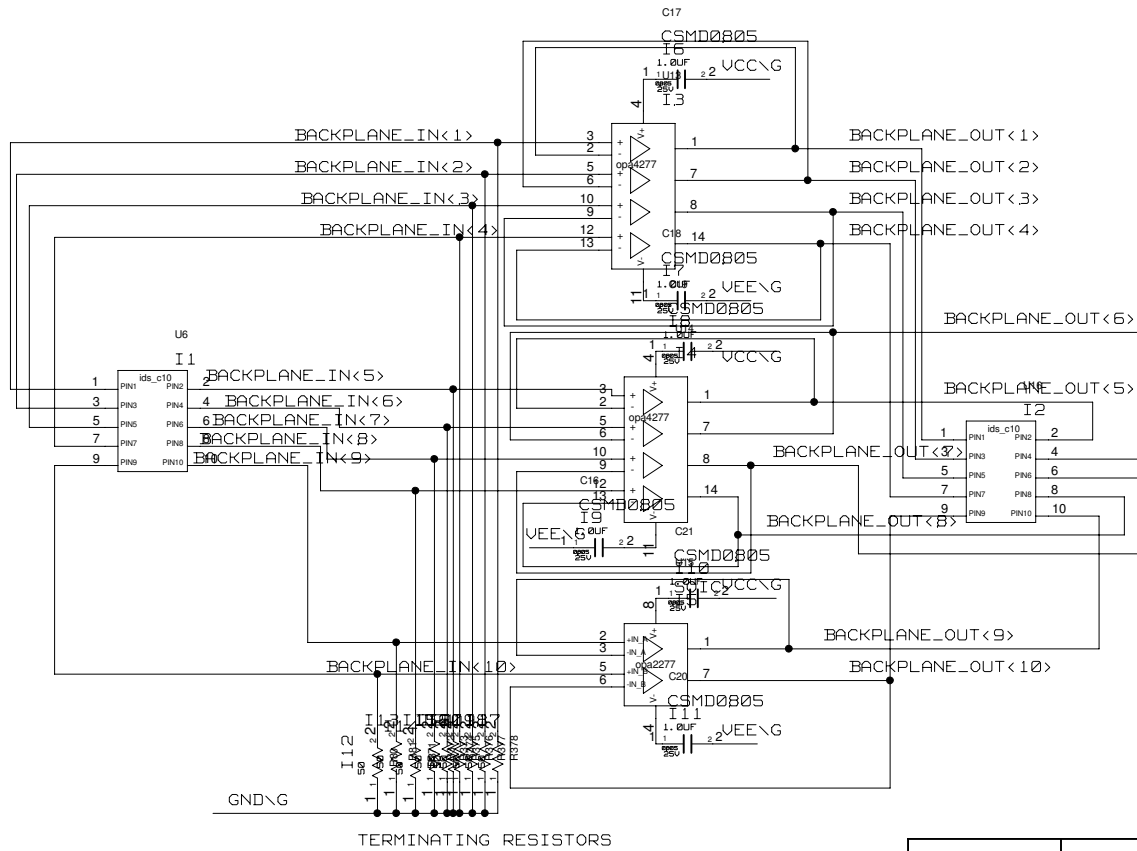
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SPEAKER

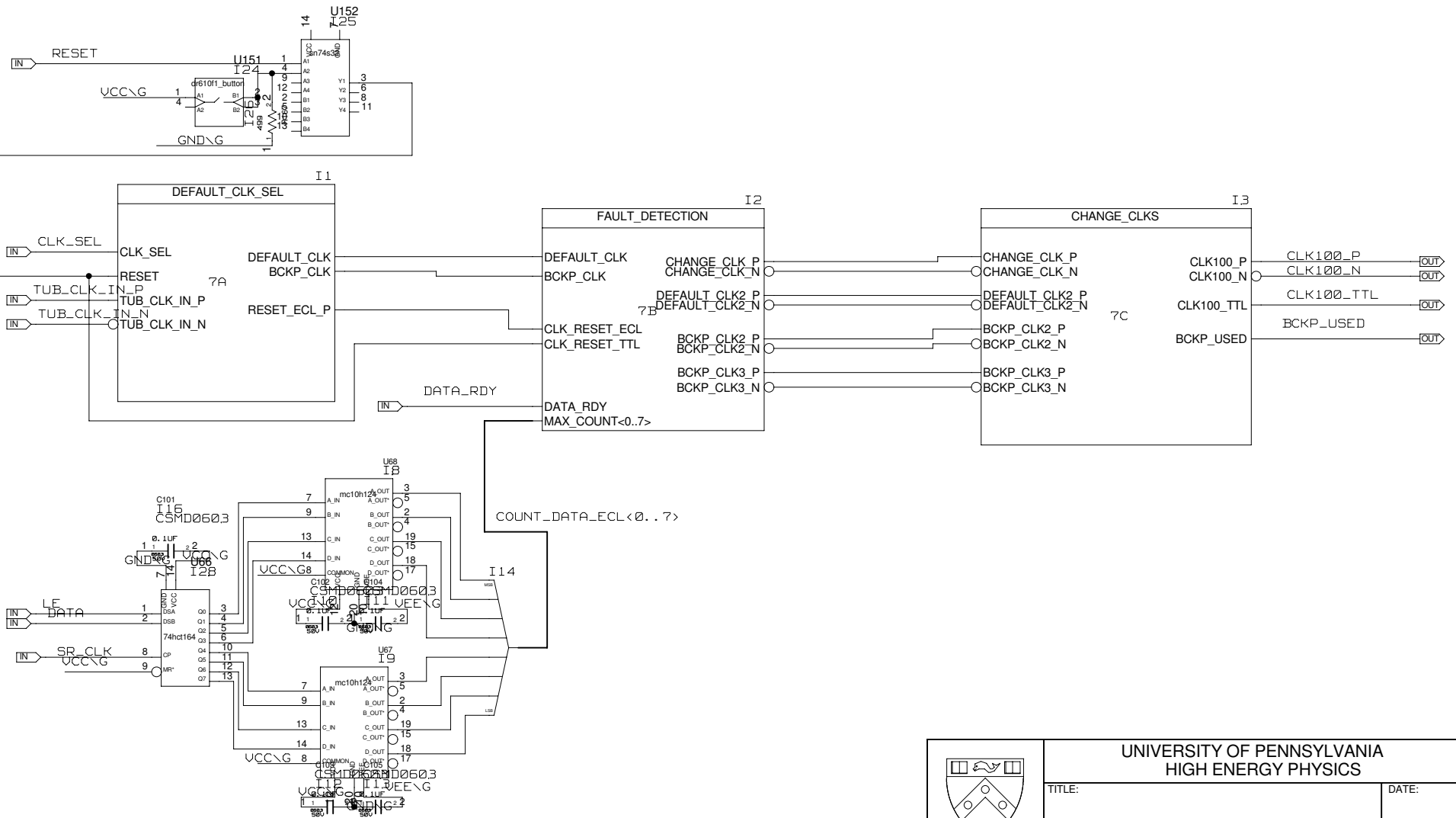


BASELINE BUFFER

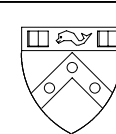
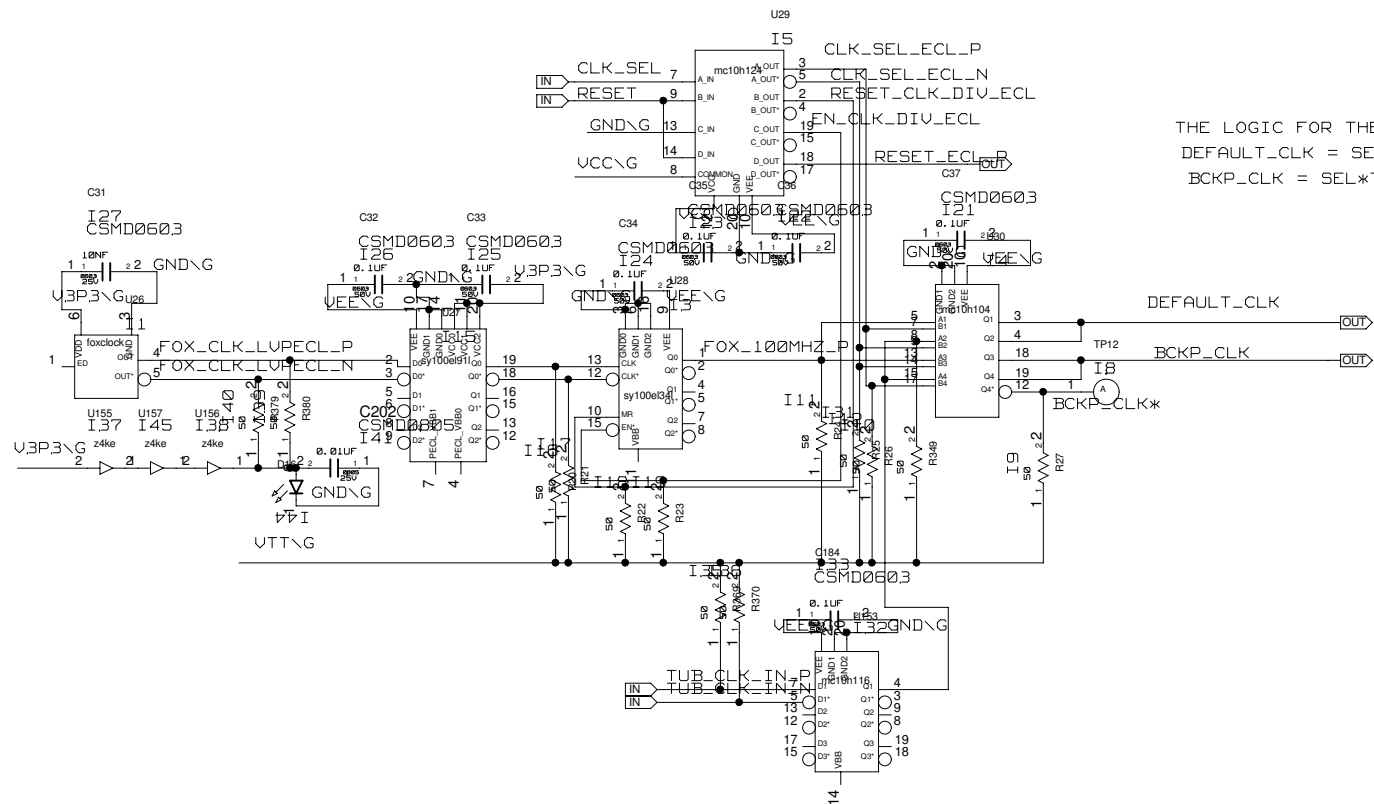
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CLOCKS



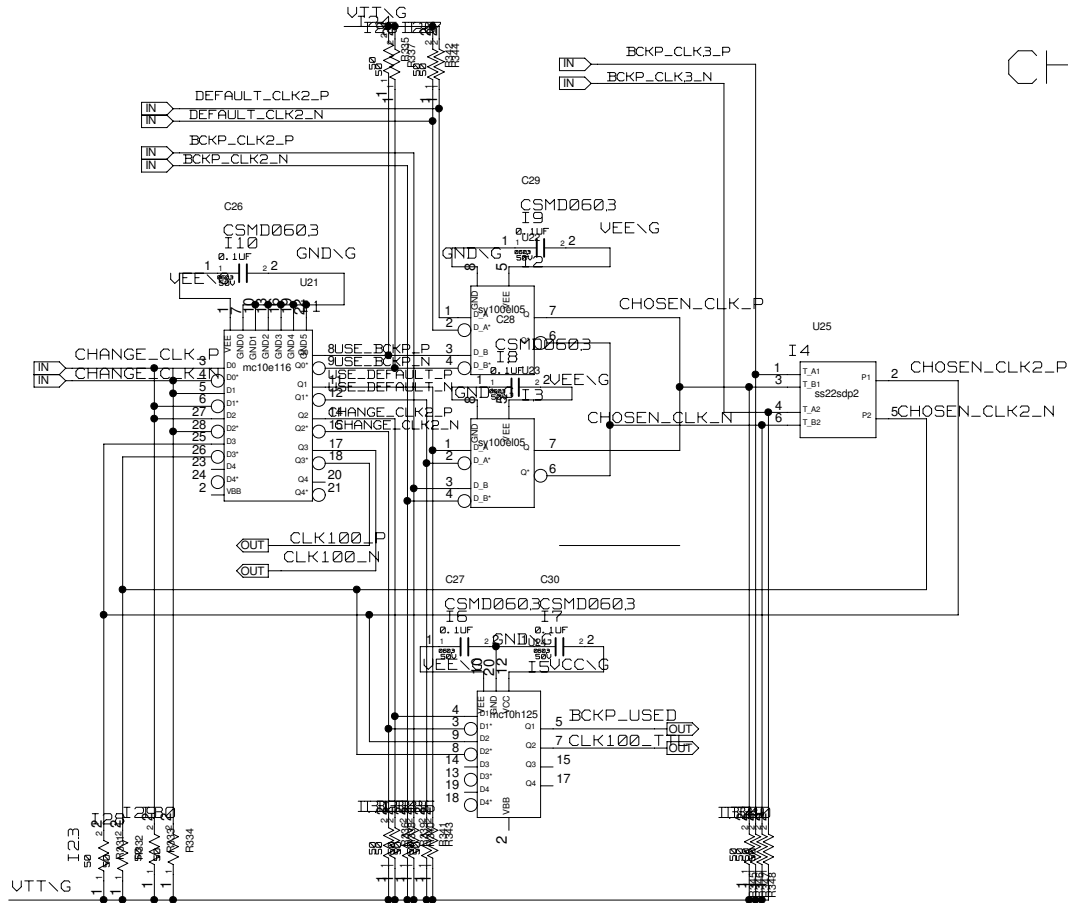
DEFAULT CLOCK SELECT




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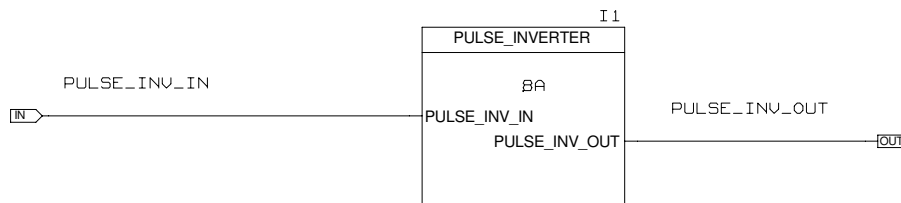
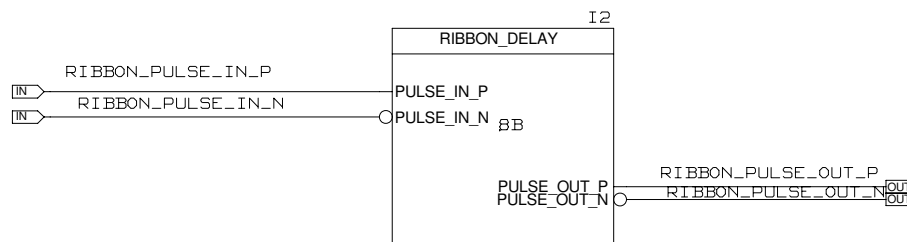
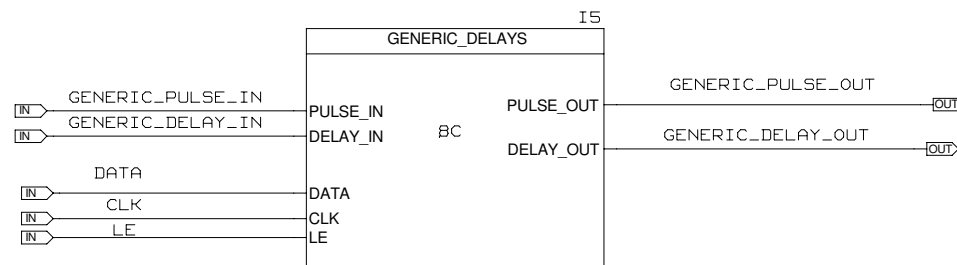
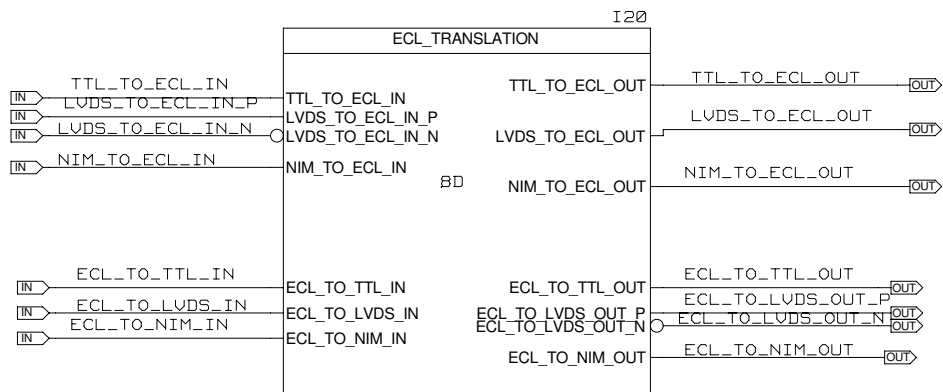
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CHANGE CLOCKS



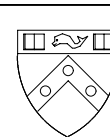
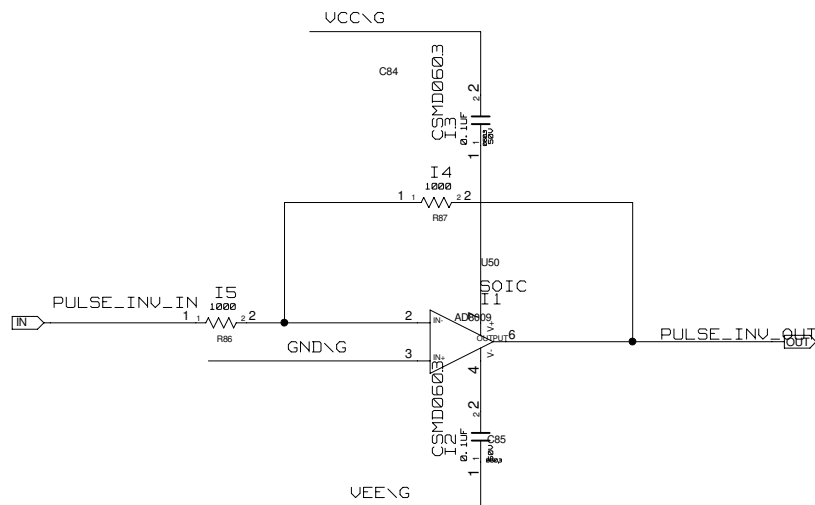
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GENERAL UTILITIES



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	TITLE:	DATE:
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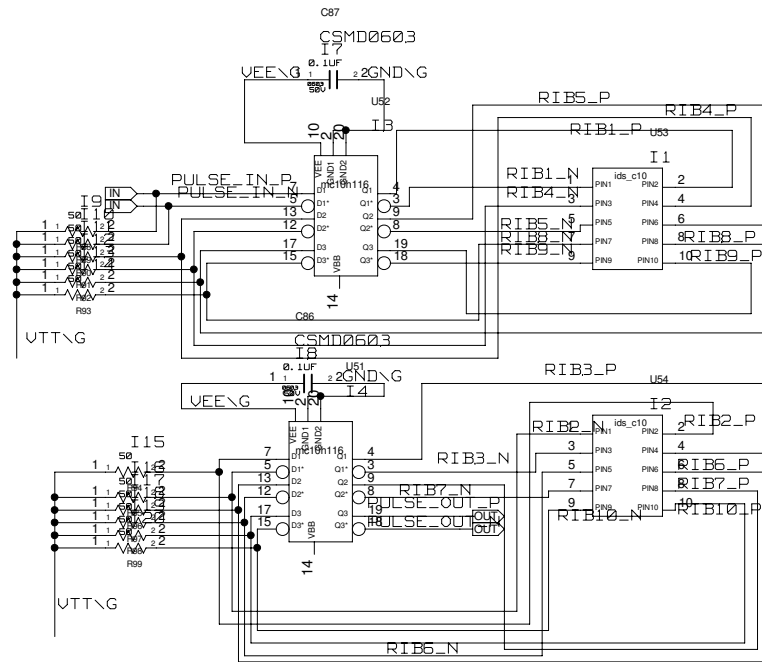
PULSE_INVERTER




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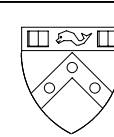
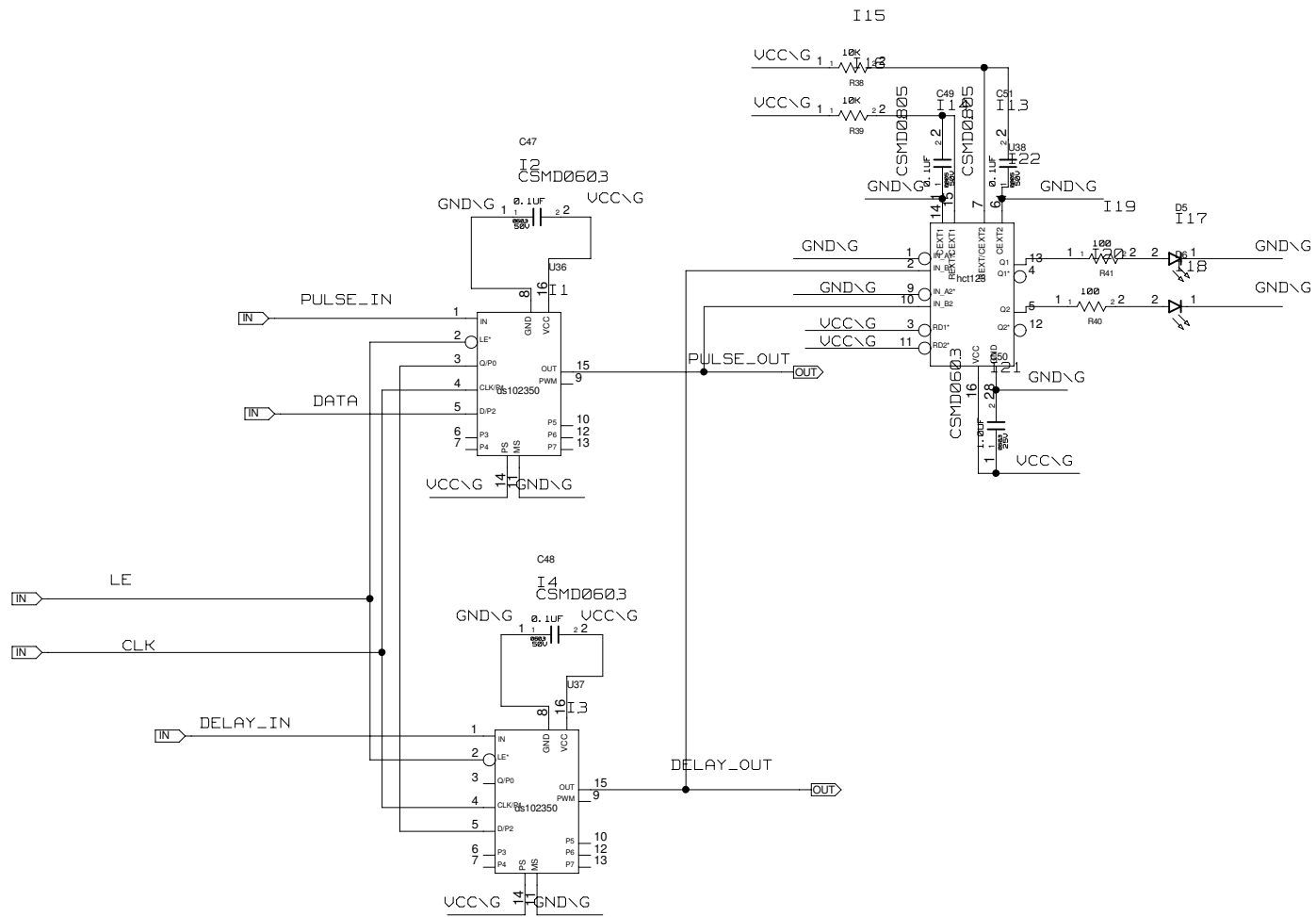
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RIBBON DELAY



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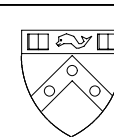
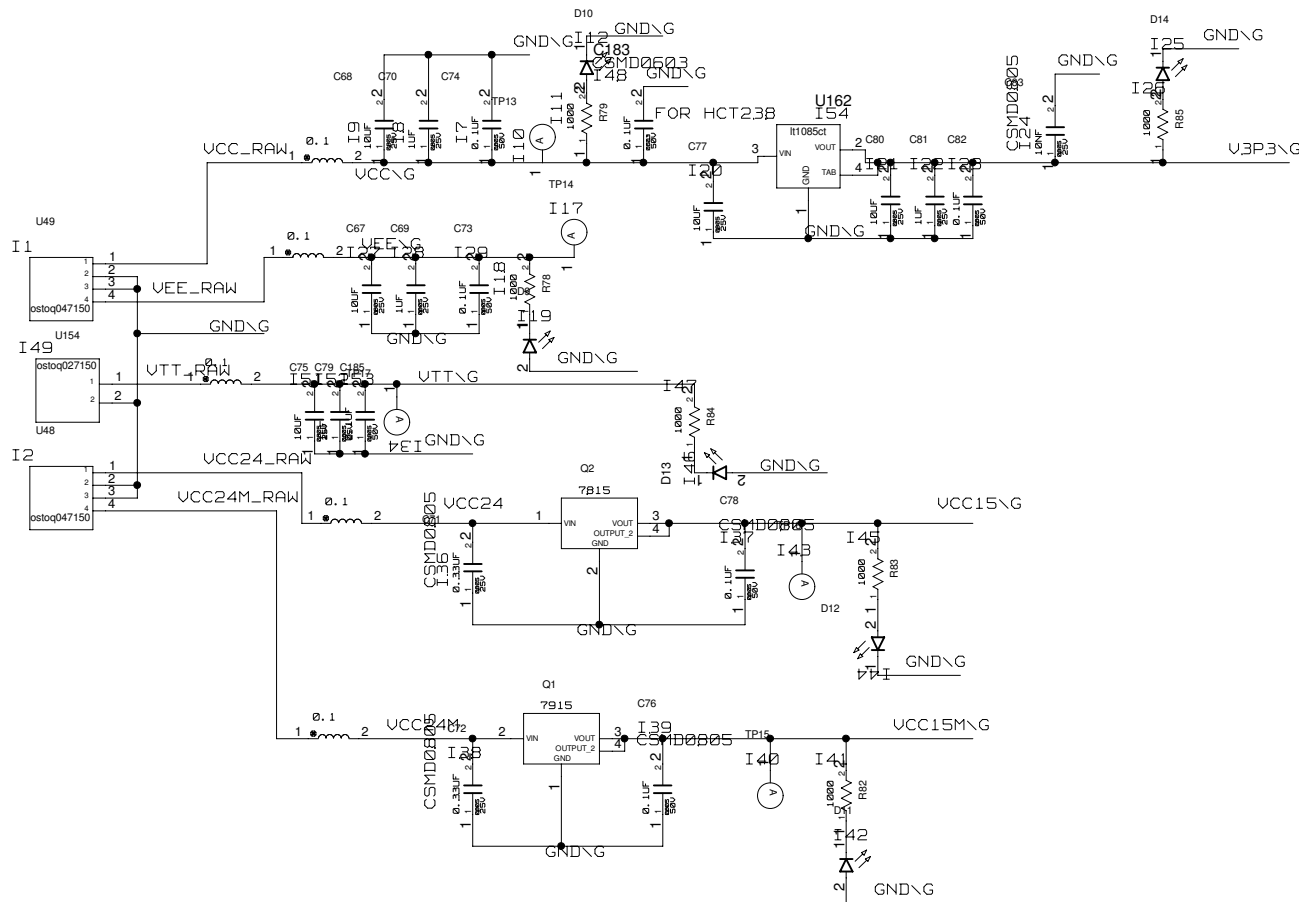
GENERIC DELAYS



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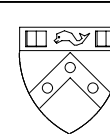
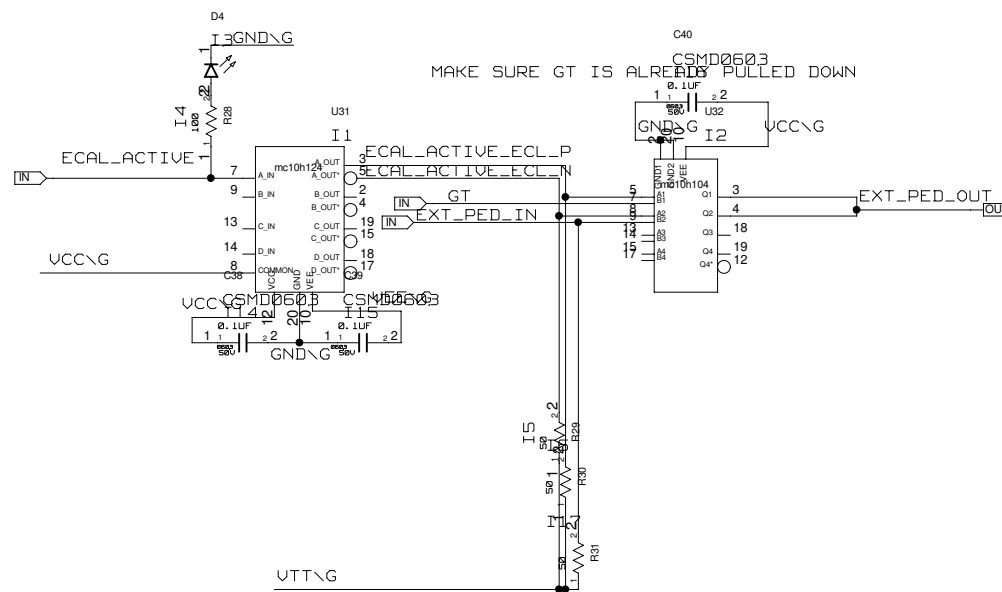
POWER



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ECAL CONTROL

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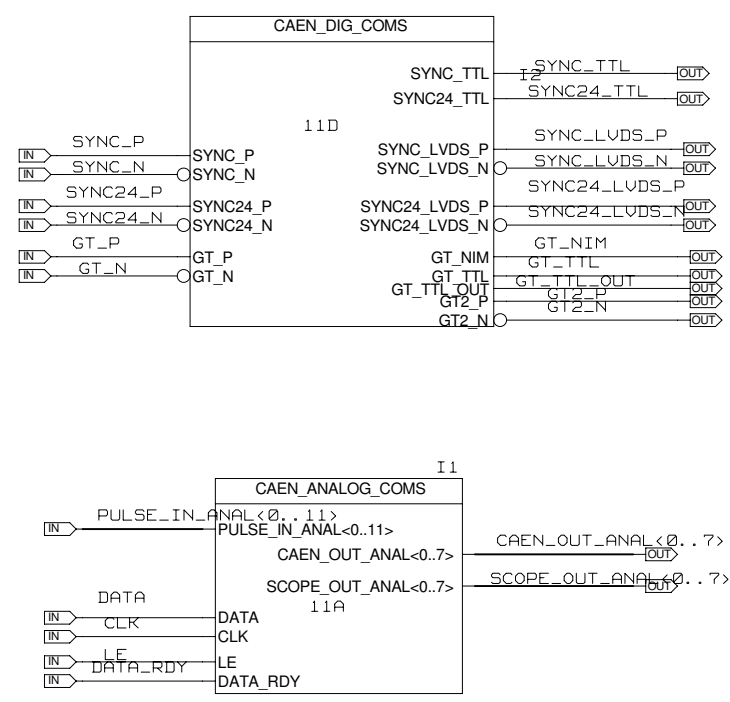
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DATE:

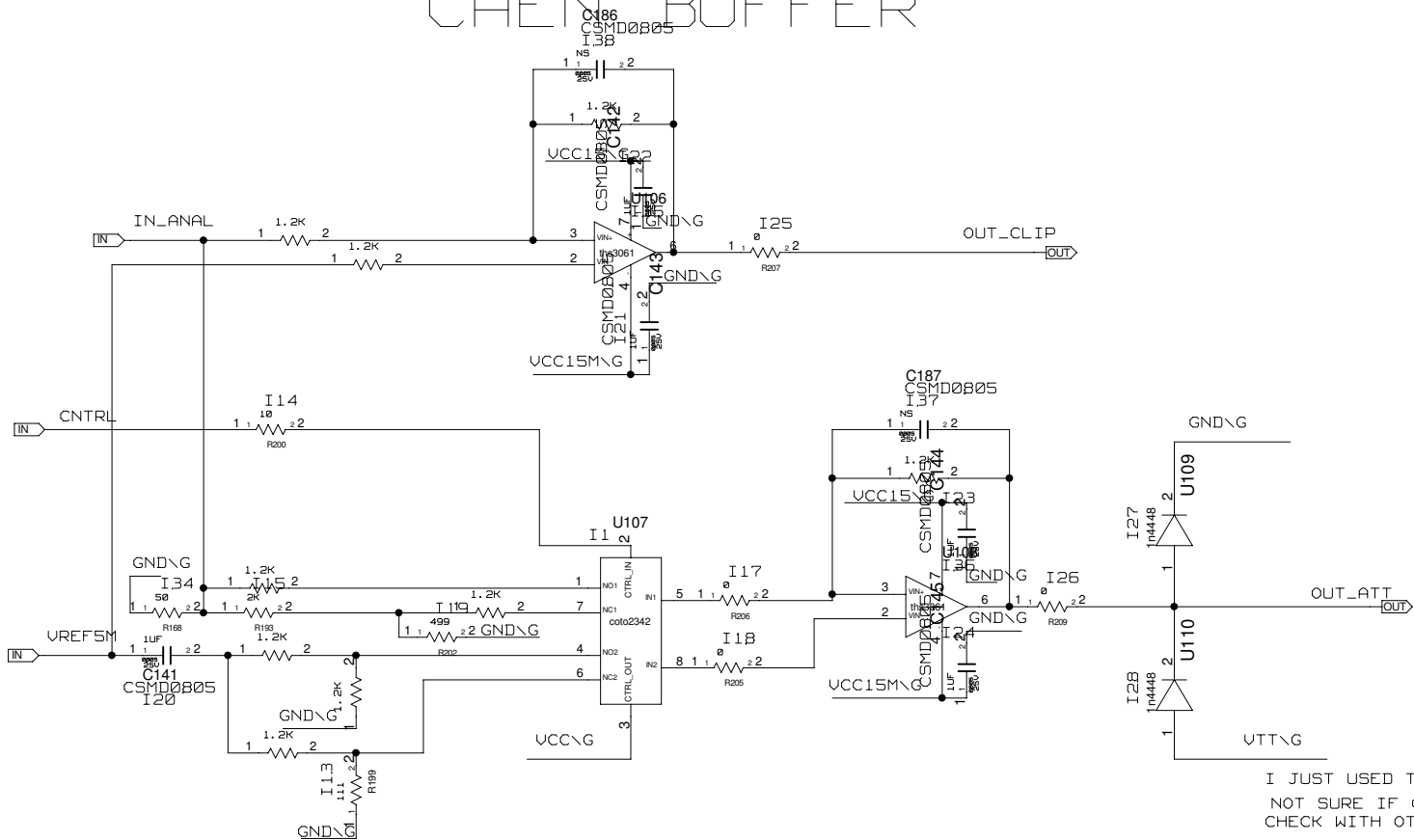
ENGINEER:

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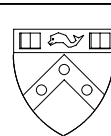
CAEN COMMS



CAEN BUFFER



I JUST USED THIS FOR A -2V VALUE
NOT SURE IF GOOD IDEA.
CHECK WITH OTHER PEOPLE LATER

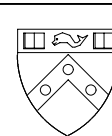
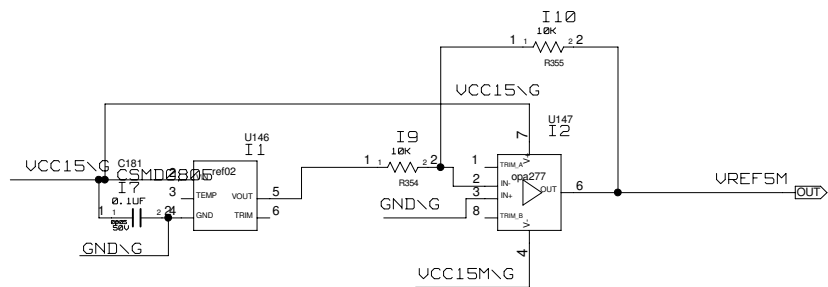


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VREF

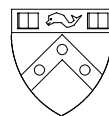
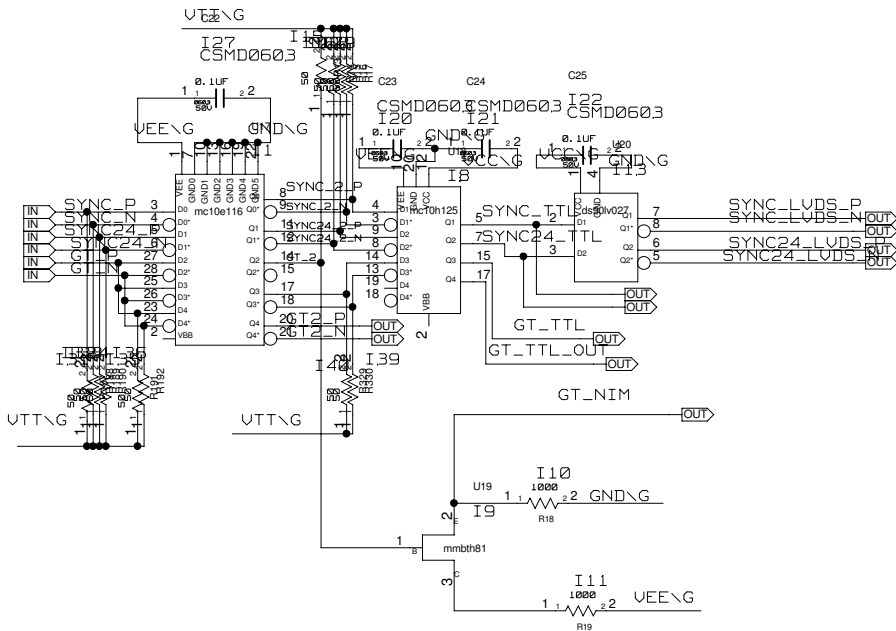
MAKE SURE THESE ARE PRECISION 10K RESISTORS



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CAEN DIGITAL COMMS

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HIGH ENERGY PHYSICS

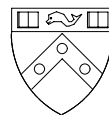
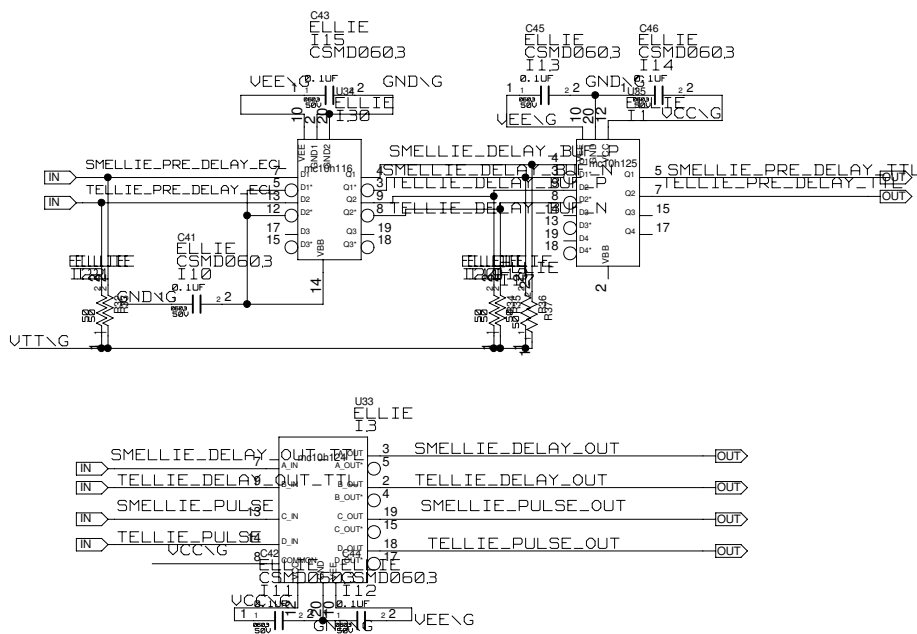
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DATE:

ENGINEER:

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ELLIE COMMS

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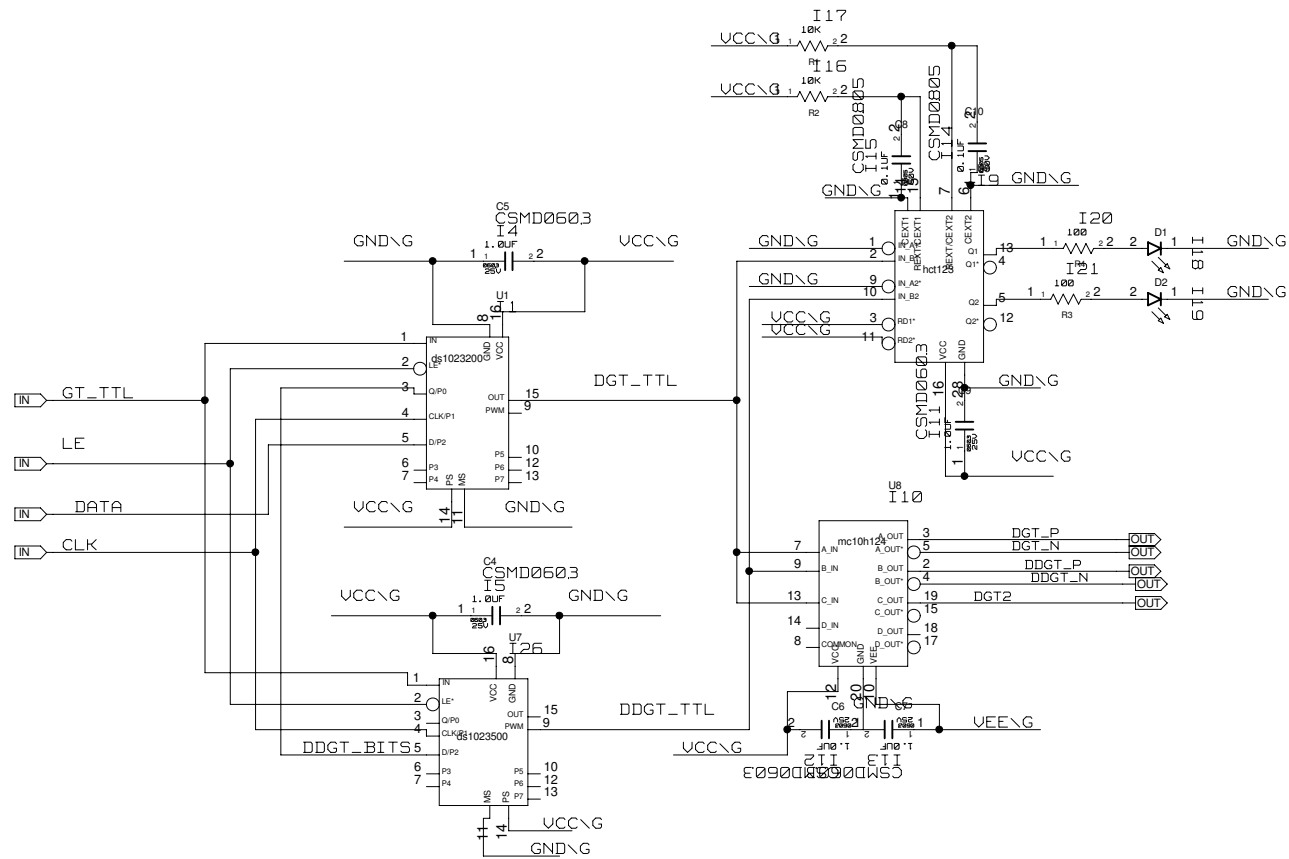
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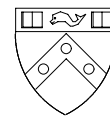
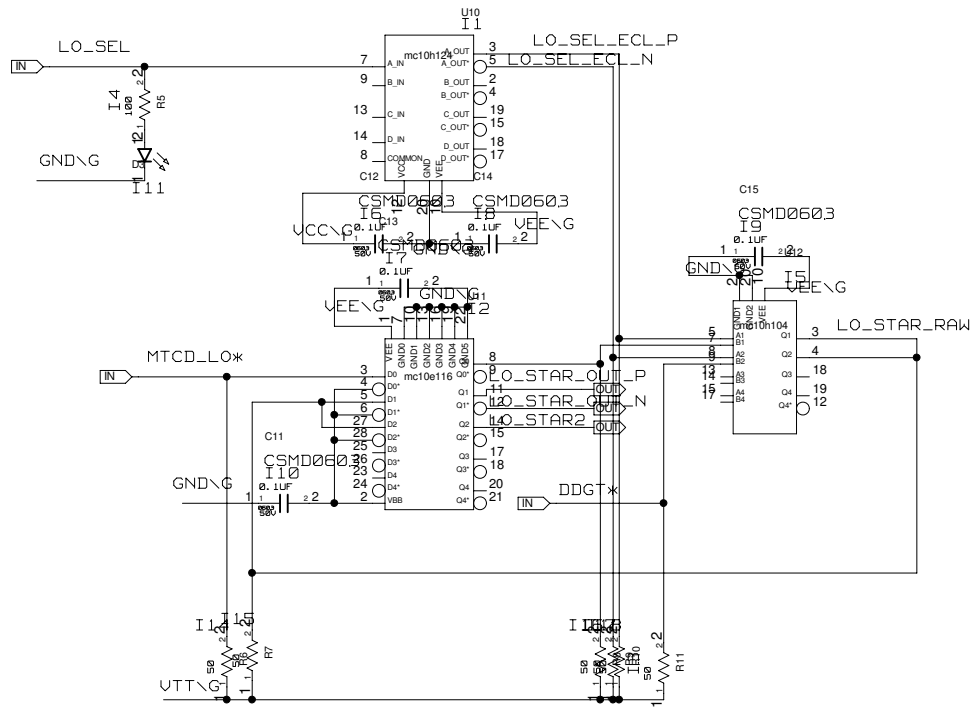
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GLOBAL TRIGGER DELAYS



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SELECT LOCKOUT SOURCE



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TITLE:

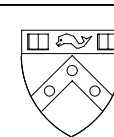
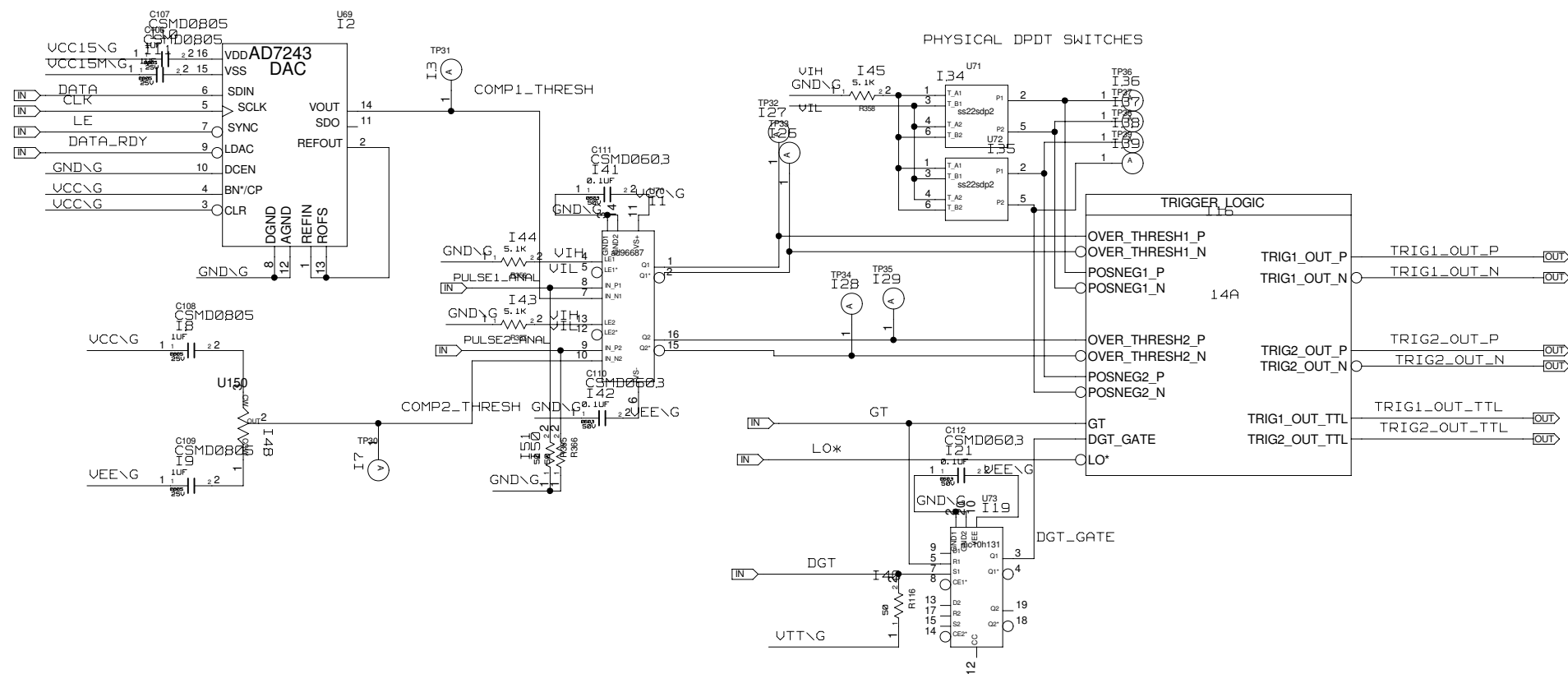
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1.3B

MTCA_MIMIC

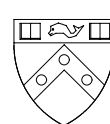
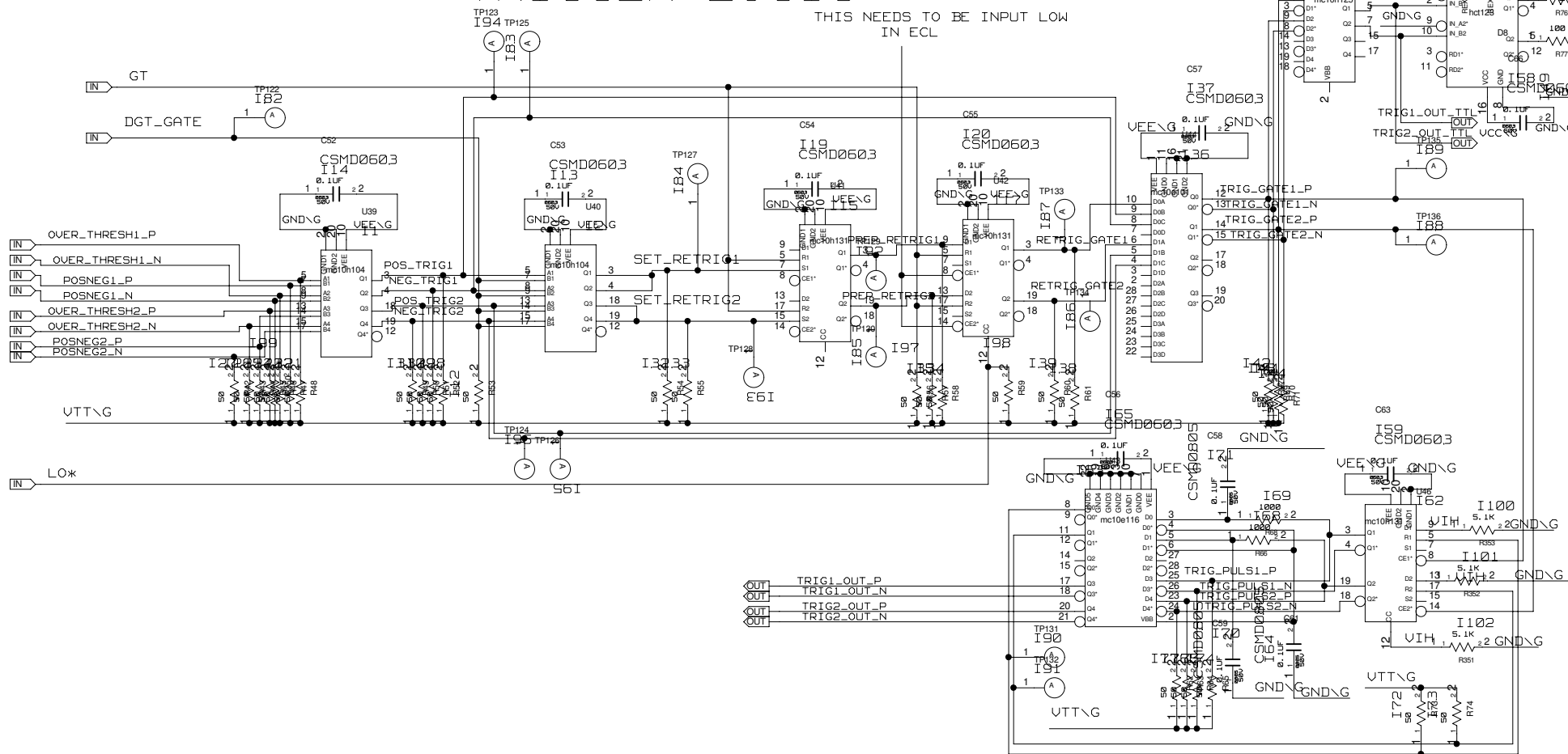


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HIGH ENERGY PHYSICS

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MTCA_MIMIC TRIGGER LOGIC

THIS NEEDS TO BE INPUT LOW
IN ECL

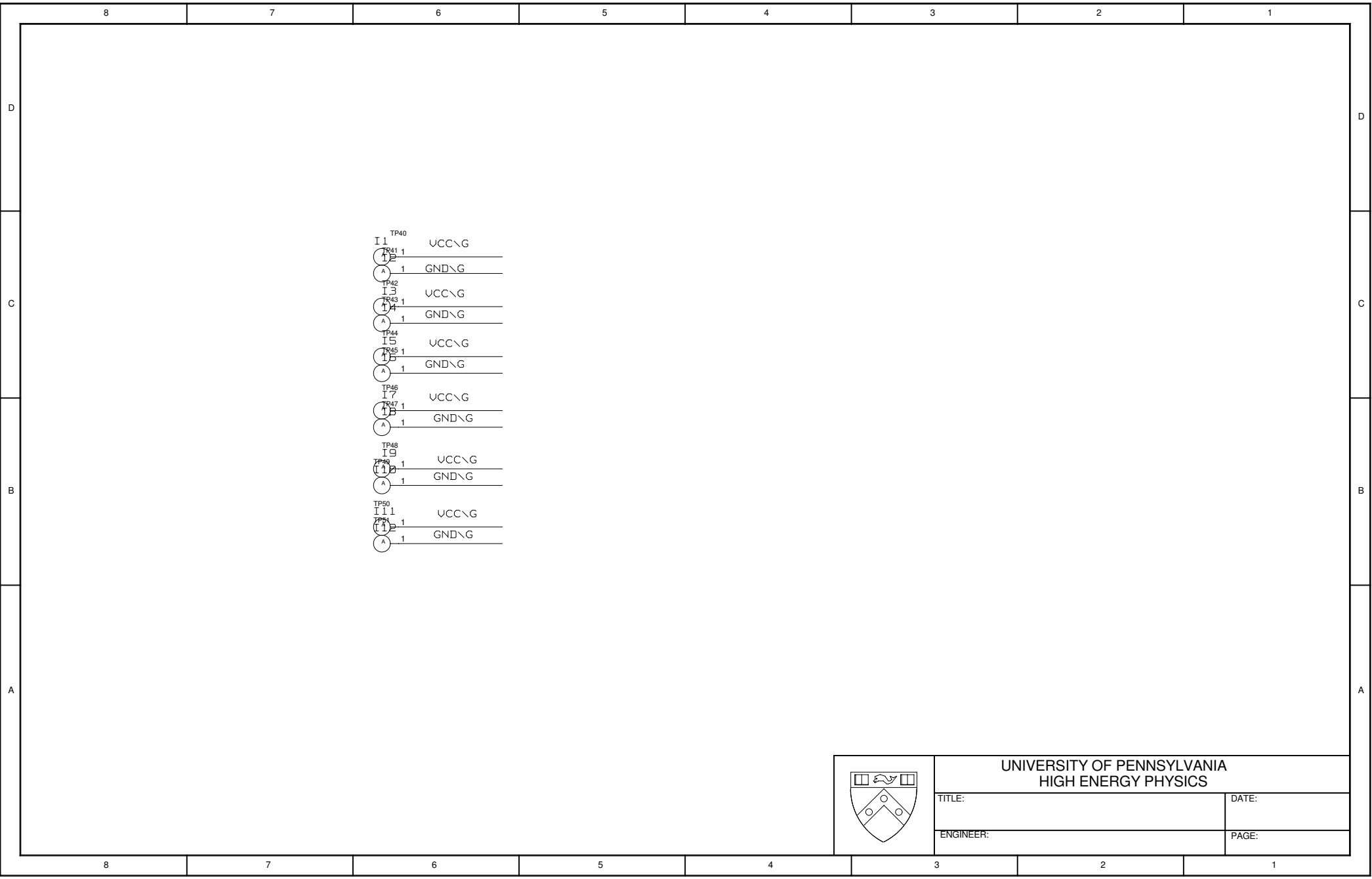
UNIVERSITY OF PENNSYLVANIA
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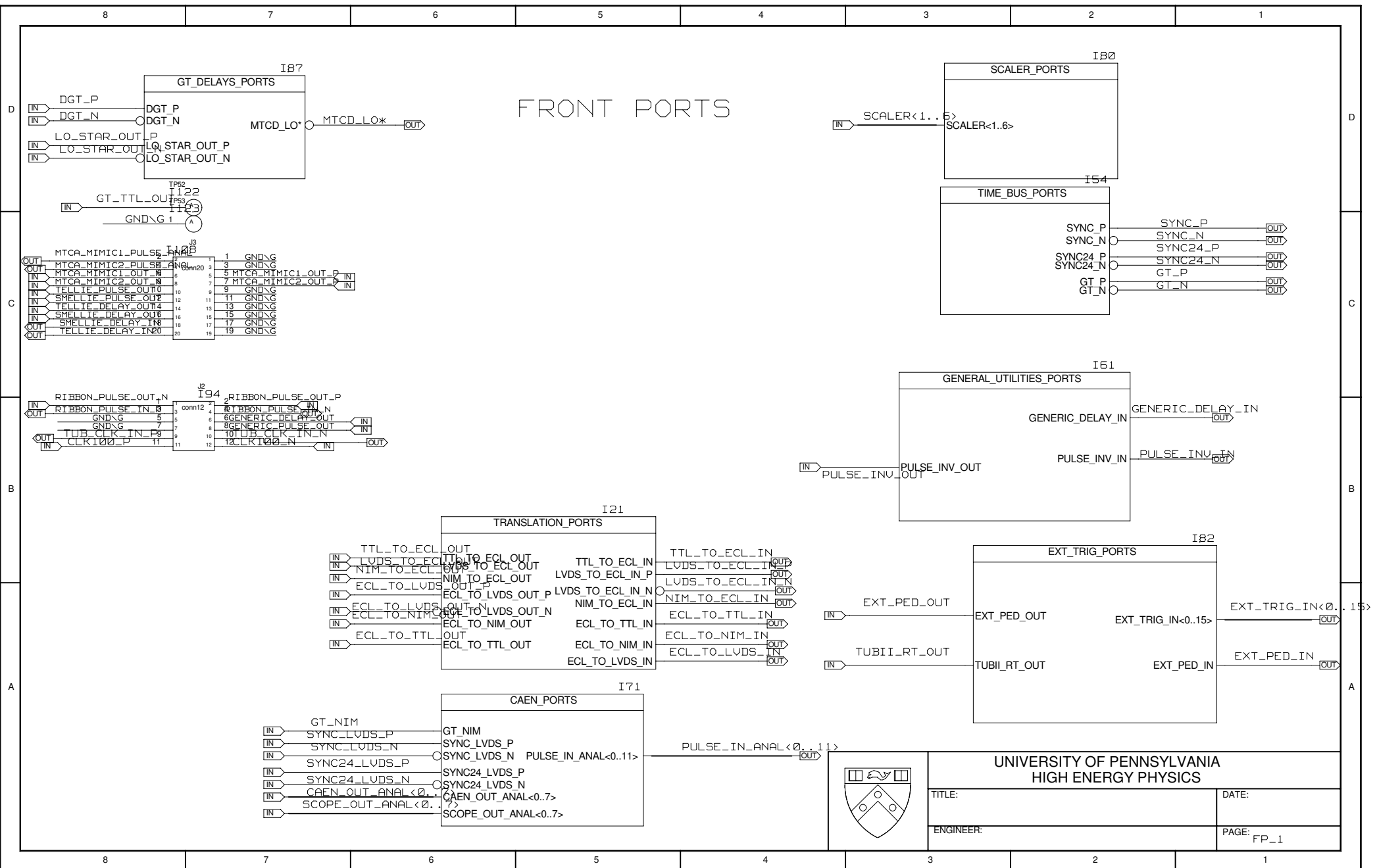
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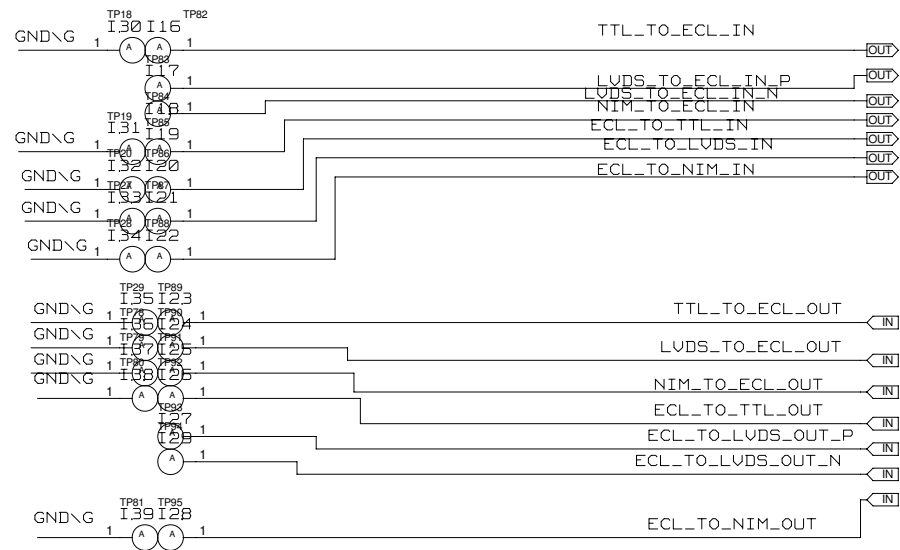
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TRANSLATION PORTS



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TIME BUS PORTS

The diagram shows the timing of various signals over 10 clock cycles. The signals are:

- GT_P (Output)
- GT_N (Output)
- SYNC_P (Output)
- SYNC_N (Output)
- SYNC24_P (Output)
- SYNC24_N (Output)

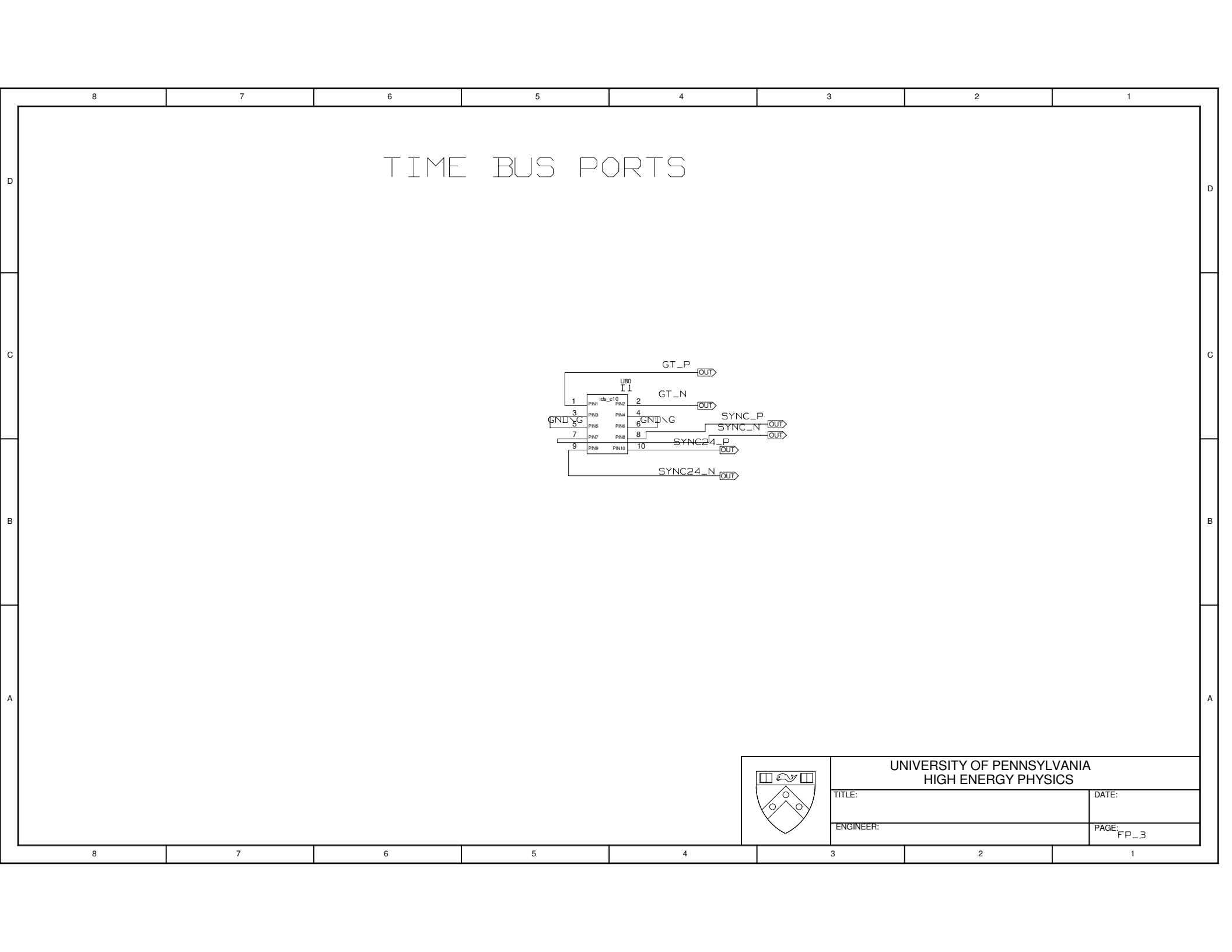
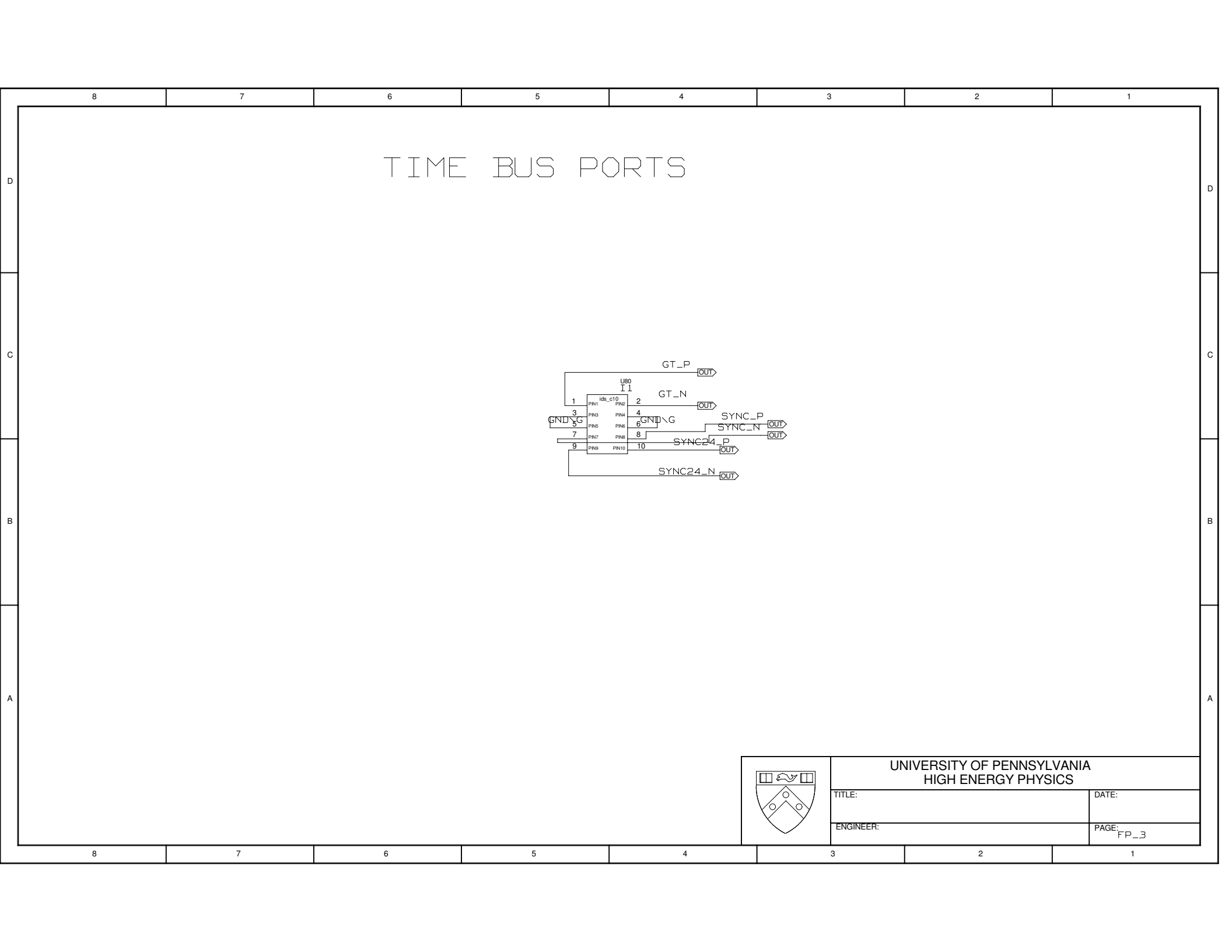
The clock signal is represented by a square wave. The ground signal is represented by a low level. The signals are labeled with their respective pins: GT_P (PIN1), GT_N (PIN2), SYNC_P (PIN3), SYNC_N (PIN4), SYNC24_P (PIN5), and SYNC24_N (PIN6).

Signal	Pin	Output
GT_P	PIN1	OUT
GT_N	PIN2	OUT
SYNC_P	PIN3	OUT
SYNC_N	PIN4	OUT
SYNC24_P	PIN5	OUT
SYNC24_N	PIN6	OUT

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[illegible][illegible]

TIME BUS PORTS

U80

1 2 3 4 5 6 7 8 9 10

GT_P OUT

GT_N OUT

SYNC_P OUT

SYNC_N OUT

SYNC24_P OUT

SYNC24_N OUT

GND

GND

GND

GND

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TIME BUS PORTS

U80

1 2 3 4 5 6 7 8 9 10

GT_P OUT

GT_N OUT

SYNC_P OUT

SYNC_N OUT

SYNC24_P OUT

SYNC24_N OUT

GND

GND

GND

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TITLE:	DATE:
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TIME BUS PORTS

U80

1 2 3 4 5 6 7 8 9 10

GT_P OUT

GT_N OUT

SYNC_P OUT

SYNC_N OUT

SYNC24_P OUT

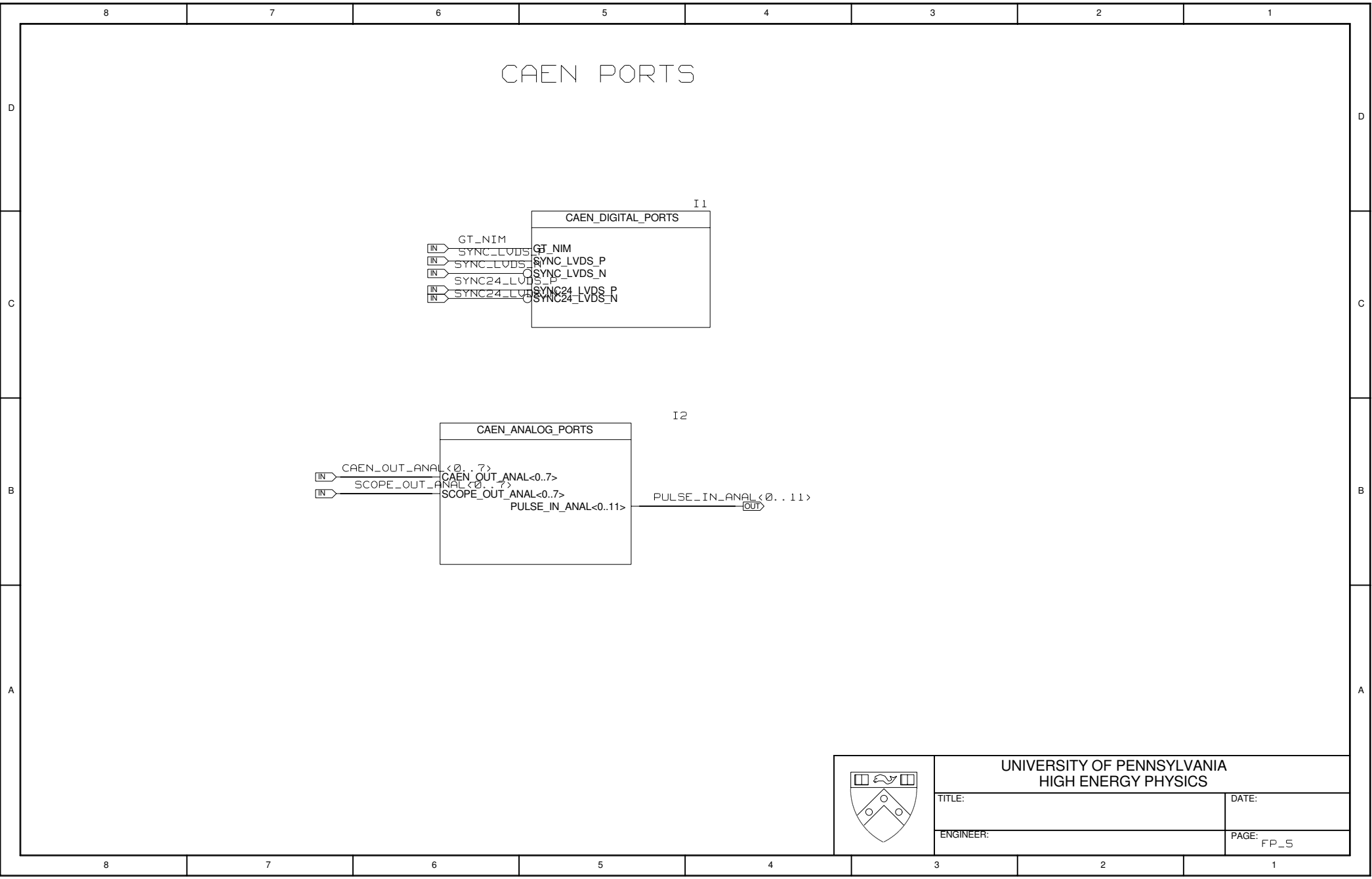
SYNC24_N OUT

GND

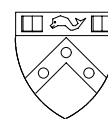
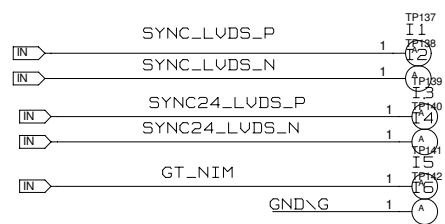
GND

GND

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CAEN DIGITAL PORTS



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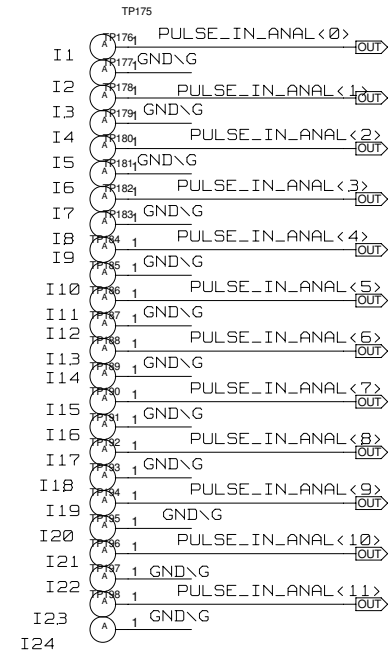
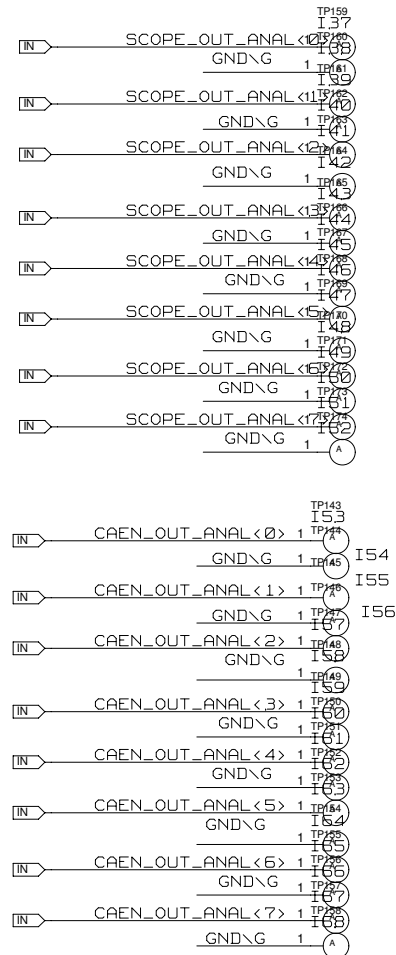
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DATE:

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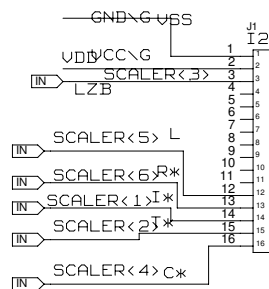
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CAEN ANALOG PORTS



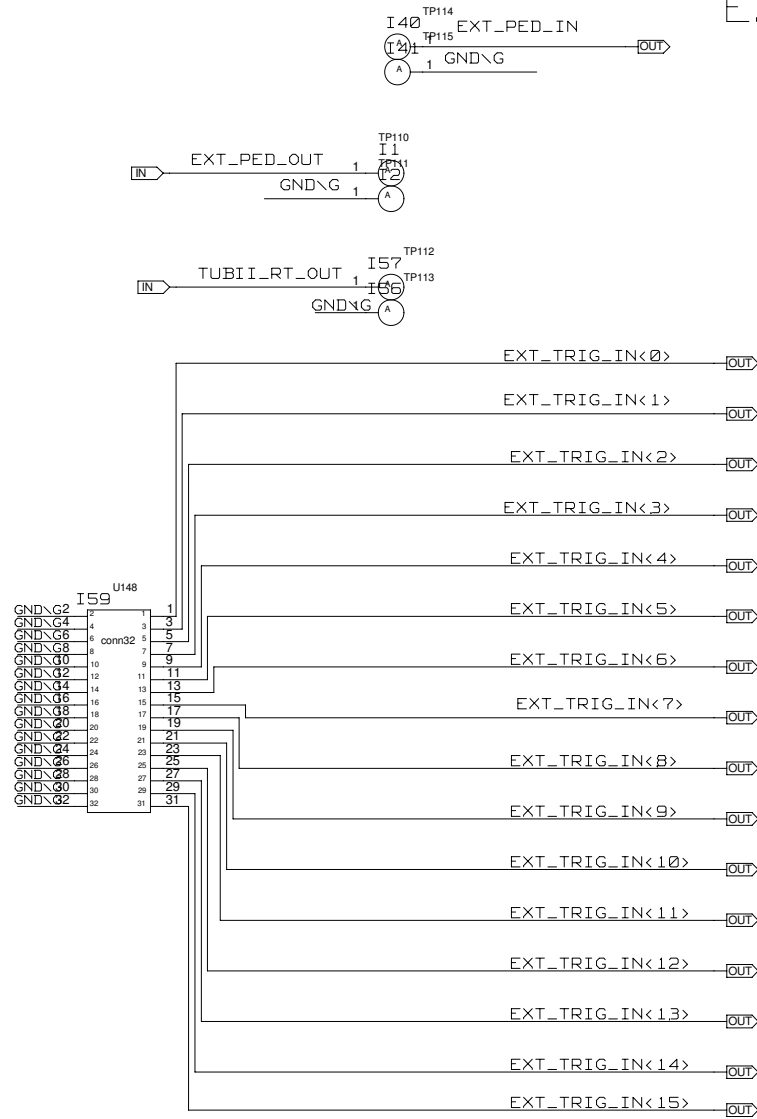
	UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
	TITLE:	DATE:
	ENGINEER:	PAGE:FP_5B


SCALER PORTS



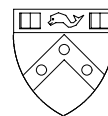
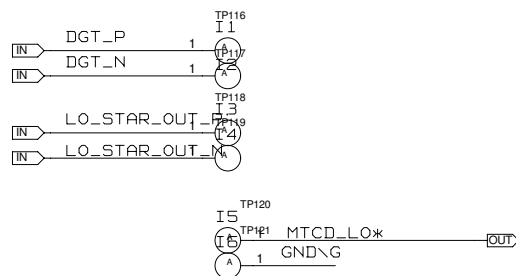
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EXTERNAL TRIGGERS PORTS



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GT DELAYS PORTS

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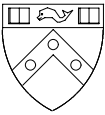
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8	7	6	5	4	3	2	1
BACK PORTS							
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

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