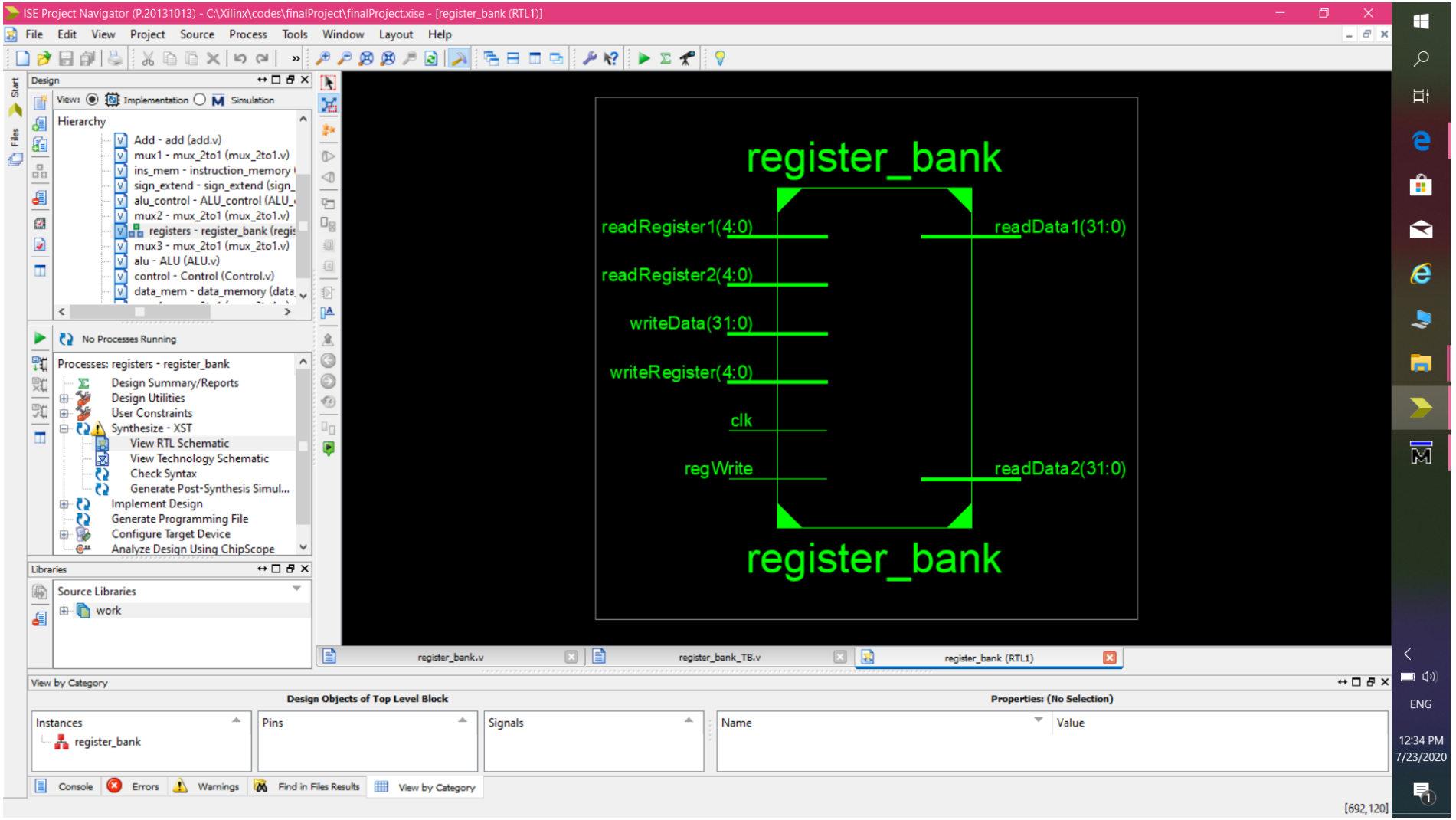
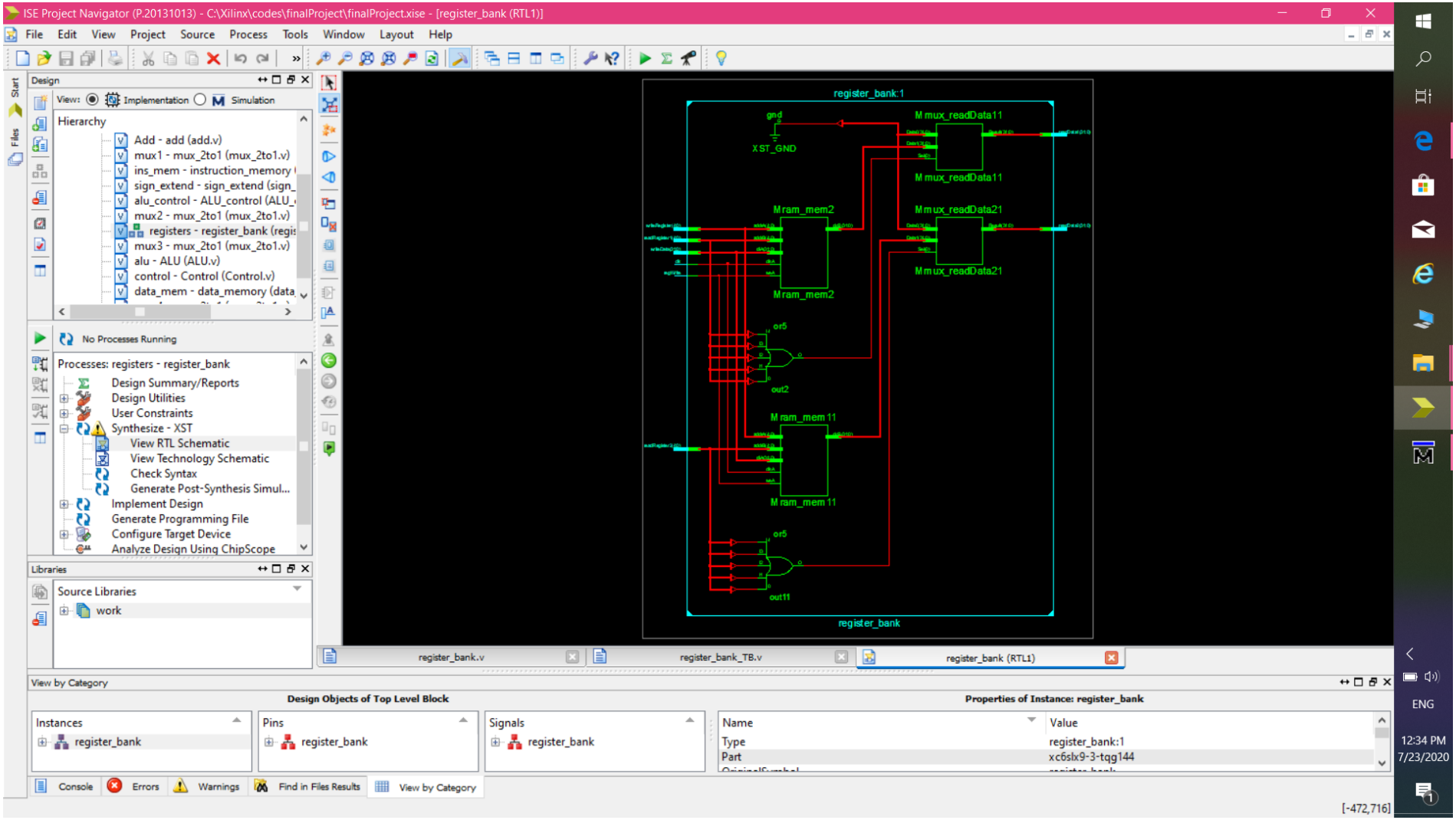

ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [register_bank (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Add - add (add.v)
mux1 - mux_2to1 (mux_2to1.v)
ins_mem - instruction_memory
sign_extend - sign_extend (sign_
alu_control - ALU_control (ALU_
mux2 - mux_2to1 (mux_2to1.v)
registers - register_bank (regis
mux3 - mux_2to1 (mux_2to1.v)
alu - ALU (ALU.v)
control - Control (Control.v)
data_mem - data_memory (data
No Processes Running
Processes: registers - register_bank
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simul...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Libraries
Source Libraries
work
register_bank
readRegister1(4:0)
readRegister2(4:0)
writeData(31:0)
writeRegister(4:0)
clk
regWrite
readData1(31:0)
readData2(31:0)
register_bank
register_bank.v
register_bank_TB.v
register_bank (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
register_bank
Pins
Signals
Name
Value
Console
Errors
Warnings
Find in Files Results
View by Category
[692,120]
ENG
12:34 PM
7/23/2020


ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [register_bank (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Add - add (add.v)
mux1 - mux_2to1 (mux_2to1.v)
ins_mem - instruction_memory
sign_extend - sign_extend (sign_
alu_control - ALU_control (ALU_
mux2 - mux_2to1 (mux_2to1.v)
registers - register_bank (regis
mux3 - mux_2to1 (mux_2to1.v)
alu - ALU (ALU.v)
control - Control (Control.v)
data_mem - data_memory (data
No Processes Running
Processes: registers - register_bank
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simul...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Libraries
Source Libraries
work
register_bank:1
gnd
XST_GND
Mmux_readData11
Mmux_readData11
Mmux_readData21
Mmux_readData21
Mram_mem2
Mram_mem2
or5
out2
Mram_mem11
Mram_mem11
or5
out11
register_bank
register_bank.v
register_bank_TB.v
register_bank (RTL1)
View by Category
Design Objects of Top Level Block
Instances
register_bank
Pins
register_bank
Signals
register_bank
Properties of Instance: register_bank
Name
Value
Type
register_bank:1
Part
xc6slx9-3-tqg144
Console
Errors
Warnings
Find in Files Results
View by Category
[-472,716]
ENG
12:34 PM
7/23/2020