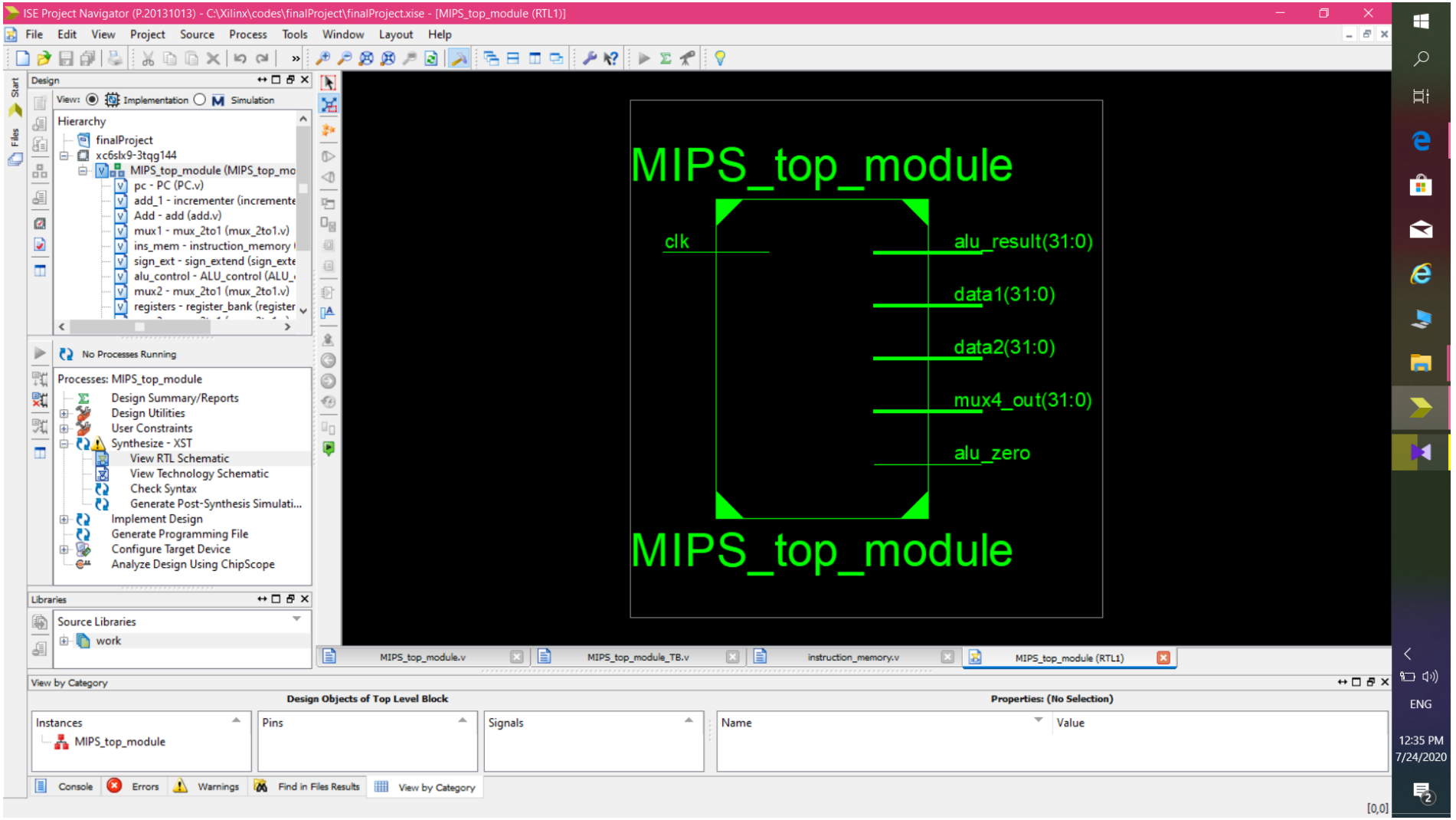
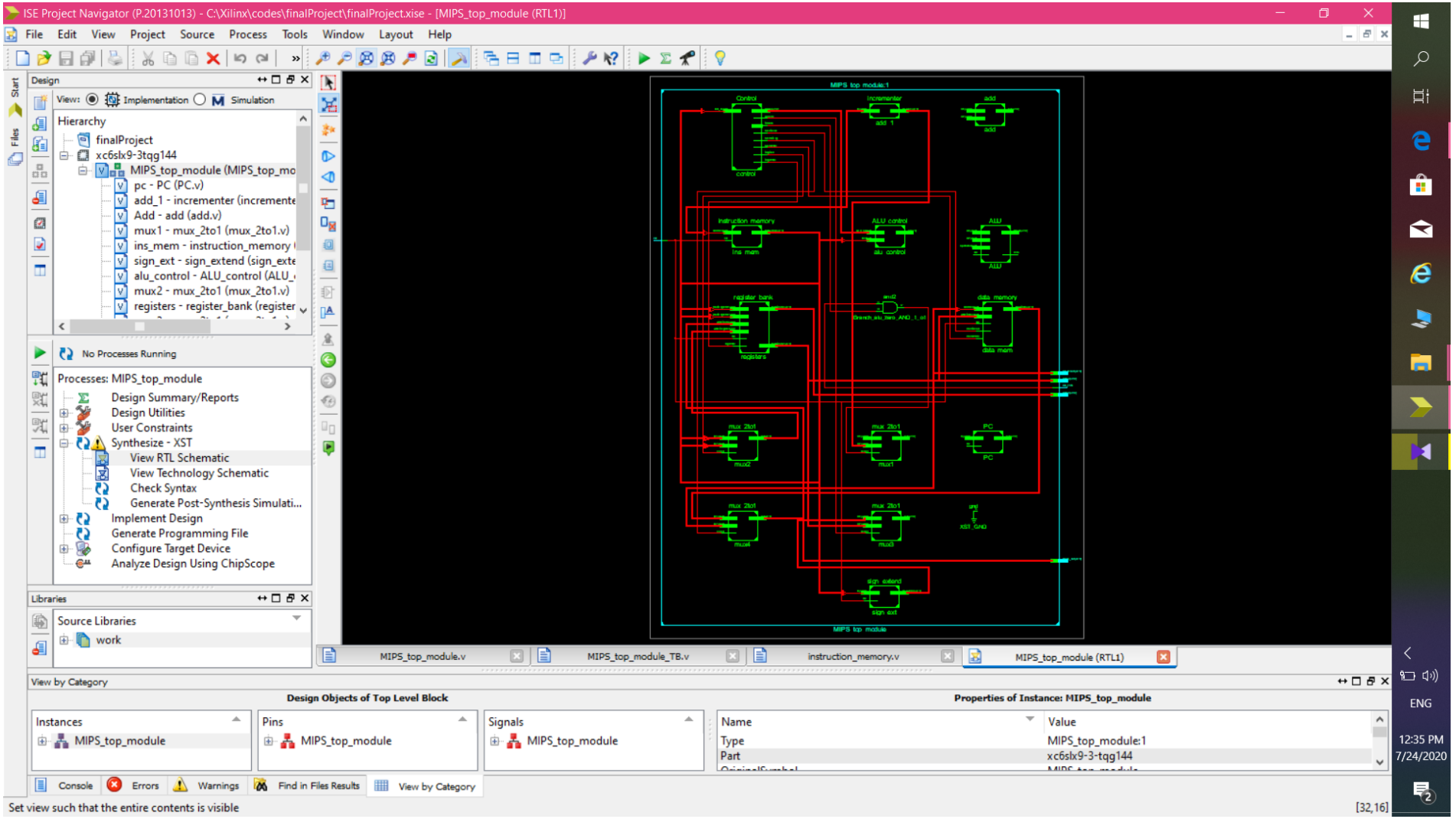

ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [MIPS_top_module (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
finalProject
xc6slx9-3tqg144
MIPS_top_module (MIPS_top_mo
pc - PC (PC.v)
add_1 - incrementer (incremente
Add - add (add.v)
mux1 - mux_2to1 (mux_2to1.v)
ins_mem - instruction_memory
sign_ext - sign_extend (sign_exte
alu_control - ALU_control (ALU_
mux2 - mux_2to1 (mux_2to1.v)
registers - register_bank (register
No Processes Running
Processes: MIPS_top_module
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulati...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Libraries
Source Libraries
work
MIPS_top_module
clk
alu_result(31:0)
data1(31:0)
data2(31:0)
mux4_out(31:0)
alu_zero
MIPS_top_module
MIPS_top_module.v
MIPS_top_module_TB.v
instruction_memory.v
MIPS_top_module (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
MIPS_top_module
Pins
Signals
Name
Value
Console
Errors
Warnings
Find in Files Results
View by Category
[0,0]
ENG
12:35 PM
7/24/2020


ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [MIPS_top_module (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
finalProject
xc6slx9-3tqg144
MIPS_top_module (MIPS_top_mo
pc - PC (PC.v)
add_1 - incrementer (incremente
Add - add (add.v)
mux1 - mux_2to1 (mux_2to1.v)
ins_mem - instruction_memory
sign_ext - sign_extend (sign_exte
alu_control - ALU_control (ALU_
mux2 - mux_2to1 (mux_2to1.v)
registers - register_bank (register
No Processes Running
Processes: MIPS_top_module
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulati...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Libraries
Source Libraries
work
MIPS top module:1
Control
incrementer
add
instruction memory
ALU control
ALU
register bank
data memory
mux 2to1
PC
sign extend
MIPS top module
MIPS_top_module.v
MIPS_top_module_TB.v
instruction_memory.v
MIPS_top_module (RTL1)
View by Category
Design Objects of Top Level Block
Instances
MIPS_top_module
Pins
MIPS_top_module
Signals
MIPS_top_module
Properties of Instance: MIPS_top_module
Name
Value
Type
MIPS_top_module:1
Part
xc6slx9-3-tqg144
Console
Errors
Warnings
Find in Files Results
View by Category
Set view such that the entire contents is visible
[32,16]
ENG
12:35 PM
7/24/2020