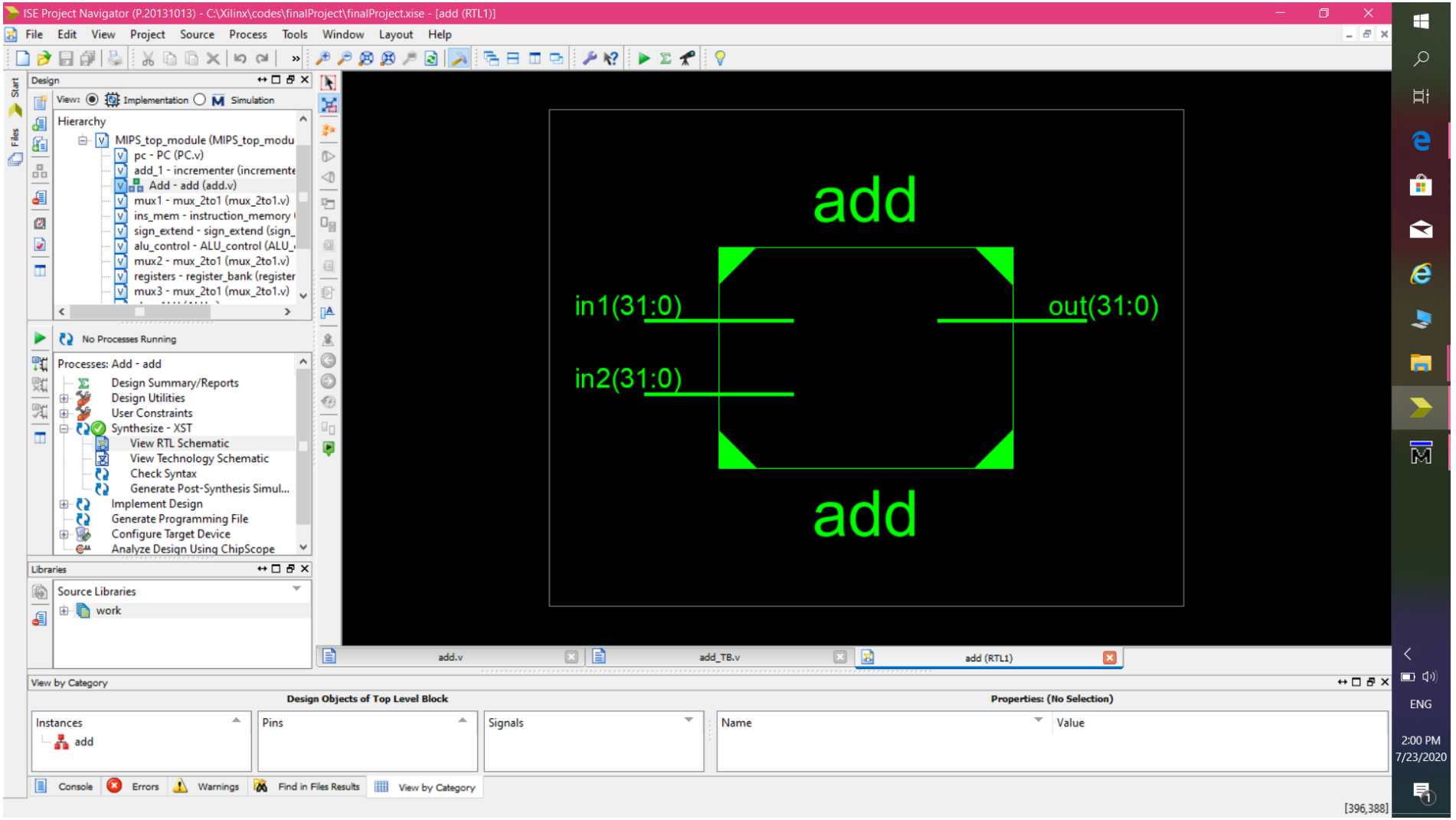
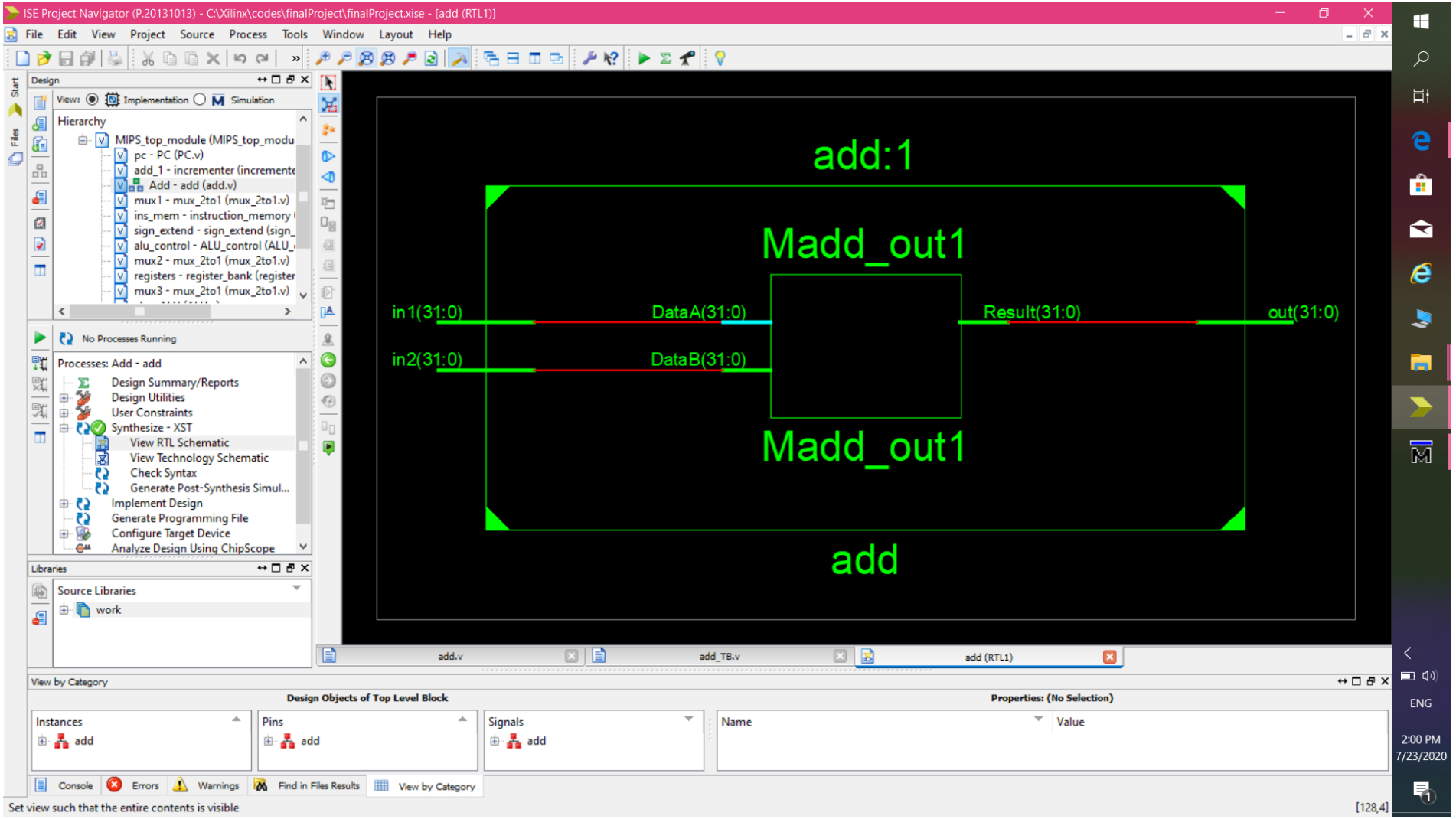

ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [add (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
MIPS_top_module (MIPS_top_modu
pc - PC (PC.v)
add_1 - incrementer (incremente
Add - add (add.v)
mux1 - mux_2to1 (mux_2to1.v)
ins_mem - instruction_memory
sign_extend - sign_extend (sign_
alu_control - ALU_control (ALU_
mux2 - mux_2to1 (mux_2to1.v)
registers - register_bank (register
mux3 - mux_2to1 (mux_2to1.v)
No Processes Running
Processes: Add - add
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simul...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Libraries
Source Libraries
work
add
in1(31:0)
in2(31:0)
out(31:0)
add
add.v
add_TB.v
add (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
add
Pins
Signals
Name
Value
Console
Errors
Warnings
Find in Files Results
View by Category
[396,388]
ENG
2:00 PM
7/23/2020


ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [add (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
MIPS_top_module (MIPS_top_modu
pc - PC (PC.v)
add_1 - incrementer (incremente
Add - add (add.v)
mux1 - mux_2to1 (mux_2to1.v)
ins_mem - instruction_memory
sign_extend - sign_extend (sign_
alu_control - ALU_control (ALU_
mux2 - mux_2to1 (mux_2to1.v)
registers - register_bank (register
mux3 - mux_2to1 (mux_2to1.v)
No Processes Running
Processes: Add - add
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simul...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Libraries
Source Libraries
work
add:1
Madd_out1
in1(31:0)
DataA(31:0)
Result(31:0)
out(31:0)
in2(31:0)
DataB(31:0)
Madd_out1
add
add.v
add_TB.v
add (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
add
Pins
add
Signals
add
Name
Value
Console
Errors
Warnings
Find in Files Results
View by Category
Set view such that the entire contents is visible
[128,4]
ENG
2:00 PM
7/23/2020