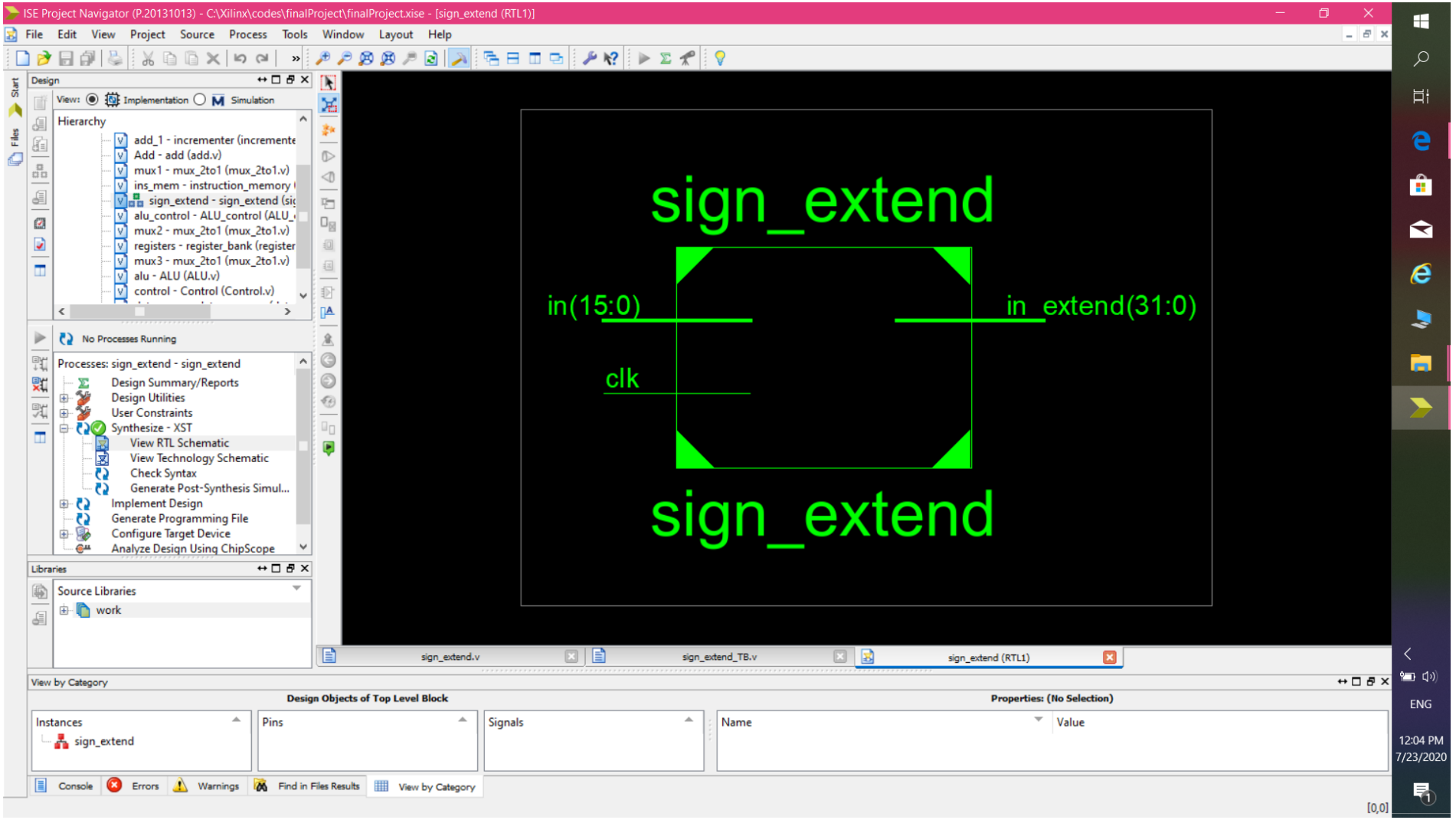
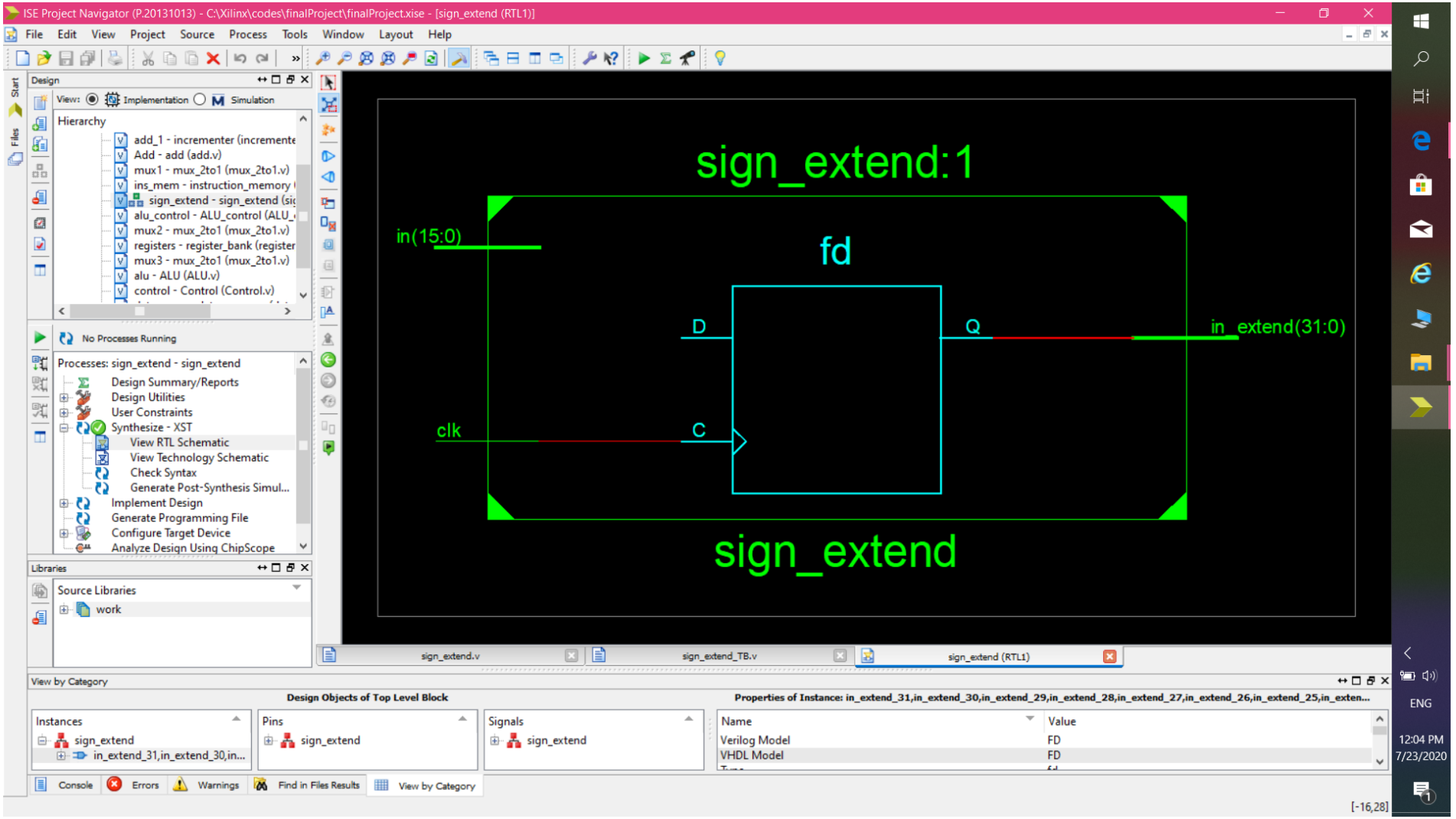

ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [sign_extend (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
add_1 - incrementer (incremente
Add - add (add.v)
mux1 - mux_2to1 (mux_2to1.v)
ins_mem - instruction_memory
sign_extend - sign_extend (sig
alu_control - ALU_control (ALU_
mux2 - mux_2to1 (mux_2to1.v)
registers - register_bank (register
mux3 - mux_2to1 (mux_2to1.v)
alu - ALU (ALU.v)
control - Control (Control.v)
No Processes Running
Processes: sign_extend - sign_extend
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simul...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Libraries
Source Libraries
work
sign_extend
in(15:0)
in_extend(31:0)
clk
sign_extend
sign_extend.v
sign_extend_TB.v
sign_extend (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
sign_extend
Pins
Signals
Name
Value
Console
Errors
Warnings
Find in Files Results
View by Category
[0,0]
ENG
12:04 PM
7/23/2020


ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [sign_extend (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
add_1 - incrementer (incremente
Add - add (add.v)
mux1 - mux_2to1 (mux_2to1.v)
ins_mem - instruction_memory
sign_extend - sign_extend (sig
alu_control - ALU_control (ALU_
mux2 - mux_2to1 (mux_2to1.v)
registers - register_bank (register
mux3 - mux_2to1 (mux_2to1.v)
alu - ALU (ALU.v)
control - Control (Control.v)
No Processes Running
Processes: sign_extend - sign_extend
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simul...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Libraries
Source Libraries
work
sign_extend:1
in(15:0)
fd
D
Q
in_extend(31:0)
clk
C
sign_extend
sign_extend.v
sign_extend_TB.v
sign_extend (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Instance: in_extend_31,in_extend_30,in_extend_29,in_extend_28,in_extend_27,in_extend_26,in_extend_25,in_exten...
Instances
sign_extend
in_extend_31,in_extend_30,in...
Pins
sign_extend
Signals
sign_extend
Name
Value
Verilog Model
FD
VHDL Model
FD
Console
Errors
Warnings
Find in Files Results
View by Category
[-16,28]
ENG
12:04 PM
7/23/2020