

ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [ALU (RTL1)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- mux1 - mux_2to1 (mux_2to1.v)
- ins_mem - instruction_memory
- sign_extend - sign_extend (sign_
- alu_control - ALU_control (ALU_
- mux2 - mux_2to1 (mux_2to1.v)
- registers - register_bank (register
- mux3 - mux_2to1 (mux_2to1.v)
- alu - ALU (ALU.v)
- control - Control (Control.v)
- data_mem - data_memory (data
- mem4 - mux_2to1 (mux_2to1.v)

No Processes Running

Processes: alu - ALU

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
 - View RTL Schematic
 - View Technology Schematic
 - Check Syntax
 - Generate Post-Synthesis Simul...
- Implement Design
 - Generate Programming File
 - Configure Target Device

Libraries

Source Libraries

- work

View by Category

Design Objects of Top Level Block

Instances	Pins	Signals	Name	Value
ALU				

Properties: (No Selection)

Console Errors Warnings Find in Files Results View by Category

ALU

in1(31:0)

in2(31:0)

operation(3:0)

clk

result(31:0)

zero

ALU

ALU.v ALU_TB.v ALU (RTL1)

[0,0]

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No Processes Running

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ALU.v ALU_TB.v ALU (RTL1)

Design Objects of Top Level Block

Instances

- ALU

Pins

- ALU

Signals

- ALU

Properties of Instance: ALU

Name	Value
Type	ALU:1
Part	xc6slx9-3-tqg144
Original Symbol	ALU

Console Errors Warnings Find in Files Results View by Category

[412,1980]