

ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [MIPS_top_module (RTL4)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- finalProject
 - xc6slx9-3tqg144
 - MIPS_top_module (MIPS_top_mo
 - pc - PC (PC.v)
 - add_1 - incrementer (incremente
 - Add - add (add.v)
 - mux1 - mux_2to1 (mux_2to1.v)
 - ins_mem - instruction_memory
 - sign_ext - sign_extend (sign_exte
 - alu_control - ALU_control (ALU_
 - mux2 - mux_2to1 (mux_2to1.v)
 - registers - register_bank (register

No Processes Running

Processes: MIPS_top_module

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
 - View RTL Schematic
 - View Technology Schematic
 - Check Syntax
 - Generate Post-Synthesis Simulati...
- Implement Design
 - Generate Programming File
 - Configure Target Device
 - Analyze Design Using ChipScope

Libraries

Source Libraries

- work

View by Category

Design Objects of Top Level Block

Instances	Pins	Signals	Name	Value
MIPS_top_module				

Properties: (No Selection)

Console Errors Warnings Find in Files Results View by Category

[212,472]

MIPS_top_module

clk

alu_result(31:0)

data1(31:0)

data2(31:0)

ins(31:0)

pc_in(31:0)

alu_zero

MIPS_top_module

MIPS_top_module.v MIPS_top_module_TB.v instruction_memory.v data_memory.v MIPS_top_module (RTL4)

ENG

5:03 PM

7/24/2020

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View by Category

Design Objects of Top Level Block

Instances

- MIPS_top_module

Pins

- MIPS_top_module

Signals

- MIPS_top_module

Properties of Instance: MIPS_top_module

Name	Value
Type	MIPS_top_module:1
Part	xc6slx9-3-tqg144
OriginalSymbol	MIPS_top_module

Console Errors Warnings Find in Files Results View by Category

[4608,1092]