

ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [PC (RTL1)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- finalProject
 - xc6slx9-3tqg144
 - MIPS_top_module (MIPS_top_modu
 - pc - PC (PC.v)
 - add_1 - incrementer (incremente
 - Add - add (add.v)
 - mux1 - mux_2to1 (mux_2to1.v)
 - ins_mem - instruction_memory
 - sign_extend - sign_extend (sign_
 - alu_control - ALU_control (ALU_
 - mux2 - mux_2to1 (mux_2to1.v)

No Processes Running

Processes: pc - PC

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
 - View RTL Schematic
 - View Technology Schematic
 - Check Syntax
 - Generate Post-Synthesis Simul...
- Implement Design
- Generate Programming File
- Configure Target Device

Libraries

Source Libraries

- work

View by Category

Design Objects of Top Level Block

Instances

- PC

Pins

Signals

Name

Value

Properties: (No Selection)

PC

in(31:0)

clk

out(31:0)

PC

PC.v PC_TB.v PC (RTL1)

Console Errors Warnings Find in Files Results View by Category

[424,456]

Design

View: ☒ Implementation ☐ Simulation

Hierarchy

- finalProject
 - xc6slx9-3tqg144
 - MIPS_top_module (MIPS_top_modu
 - pc - PC (PC.v)
 - add_1 - incrementer (incremente
 - Add - add (add.v)
 - mux1 - mux_2to1 (mux_2to1.v)
 - ins_mem - instruction_memory
 - sign_extend - sign_extend (sign_
 - alu_control - ALU_control (ALU_
 - mux2 - mux_2to1 (mux_2to1.v)

No Processes Running

Processes: pc - PC

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
 - View RTL Schematic
 - View Technology Schematic
 - Check Syntax
 - Generate Post-Synthesis Simul...
- Implement Design
- Generate Programming File
- Configure Target Device

Libraries

Source Libraries

- work

View by Category

Design Objects of Top Level Block

Instances

- PC
- out_31,out_30,out_29,out_28,...

Pins

- PC

Signals

- PC

Properties of Instance: out_31,out_30,out_29,out_28,out_27,out_26,out_25,out_24,out_23,out_22,out_21,out_20,out_19,out_18,o...

Name	Value
Verilog Model	FD
VHDL Model	FD
T...	...

Set view such that the entire contents is visible

[96,0]