

ISE Project Navigator (P.20131013) - C:\Xilinx\codes\finalProject\finalProject.xise - [data_memory (RTL1)]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Hierarchy

- Add - add (add.v)
- mux1 - mux_2to1 (mux_2to1.v)
- ins_mem - instruction_memory
- sign_extend - sign_extend (sign_
- alu_control - ALU_control (ALU_
- mux2 - mux_2to1 (mux_2to1.v)
- registers - register_bank (register
- mux3 - mux_2to1 (mux_2to1.v)
- alu - ALU (ALU.v)
- control - Control (Control.v)
- data_mem - data_memory (d

No Processes Running

Processes: data_mem - data_memory

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
 - View RTL Schematic
 - View Technology Schematic
 - Check Syntax
 - Generate Post-Synthesis Simul...
- Implement Design
 - Generate Programming File
 - Configure Target Device
 - Analyze Design Using ChipScope

Libraries

Source Libraries

- work

View by Category

Design Objects of Top Level Block

Instances

- data_memory

Pins

Signals

Properties: (No Selection)

Name	Value
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Console Errors Warnings Find in Files Results View by Category

[332,648]

data_memory

address(6:0)

writeData(31:0)

clk

memRead

memWrite

readData(31:0)

data_memory

data_memory.v data_memory_TB.v data_memory (RTL1)

ENG

11:17 AM 7/23/2020

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data_memory.v data_memory_TB.v data_memory (RTL1)

Design Objects of Top Level Block

Instances

- data_memory

Pins

- data_memory

Signals

- data_memory

Properties of Instance: data_memory

Name	Value
Type	data_memory:1
Part	xc6slx9-3-tqg144
Original Symbol	data_memory

Console Errors Warnings Find in Files Results View by Category

[1940,2328]

The RTL schematic for the data_memory block shows a complex internal structure. It includes two multiplexers (Mmux_n00231) for reading and writing data, a memory block (Mram_mem1), and several logic gates (and2b2, or2, and2b1, and2, inv). The block is labeled 'data_memory' and 'data_memory:1'. The schematic is connected to external signals like 'writeData[31]', 'readData[31]', and 'idle'.