

ModelSim SE-64 10.6d

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

100 ps

Layout Simulate ColumnLayout Default

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Wave - Default

Instance	Path	Signal	Value
PC_TB	/PC_TB/dk	1'h0	
PC_TB	/PC_TB/in	32h00000000	00000000
PC_TB	/PC_TB/out	32h00000000	00000000
gbl	/gbl/GSR	1'h0	00000000

Now: 1000 ns
Cursor 1: 999.248 ns

Transcript

```
# Errors: 0, Warnings: 0
# Model Technology ModelSim SE-64 vlog 10.6d Compiler 2018.02 Feb 24 2018
# Start time: 19:29:39 on Jul 18, 2020
# vlog -reportprogress 300 C:/Xilinx/14.7/ISE_DS/ISE/verilog/src/glbl.v
# -- Compiling module glbl
#
# Top level modules:
#   glbl
# End time: 19:29:40 on Jul 18, 2020, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
# vsim -voptargs="" -t lps -L xilinxcorelib_ver -L unisims_ver -L unimacro_ver -L secureip -lib work work.PC_TB glbl
# Start time: 19:29:40 on Jul 18, 2020
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# Loading work.PC_TB(fast)
# Loading work.PC(fast)
# Loading work.glbl(fast)
# .main_pane.wave.interior.cs.body.pw.wf
# .main_pane.structure.interior.cs.body.struct
# .main_pane.objects.interior.cs.body.tree
VSIM 2>
```

Now: 1us Delta: 0 sim:/PC_TB 0 ps to 255253 ps Keep 0