

ModelSim SE-64 10.6d

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

100 ps

Layout Simulate ColumnLayout Default

Search:

Wave - Default

Instance	Msgs	
/data_memory_TB/clk	1'h0	
/data_memory_TB/address	7'h7d	
/data_memory_TB/memWrite	1'h1	
/data_memory_TB/memRead	1'h1	
/data_memory_TB/writeData	32'h00000000	
/data_memory_TB/readData	32'h00000000	
/gbl/GSR	1'h0	

Now: 1000 ns
Cursor 1: 999.45 ns

Transcript

```
# Errors: 0, Warnings: 0
# Model Technology ModelSim SE-64 vlog 10.6d Compiler 2018.02 Feb 24 2018
# Start time: 11:12:45 on Jul 23, 2020
# vlog -reportprogress 300 C:/Xilinx/14.7/ISE_DS/ISE/verilog/src/glbl.v
# -- Compiling module glbl
#
# Top level modules:
#   glbl
# End time: 11:12:45 on Jul 23, 2020, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# vsim -voptargs="" -acc -t lps -L xilinxcorelib_ver -L unisims_ver -L unimacro_ver -L secureip -lib work work.data_memory_TB glbl
# Start time: 11:12:45 on Jul 23, 2020
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# Loading work.data_memory_TB(fast)
# Loading work.data_memory_TB(fast)
# Loading work.glbl(fast)
# .main_pane.wave.interior.cs.body.pw.wf
# .main_pane.structure.interior.cs.body.struct
# .main_pane.objects.interior.cs.body.tree
VSIM 2>
```

Now: 1us Delta: 0 /data_memory_TB/memRead 0 ps to 457415 ps Keep 0