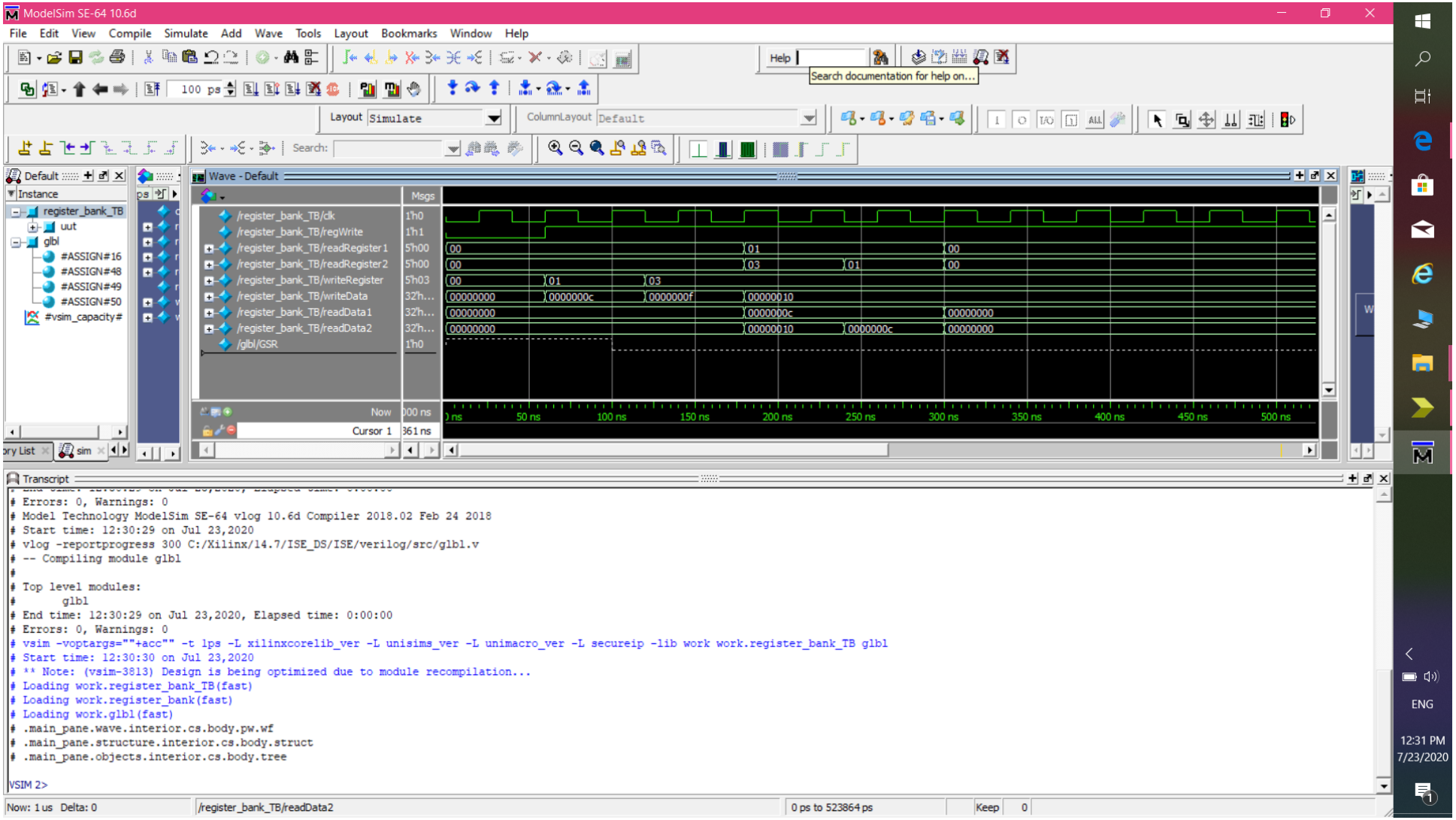
ModelSim SE-64 10.6d
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Search documentation for help on...
Wave - Default
/register_bank_TB/clk
/register_bank_TB/regWrite
/register_bank_TB/readRegister1
/register_bank_TB/readRegister2
/register_bank_TB/writeRegister
/register_bank_TB/writeData
/register_bank_TB/readData1
/register_bank_TB/readData2
/glbl/GSR
Cursor 1
50 ns 100 ns 150 ns 200 ns 250 ns 300 ns 350 ns 400 ns 450 ns 500 ns
Transcript
Errors: 0, Warnings: 0
Model Technology ModelSim SE-64 vlog 10.6d Compiler 2018.02 Feb 24 2018
Start time: 12:30:29 on Jul 23,2020
vlog -reportprogress 300 C:/Xilinx/14.7/ISE_DS/ISE/verilog/src/glbl.v
-- Compiling module glbl
Top level modules:
glbl
End time: 12:30:29 on Jul 23,2020, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vsim -voptargs=""+acc"" -t 1ps -L xilinxcorelib_ver -L unisims_ver -L unimacro_ver -L secureip -lib work work.register_bank_TB glbl
Start time: 12:30:30 on Jul 23,2020
** Note: (vsim-3813) Design is being optimized due to module recompilation...
Loading work.register_bank_TB(fast)
Loading work.register_bank(fast)
Loading work.glbl(fast)
.main_pane.wave.interior.cs.body.pw.wf
.main_pane.structure.interior.cs.body.struct
.main_pane.objects.interior.cs.body.tree
VSIM 2>
Now: 1 us Delta: 0
/register_bank_TB/readData2
0 ps to 523864 ps
Keep
ENG
12:31 PM
7/23/2020