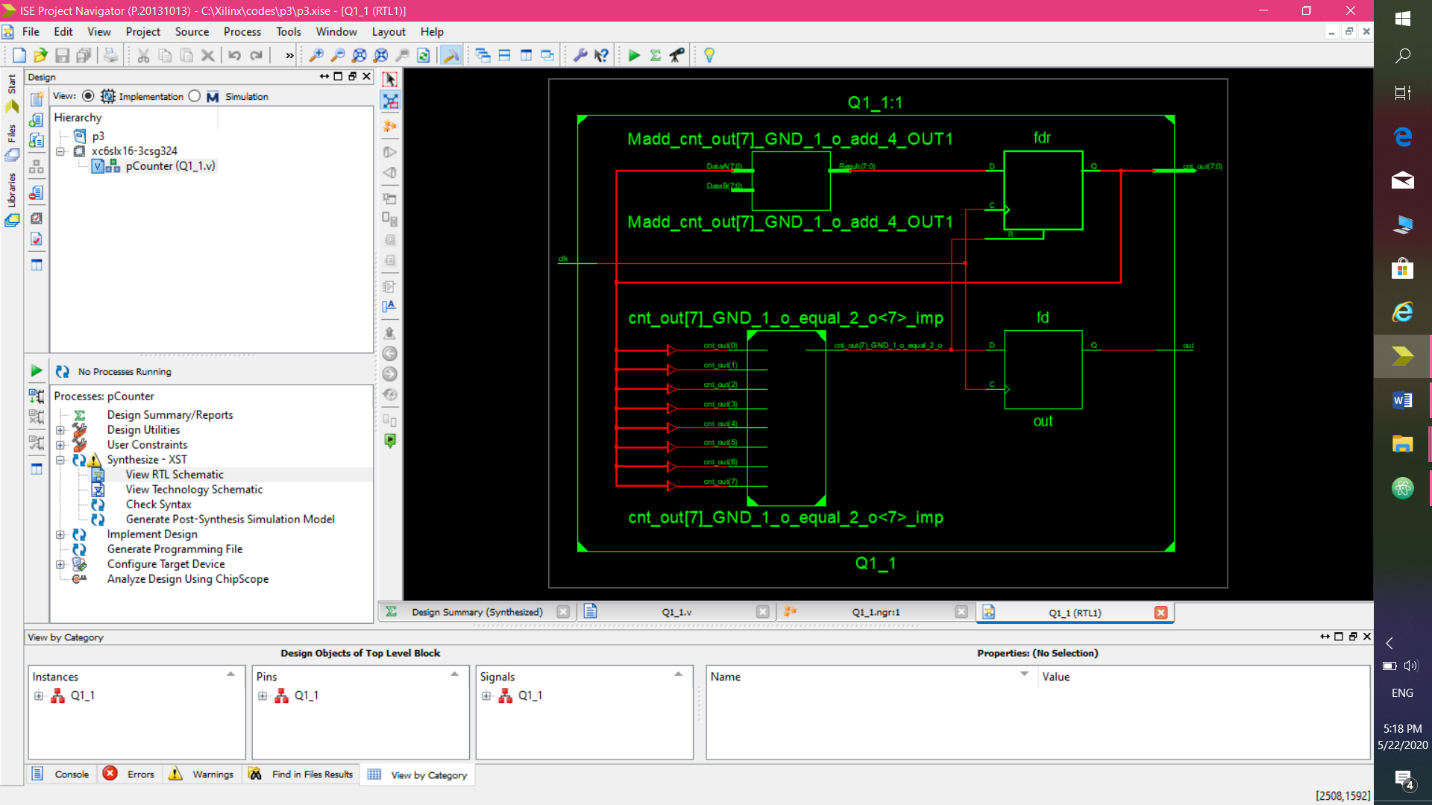
به نام خدا

* Q1-1 :

این بخش به درستی سنتز شد:

(warning اش مهم نبود)



اطلاعات synthesis report :

=========================================================================

\* HDL Synthesis \*

=========================================================================

Synthesizing Unit <pCounter>.

Related source file is "C:\Xilinx\codes\p3\Q1\_1.v".

p = 8'b00001010

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_1\_o\_add\_4\_OUT> created at line 42.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

Unit <pCounter> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 1

8-bit adder : 1

# Registers : 2

1-bit register : 1

8-bit register : 1

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

Synthesizing (advanced) Unit <pCounter>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounter> synthesized (advanced).

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Counters : 1

8-bit up counter : 1

# Registers : 1

Flip-Flops : 1

=========================================================================

=========================================================================

\* Design Summary \*

=========================================================================

Top Level Output File Name : pCounter.ngc

Primitive and Black Box Usage:

------------------------------

# BELS : 14

# GND : 1

# INV : 1

# LUT1 : 3

# LUT4 : 1

# MUXCY : 3

# VCC : 1

# XORCY : 4

# FlipFlops/Latches : 5

# FD : 1

# FDR : 4

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 9

# OBUF : 9

Device utilization summary:

---------------------------

Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice Registers: 5 out of 18224 0%

Number of Slice LUTs: 5 out of 9112 0%

Number used as Logic: 5 out of 9112 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 10

Number with an unused Flip Flop: 5 out of 10 50%

Number with an unused LUT: 5 out of 10 50%

Number of fully used LUT-FF pairs: 0 out of 10 0%

Number of unique control sets: 2

IO Utilization:

Number of IOs: 10

Number of bonded IOBs: 10 out of 232 4%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 5 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -3

Minimum period: 2.692ns (Maximum Frequency: 371.437MHz)

Minimum input arrival time before clock: No path found

Maximum output required time after clock: 3.668ns

Maximum combinational path delay: No path found

Timing Details:

---------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 2.692ns (frequency: 371.437MHz)

Total number of paths / destination ports: 30 / 9

-------------------------------------------------------------------------

Delay: 2.692ns (Levels of Logic = 1)

Source: cnt\_out\_3 (FF)

Destination: cnt\_out\_0 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: cnt\_out\_3 to cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDR:C->Q 3 0.447 0.898 cnt\_out\_3 (cnt\_out\_3)

LUT4:I0->O 5 0.203 0.714 cnt\_out[7]\_GND\_1\_o\_equal\_2\_o<7>1 (cnt\_out[7]\_GND\_1\_o\_equal\_2\_o)

FDR:R 0.430 cnt\_out\_0

----------------------------------------

Total 2.692ns (1.080ns logic, 1.612ns route)

(40.1% logic, 59.9% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 5 / 5

-------------------------------------------------------------------------

Offset: 3.668ns (Levels of Logic = 1)

Source: cnt\_out\_3 (FF)

Destination: cnt\_out<3> (PAD)

Source Clock: clk rising

Data Path: cnt\_out\_3 to cnt\_out<3>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDR:C->Q 3 0.447 0.650 cnt\_out\_3 (cnt\_out\_3)

OBUF:I->O 2.571 cnt\_out\_3\_OBUF (cnt\_out<3>)

----------------------------------------

Total 3.668ns (3.018ns logic, 0.650ns route)

(82.3% logic, 17.7% route)

=========================================================================

Cross Clock Domains Report:

--------------------------

Clock to Setup on destination clock clk

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | 2.692| | | |

---------------+---------+---------+---------+---------+

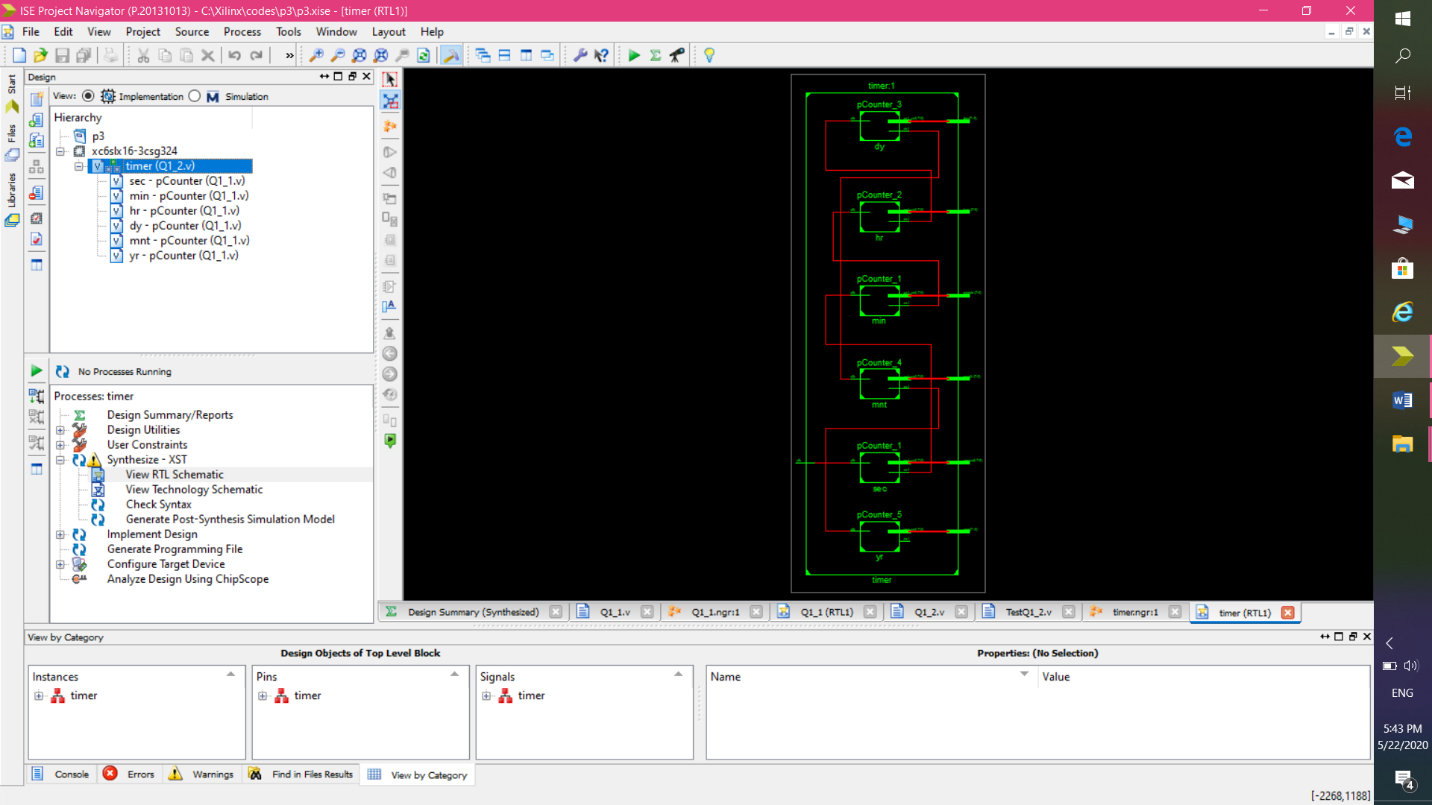
=========================================================================

* Q1-2 :

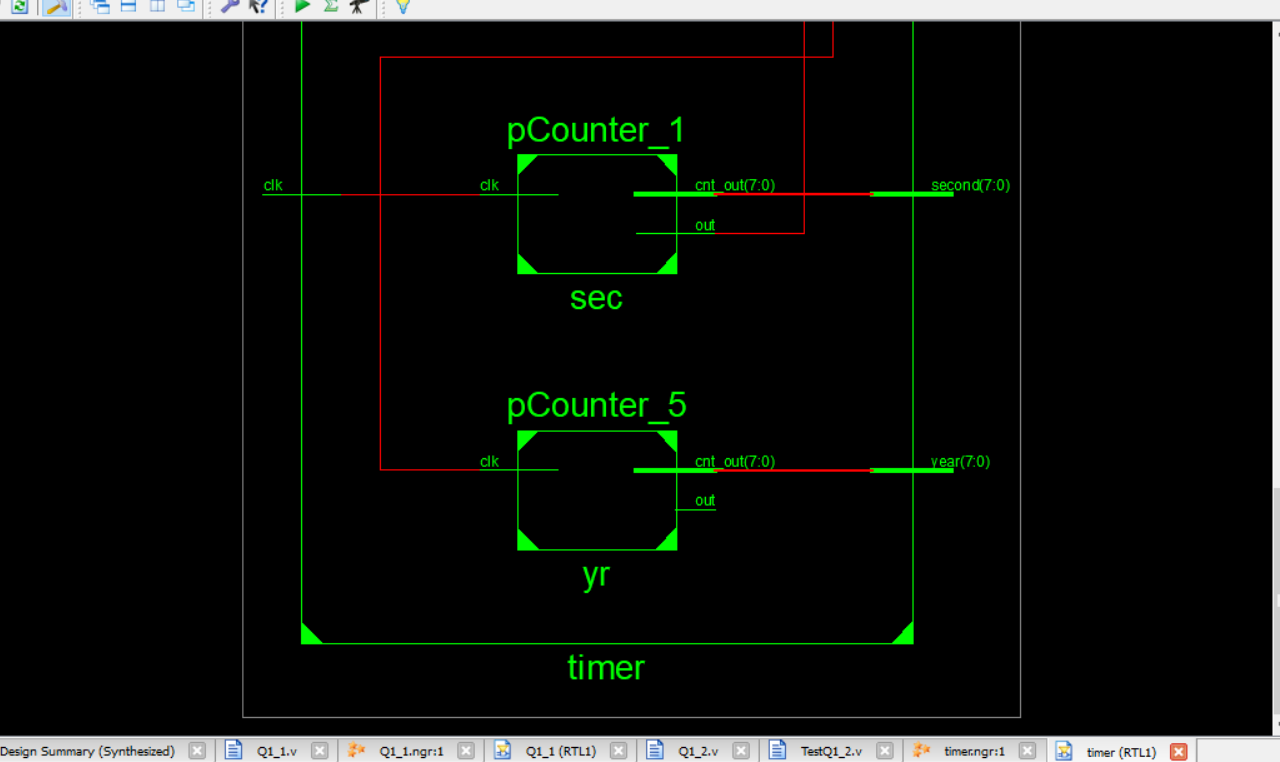
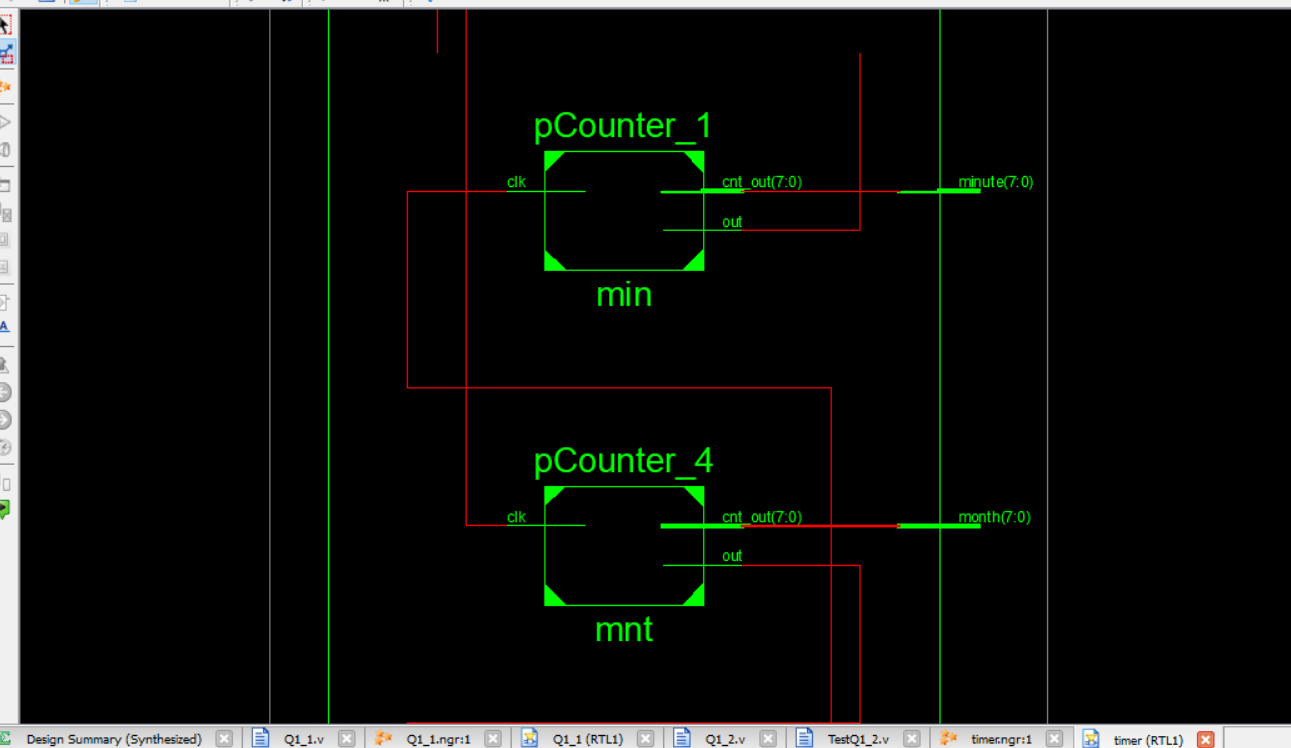
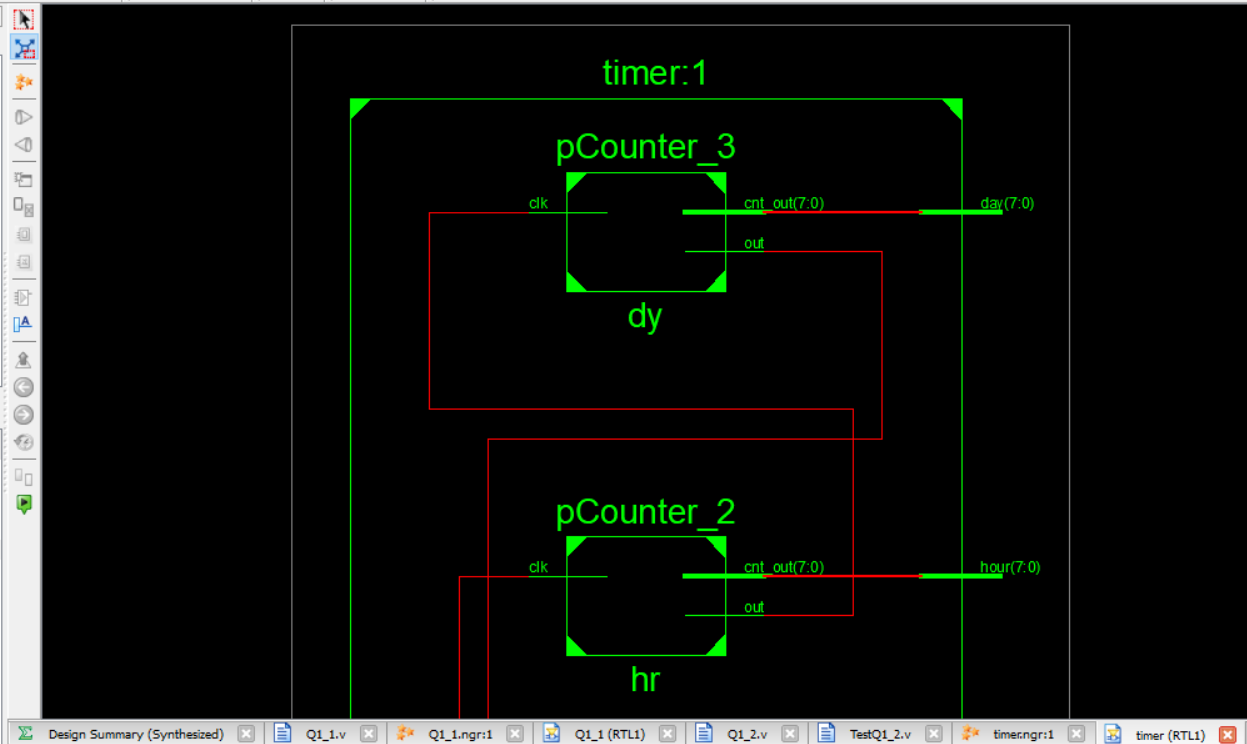
در این بخش، فایلی که قبلا فرستاده بودم قابل سنتز نبود. ارورش این بود که بعضی از متغیر ها را چند بار مقدار دهی کرده بودم(مقدار اولیه تعریف کرده بودم) .

این مشکل را رفع کردم و فایل درست و قابل سنتز را ضمیمه کردم.

حالا به درستی سنتز شد:



شمایRTL از نزدیکتر:



اطلاعات synthesis report :

=========================================================================

\* HDL Synthesis \*

=========================================================================

Synthesizing Unit <timer>.

Related source file is "C:\Xilinx\codes\p3\Q1\_2.v".

INFO:Xst:3210 - "C:\Xilinx\codes\p3\Q1\_2.v" line 38: Output port <out> of the instance <yr> is unconnected or connected to loadless signal.

Summary:

no macro.

Unit <timer> synthesized.

Synthesizing Unit <pCounter\_1>.

Related source file is "C:\Xilinx\codes\p3\Q1\_1.v".

p = 8'b00111011

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_2\_o\_add\_4\_OUT> created at line 42.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

Unit <pCounter\_1> synthesized.

Synthesizing Unit <pCounter\_2>.

Related source file is "C:\Xilinx\codes\p3\Q1\_1.v".

p = 8'b00010111

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_3\_o\_add\_4\_OUT> created at line 42.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

Unit <pCounter\_2> synthesized.

Synthesizing Unit <pCounter\_3>.

Related source file is "C:\Xilinx\codes\p3\Q1\_1.v".

p = 8'b00011101

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_4\_o\_add\_4\_OUT> created at line 42.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

Unit <pCounter\_3> synthesized.

Synthesizing Unit <pCounter\_4>.

Related source file is "C:\Xilinx\codes\p3\Q1\_1.v".

p = 8'b00001011

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_5\_o\_add\_4\_OUT> created at line 42.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

Unit <pCounter\_4> synthesized.

Synthesizing Unit <pCounter\_5>.

Related source file is "C:\Xilinx\codes\p3\Q1\_1.v".

p = 8'b00001010

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_6\_o\_add\_4\_OUT> created at line 42.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

Unit <pCounter\_5> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 6

8-bit adder : 6

# Registers : 12

1-bit register : 6

8-bit register : 6

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

Synthesizing (advanced) Unit <pCounter\_1>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounter\_1> synthesized (advanced).

Synthesizing (advanced) Unit <pCounter\_2>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounter\_2> synthesized (advanced).

Synthesizing (advanced) Unit <pCounter\_3>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounter\_3> synthesized (advanced).

Synthesizing (advanced) Unit <pCounter\_4>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounter\_4> synthesized (advanced).

Synthesizing (advanced) Unit <pCounter\_5>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounter\_5> synthesized (advanced).

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Counters : 6

8-bit up counter : 6

# Registers : 6

Flip-Flops : 6

=========================================================================

=========================================================================

\* Design Summary \*

=========================================================================

Top Level Output File Name : timer.ngc

Primitive and Black Box Usage:

------------------------------

# BELS : 200

# GND : 1

# INV : 6

# LUT1 : 42

# LUT2 : 48

# LUT3 : 6

# LUT6 : 6

# MUXCY : 42

# VCC : 1

# XORCY : 48

# FlipFlops/Latches : 53

# FD : 53

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 48

# OBUF : 48

Device utilization summary:

---------------------------

Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice Registers: 53 out of 18224 0%

Number of Slice LUTs: 108 out of 9112 1%

Number used as Logic: 108 out of 9112 1%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 108

Number with an unused Flip Flop: 55 out of 108 50%

Number with an unused LUT: 0 out of 108 0%

Number of fully used LUT-FF pairs: 53 out of 108 49%

Number of unique control sets: 6

IO Utilization:

Number of IOs: 49

Number of bonded IOBs: 49 out of 232 21%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

sec/out | NONE(min/out) | 9 |

clk | BUFGP | 9 |

min/out | NONE(hr/out) | 9 |

hr/out | NONE(dy/out) | 9 |

dy/out | NONE(mnt/out) | 9 |

mnt/out | NONE(yr/cnt\_out\_0) | 8 |

-----------------------------------+------------------------+-------+

INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer\_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -3

Minimum period: 3.453ns (Maximum Frequency: 289.616MHz)

Minimum input arrival time before clock: No path found

Maximum output required time after clock: 3.668ns

Maximum combinational path delay: No path found

Timing Details:

---------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'sec/out'

Clock period: 3.453ns (frequency: 289.616MHz)

Total number of paths / destination ports: 108 / 9

-------------------------------------------------------------------------

Delay: 3.453ns (Levels of Logic = 3)

Source: min/cnt\_out\_7 (FF)

Destination: min/cnt\_out\_0 (FF)

Source Clock: sec/out rising

Destination Clock: sec/out rising

Data Path: min/cnt\_out\_7 to min/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.879 min/cnt\_out\_7 (min/cnt\_out\_7)

LUT3:I0->O 1 0.205 0.580 min/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o<7>\_SW0 (N8)

LUT6:I5->O 9 0.205 0.830 min/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o<7> (min/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o)

LUT2:I1->O 1 0.205 0.000 min/cnt\_out\_0\_rstpot (min/cnt\_out\_0\_rstpot)

FD:D 0.102 min/cnt\_out\_0

----------------------------------------

Total 3.453ns (1.164ns logic, 2.289ns route)

(33.7% logic, 66.3% route)

=========================================================================

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 3.453ns (frequency: 289.616MHz)

Total number of paths / destination ports: 108 / 9

-------------------------------------------------------------------------

Delay: 3.453ns (Levels of Logic = 3)

Source: sec/cnt\_out\_7 (FF)

Destination: sec/cnt\_out\_0 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: sec/cnt\_out\_7 to sec/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.879 sec/cnt\_out\_7 (sec/cnt\_out\_7)

LUT3:I0->O 1 0.205 0.580 sec/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o<7>\_SW0 (N10)

LUT6:I5->O 9 0.205 0.830 sec/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o<7> (sec/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o)

LUT2:I1->O 1 0.205 0.000 sec/cnt\_out\_0\_rstpot (sec/cnt\_out\_0\_rstpot)

FD:D 0.102 sec/cnt\_out\_0

----------------------------------------

Total 3.453ns (1.164ns logic, 2.289ns route)

(33.7% logic, 66.3% route)

=========================================================================

Timing constraint: Default period analysis for Clock 'min/out'

Clock period: 3.453ns (frequency: 289.616MHz)

Total number of paths / destination ports: 108 / 9

-------------------------------------------------------------------------

Delay: 3.453ns (Levels of Logic = 3)

Source: hr/cnt\_out\_7 (FF)

Destination: hr/cnt\_out\_0 (FF)

Source Clock: min/out rising

Destination Clock: min/out rising

Data Path: hr/cnt\_out\_7 to hr/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.879 hr/cnt\_out\_7 (hr/cnt\_out\_7)

LUT3:I0->O 1 0.205 0.580 hr/cnt\_out[7]\_GND\_3\_o\_equal\_2\_o<7>\_SW0 (N12)

LUT6:I5->O 9 0.205 0.830 hr/cnt\_out[7]\_GND\_3\_o\_equal\_2\_o<7> (hr/cnt\_out[7]\_GND\_3\_o\_equal\_2\_o)

LUT2:I1->O 1 0.205 0.000 hr/cnt\_out\_0\_rstpot (hr/cnt\_out\_0\_rstpot)

FD:D 0.102 hr/cnt\_out\_0

----------------------------------------

Total 3.453ns (1.164ns logic, 2.289ns route)

(33.7% logic, 66.3% route)

=========================================================================

Timing constraint: Default period analysis for Clock 'hr/out'

Clock period: 3.453ns (frequency: 289.616MHz)

Total number of paths / destination ports: 108 / 9

-------------------------------------------------------------------------

Delay: 3.453ns (Levels of Logic = 3)

Source: dy/cnt\_out\_7 (FF)

Destination: dy/cnt\_out\_0 (FF)

Source Clock: hr/out rising

Destination Clock: hr/out rising

Data Path: dy/cnt\_out\_7 to dy/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.879 dy/cnt\_out\_7 (dy/cnt\_out\_7)

LUT3:I0->O 1 0.205 0.580 dy/cnt\_out[7]\_GND\_4\_o\_equal\_2\_o<7>\_SW0 (N14)

LUT6:I5->O 9 0.205 0.830 dy/cnt\_out[7]\_GND\_4\_o\_equal\_2\_o<7> (dy/cnt\_out[7]\_GND\_4\_o\_equal\_2\_o)

LUT2:I1->O 1 0.205 0.000 dy/cnt\_out\_0\_rstpot (dy/cnt\_out\_0\_rstpot)

FD:D 0.102 dy/cnt\_out\_0

----------------------------------------

Total 3.453ns (1.164ns logic, 2.289ns route)

(33.7% logic, 66.3% route)

=========================================================================

Timing constraint: Default period analysis for Clock 'dy/out'

Clock period: 3.453ns (frequency: 289.616MHz)

Total number of paths / destination ports: 108 / 9

-------------------------------------------------------------------------

Delay: 3.453ns (Levels of Logic = 3)

Source: mnt/cnt\_out\_7 (FF)

Destination: mnt/cnt\_out\_0 (FF)

Source Clock: dy/out rising

Destination Clock: dy/out rising

Data Path: mnt/cnt\_out\_7 to mnt/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.879 mnt/cnt\_out\_7 (mnt/cnt\_out\_7)

LUT3:I0->O 1 0.205 0.580 mnt/cnt\_out[7]\_GND\_5\_o\_equal\_2\_o<7>\_SW0 (N16)

LUT6:I5->O 9 0.205 0.830 mnt/cnt\_out[7]\_GND\_5\_o\_equal\_2\_o<7> (mnt/cnt\_out[7]\_GND\_5\_o\_equal\_2\_o)

LUT2:I1->O 1 0.205 0.000 mnt/cnt\_out\_0\_rstpot (mnt/cnt\_out\_0\_rstpot)

FD:D 0.102 mnt/cnt\_out\_0

----------------------------------------

Total 3.453ns (1.164ns logic, 2.289ns route)

(33.7% logic, 66.3% route)

=========================================================================

Timing constraint: Default period analysis for Clock 'mnt/out'

Clock period: 3.426ns (frequency: 291.915MHz)

Total number of paths / destination ports: 100 / 8

-------------------------------------------------------------------------

Delay: 3.426ns (Levels of Logic = 3)

Source: yr/cnt\_out\_7 (FF)

Destination: yr/cnt\_out\_0 (FF)

Source Clock: mnt/out rising

Destination Clock: mnt/out rising

Data Path: yr/cnt\_out\_7 to yr/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.879 yr/cnt\_out\_7 (yr/cnt\_out\_7)

LUT3:I0->O 1 0.205 0.580 yr/cnt\_out[7]\_GND\_6\_o\_equal\_2\_o<7>\_SW0 (N18)

LUT6:I5->O 8 0.205 0.803 yr/cnt\_out[7]\_GND\_6\_o\_equal\_2\_o<7> (yr/cnt\_out[7]\_GND\_6\_o\_equal\_2\_o)

LUT2:I1->O 1 0.205 0.000 yr/cnt\_out\_0\_rstpot (yr/cnt\_out\_0\_rstpot)

FD:D 0.102 yr/cnt\_out\_0

----------------------------------------

Total 3.426ns (1.164ns logic, 2.262ns route)

(34.0% logic, 66.0% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'mnt/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.668ns (Levels of Logic = 1)

Source: yr/cnt\_out\_7 (FF)

Destination: year<7> (PAD)

Source Clock: mnt/out rising

Data Path: yr/cnt\_out\_7 to year<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.650 yr/cnt\_out\_7 (yr/cnt\_out\_7)

OBUF:I->O 2.571 year\_7\_OBUF (year<7>)

----------------------------------------

Total 3.668ns (3.018ns logic, 0.650ns route)

(82.3% logic, 17.7% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'dy/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.668ns (Levels of Logic = 1)

Source: mnt/cnt\_out\_7 (FF)

Destination: month<7> (PAD)

Source Clock: dy/out rising

Data Path: mnt/cnt\_out\_7 to month<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.650 mnt/cnt\_out\_7 (mnt/cnt\_out\_7)

OBUF:I->O 2.571 month\_7\_OBUF (month<7>)

----------------------------------------

Total 3.668ns (3.018ns logic, 0.650ns route)

(82.3% logic, 17.7% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'hr/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.668ns (Levels of Logic = 1)

Source: dy/cnt\_out\_7 (FF)

Destination: day<7> (PAD)

Source Clock: hr/out rising

Data Path: dy/cnt\_out\_7 to day<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.650 dy/cnt\_out\_7 (dy/cnt\_out\_7)

OBUF:I->O 2.571 day\_7\_OBUF (day<7>)

----------------------------------------

Total 3.668ns (3.018ns logic, 0.650ns route)

(82.3% logic, 17.7% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'min/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.668ns (Levels of Logic = 1)

Source: hr/cnt\_out\_7 (FF)

Destination: hour<7> (PAD)

Source Clock: min/out rising

Data Path: hr/cnt\_out\_7 to hour<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.650 hr/cnt\_out\_7 (hr/cnt\_out\_7)

OBUF:I->O 2.571 hour\_7\_OBUF (hour<7>)

----------------------------------------

Total 3.668ns (3.018ns logic, 0.650ns route)

(82.3% logic, 17.7% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'sec/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.668ns (Levels of Logic = 1)

Source: min/cnt\_out\_7 (FF)

Destination: minute<7> (PAD)

Source Clock: sec/out rising

Data Path: min/cnt\_out\_7 to minute<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.650 min/cnt\_out\_7 (min/cnt\_out\_7)

OBUF:I->O 2.571 minute\_7\_OBUF (minute<7>)

----------------------------------------

Total 3.668ns (3.018ns logic, 0.650ns route)

(82.3% logic, 17.7% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.668ns (Levels of Logic = 1)

Source: sec/cnt\_out\_7 (FF)

Destination: second<7> (PAD)

Source Clock: clk rising

Data Path: sec/cnt\_out\_7 to second<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FD:C->Q 3 0.447 0.650 sec/cnt\_out\_7 (sec/cnt\_out\_7)

OBUF:I->O 2.571 second\_7\_OBUF (second<7>)

----------------------------------------

Total 3.668ns (3.018ns logic, 0.650ns route)

(82.3% logic, 17.7% route)

=========================================================================

Cross Clock Domains Report:

--------------------------

Clock to Setup on destination clock clk

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | 3.453| | | |

---------------+---------+---------+---------+---------+

Clock to Setup on destination clock dy/out

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

dy/out | 3.453| | | |

---------------+---------+---------+---------+---------+

Clock to Setup on destination clock hr/out

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

hr/out | 3.453| | | |

---------------+---------+---------+---------+---------+

Clock to Setup on destination clock min/out

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

min/out | 3.453| | | |

---------------+---------+---------+---------+---------+

Clock to Setup on destination clock mnt/out

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

mnt/out | 3.426| | | |

---------------+---------+---------+---------+---------+

Clock to Setup on destination clock sec/out

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

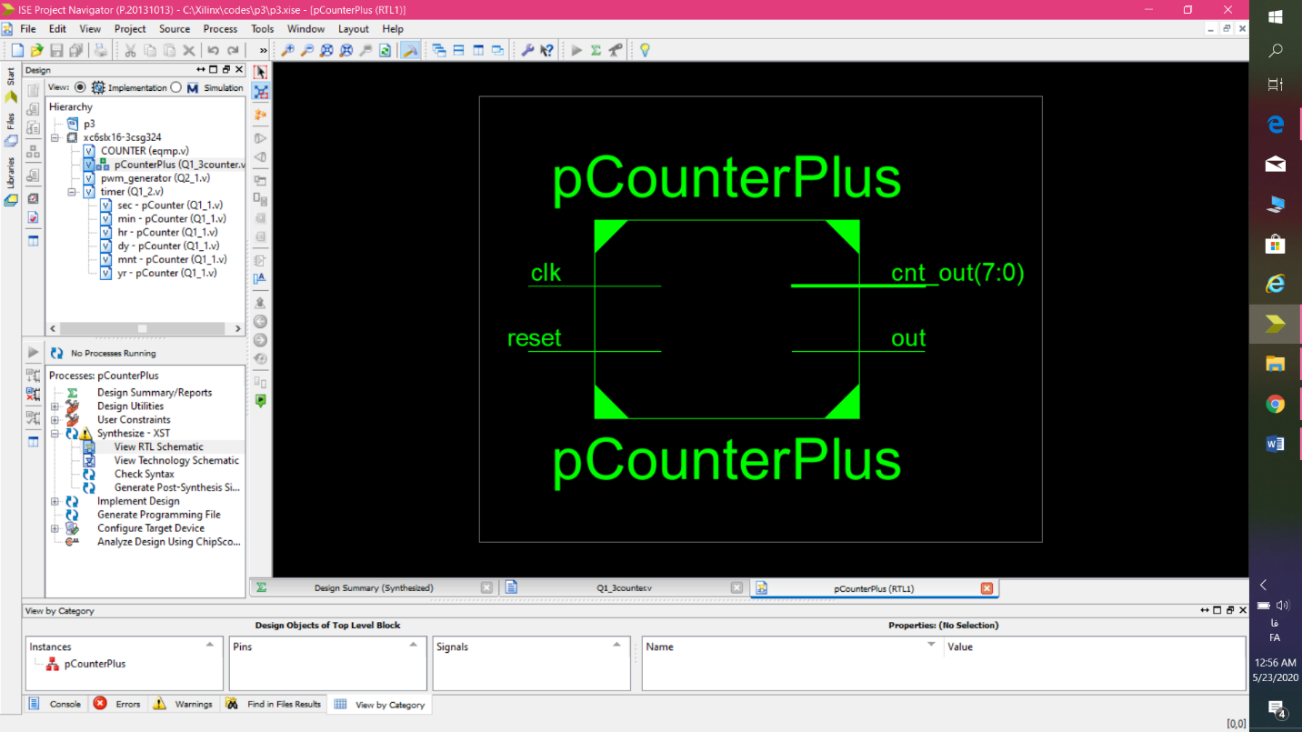
sec/out | 3.453| | | |

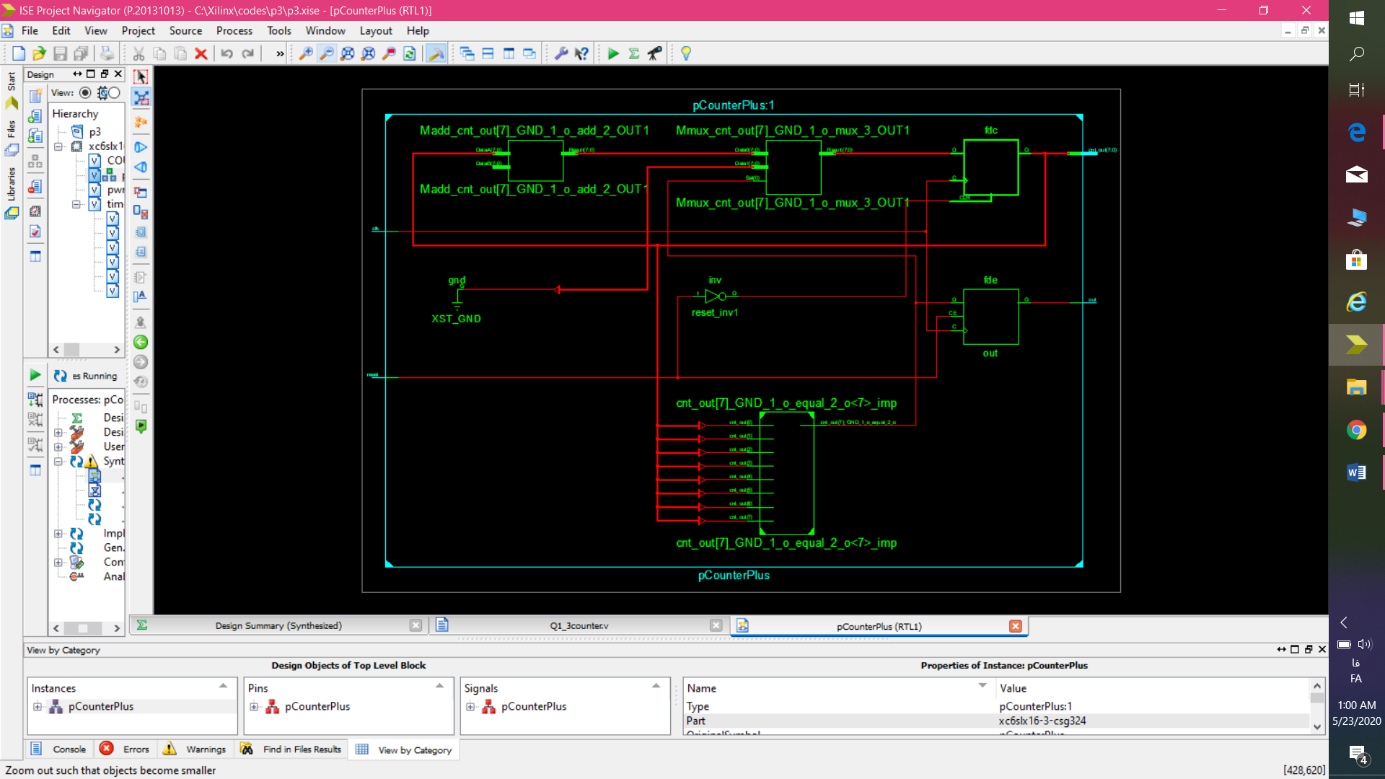
---------------+---------+---------+---------+---------+

=========================================================================

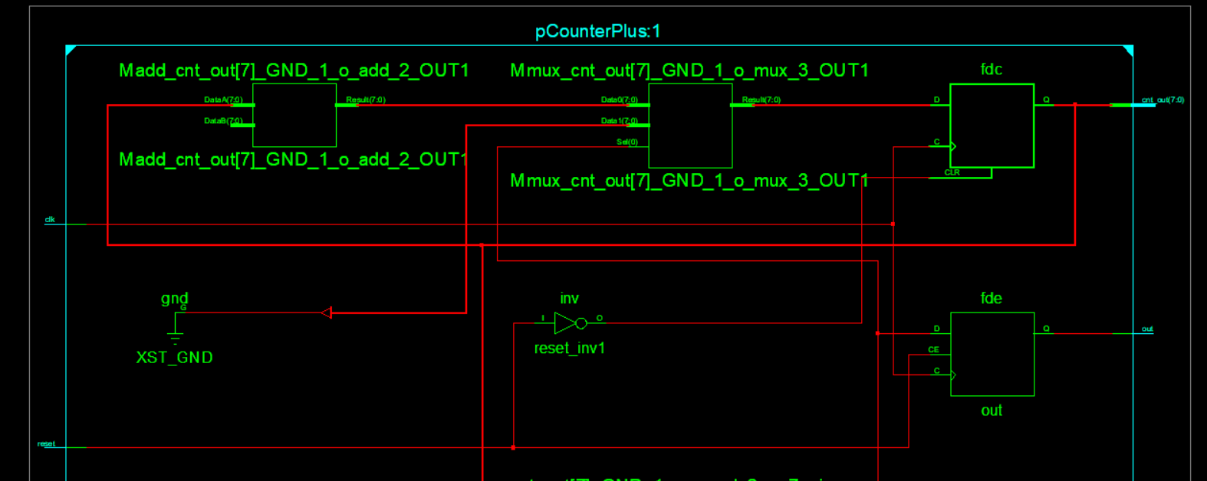
* Q1-3 :
* قسمت Q1-3counter با اصلاحاتی که اعمال شده(در تکلیف قبل به اشتباه فکر میکردم reset باید حساس به لبه باشد؛ در صورتی که باید حساس به سطح بود.)، سنتز شد:

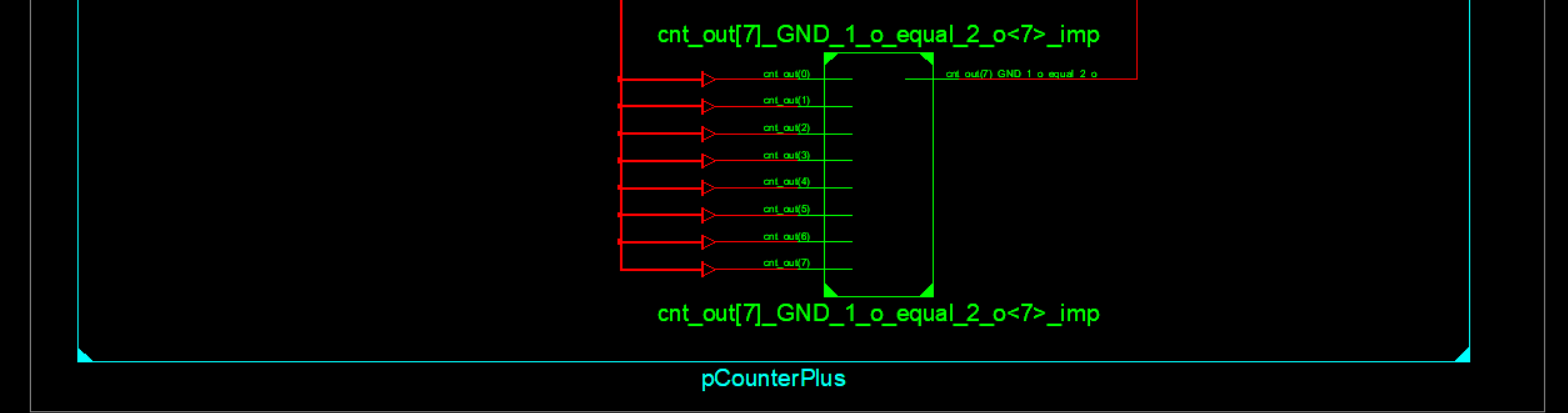
(ضمیمه شده)





از نزدیکتر:





اطلاعات synthesis report :

=========================================================================

\* HDL Synthesis \*

=========================================================================

Synthesizing Unit <pCounterPlus>.

Related source file is "C:\Xilinx\codes\p3\Q1\_3counter.v".

p = 8'b00001010

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_1\_o\_add\_2\_OUT> created at line 44.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <pCounterPlus> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 1

8-bit adder : 1

# Registers : 2

1-bit register : 1

8-bit register : 1

# Multiplexers : 1

8-bit 2-to-1 multiplexer : 1

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

Synthesizing (advanced) Unit <pCounterPlus>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounterPlus> synthesized (advanced).

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Counters : 1

8-bit up counter : 1

# Registers : 1

Flip-Flops : 1

=========================================================================

=========================================================================

\* Design Summary \*

=========================================================================

Top Level Output File Name : pCounterPlus.ngc

Primitive and Black Box Usage:

------------------------------

# BELS : 15

# GND : 1

# INV : 1

# LUT1 : 2

# LUT4 : 4

# MUXCY : 3

# XORCY : 4

# FlipFlops/Latches : 5

# FDC : 4

# FDE : 1

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 10

# IBUF : 1

# OBUF : 9

Device utilization summary:

---------------------------

Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice Registers: 5 out of 18224 0%

Number of Slice LUTs: 7 out of 9112 0%

Number used as Logic: 7 out of 9112 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 12

Number with an unused Flip Flop: 7 out of 12 58%

Number with an unused LUT: 5 out of 12 41%

Number of fully used LUT-FF pairs: 0 out of 12 0%

Number of unique control sets: 2

IO Utilization:

Number of IOs: 11

Number of bonded IOBs: 11 out of 232 4%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 5 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -3

Minimum period: 2.530ns (Maximum Frequency: 395.280MHz)

Minimum input arrival time before clock: 3.157ns

Maximum output required time after clock: 3.762ns

Maximum combinational path delay: No path found

Timing Details:

---------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 2.530ns (frequency: 395.280MHz)

Total number of paths / destination ports: 42 / 5

-------------------------------------------------------------------------

Delay: 2.530ns (Levels of Logic = 5)

Source: cnt\_out\_1 (FF)

Destination: cnt\_out\_3 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: cnt\_out\_1 to cnt\_out\_3

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 5 0.447 0.962 cnt\_out\_1 (cnt\_out\_1)

LUT4:I0->O 1 0.203 0.579 cnt\_out[7]\_GND\_1\_o\_equal\_2\_o\_inv1 (cnt\_out[7]\_GND\_1\_o\_equal\_2\_o\_inv)

MUXCY:CI->O 1 0.019 0.000 Mcount\_cnt\_out\_cy<0> (Mcount\_cnt\_out\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 Mcount\_cnt\_out\_cy<1> (Mcount\_cnt\_out\_cy<1>)

MUXCY:CI->O 0 0.019 0.000 Mcount\_cnt\_out\_cy<2> (Mcount\_cnt\_out\_cy<2>)

XORCY:CI->O 1 0.180 0.000 Mcount\_cnt\_out\_xor<3> (Mcount\_cnt\_out3)

FDC:D 0.102 cnt\_out\_3

----------------------------------------

Total 2.530ns (0.989ns logic, 1.541ns route)

(39.1% logic, 60.9% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 5 / 5

-------------------------------------------------------------------------

Offset: 3.157ns (Levels of Logic = 2)

Source: reset (PAD)

Destination: cnt\_out\_0 (FF)

Destination Clock: clk rising

Data Path: reset to cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 2 1.222 0.616 reset\_IBUF (reset\_IBUF)

INV:I->O 4 0.206 0.683 reset\_inv1\_INV\_0 (reset\_inv)

FDC:CLR 0.430 cnt\_out\_0

----------------------------------------

Total 3.157ns (1.858ns logic, 1.299ns route)

(58.9% logic, 41.1% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 5 / 5

-------------------------------------------------------------------------

Offset: 3.762ns (Levels of Logic = 1)

Source: cnt\_out\_2 (FF)

Destination: cnt\_out<2> (PAD)

Source Clock: clk rising

Data Path: cnt\_out\_2 to cnt\_out<2>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 6 0.447 0.744 cnt\_out\_2 (cnt\_out\_2)

OBUF:I->O 2.571 cnt\_out\_2\_OBUF (cnt\_out<2>)

----------------------------------------

Total 3.762ns (3.018ns logic, 0.744ns route)

(80.2% logic, 19.8% route)

=========================================================================

Cross Clock Domains Report:

--------------------------

Clock to Setup on destination clock clk

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

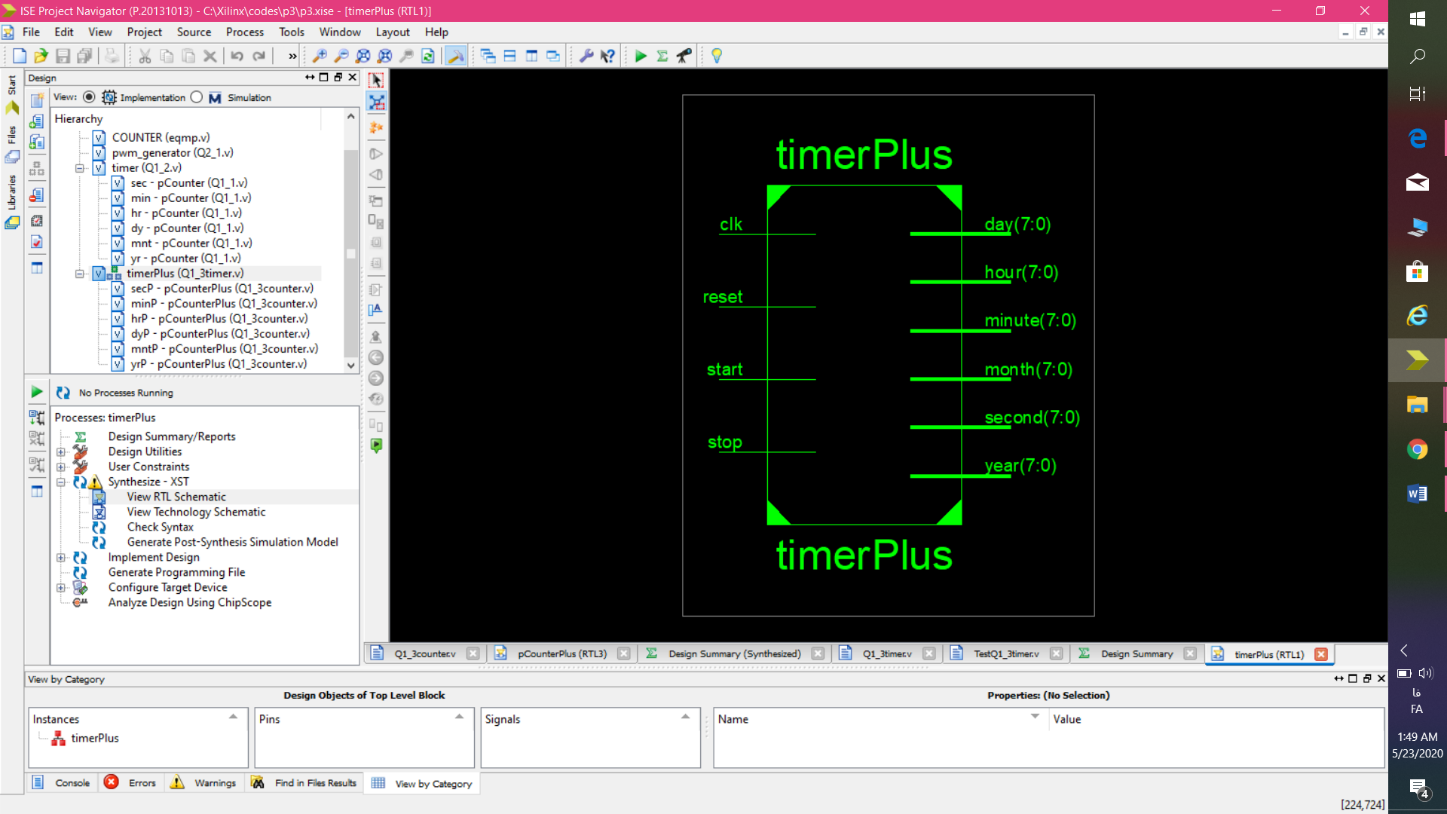
clk | 2.530| | | |

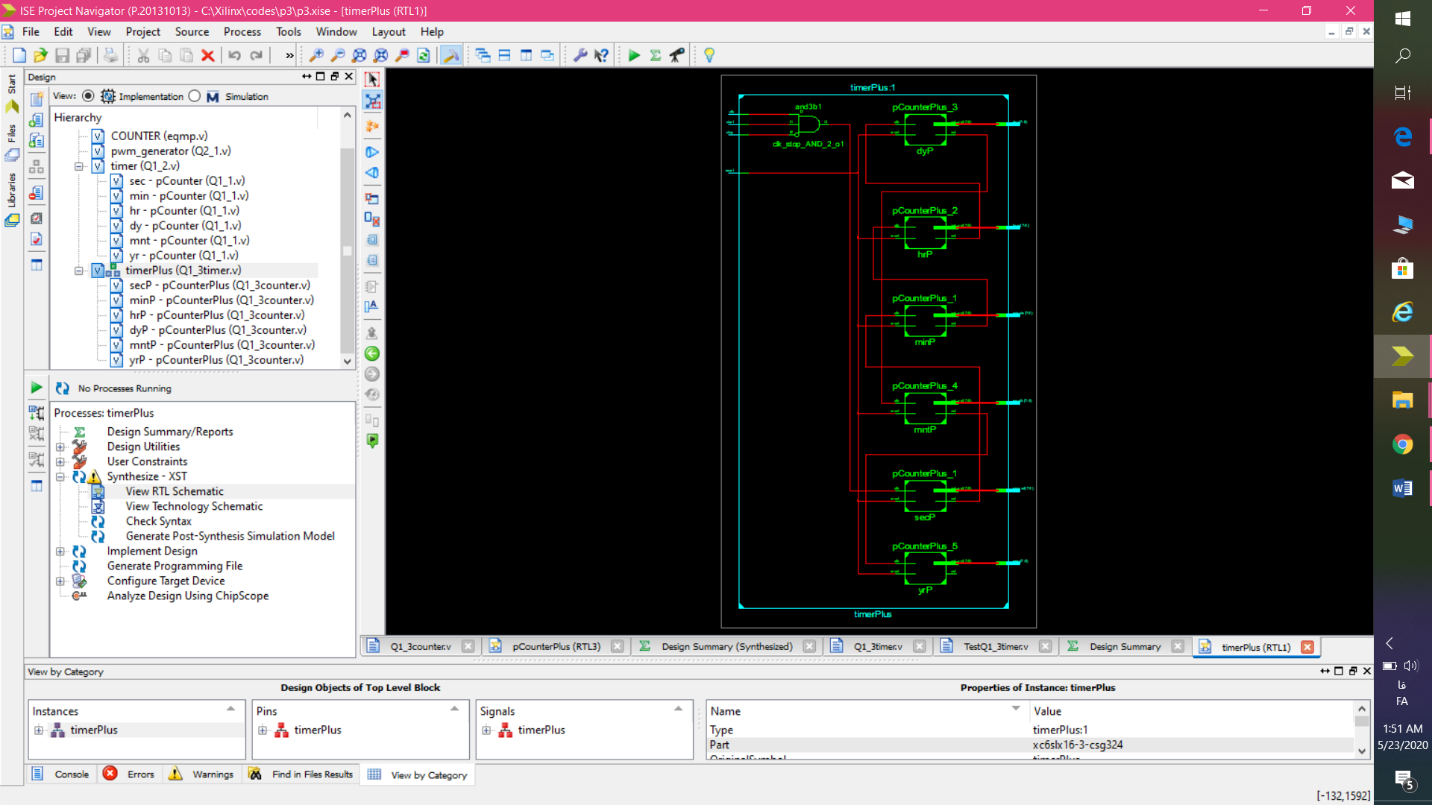
---------------+---------+---------+---------+---------+

=========================================================================

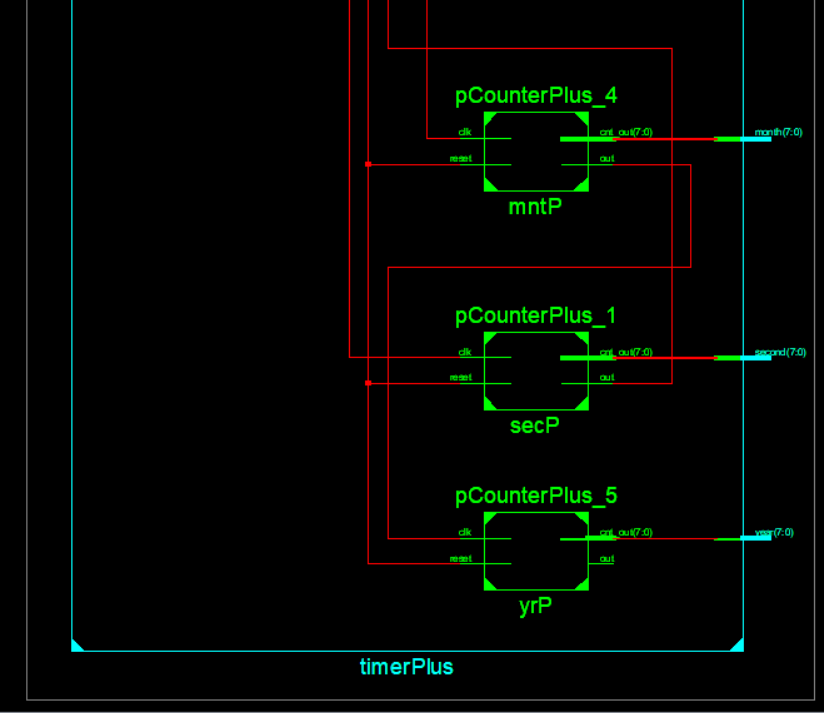
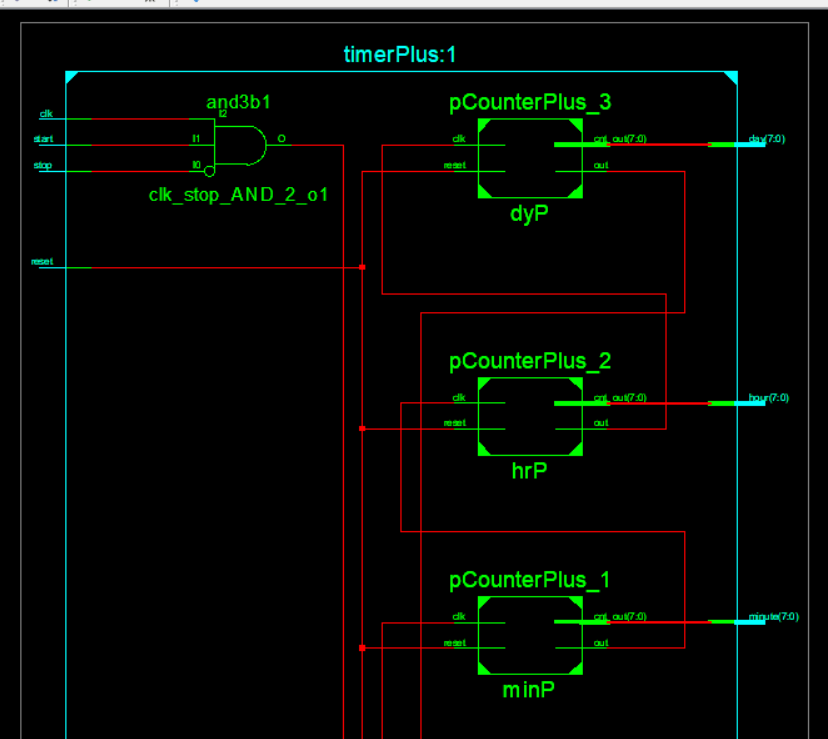
* قسمت نهایی (Q1-3timer) : سنتز فایل این بخش مانند Q1-2 ارور داشت و این ارور را داشت که بعضی از متغیر ها را چند بار مقدار دهی کرده بودم(مقدار اولیه تعریف کرده بودم). این مشکل را رفع کردم و فایل درست و قابل سنتز را ضمیمه کردم.

حالا به درستی سنتز شد:





و از نزدیکتر:



اطلاعات synthesis report :

=========================================================================

\* HDL Synthesis \*

=========================================================================

Synthesizing Unit <timerPlus>.

Related source file is "C:\Xilinx\codes\p3\Q1\_3timer.v".

INFO:Xst:3210 - "C:\Xilinx\codes\p3\Q1\_3timer.v" line 41: Output port <out> of the instance <yrP> is unconnected or connected to loadless signal.

Summary:

no macro.

Unit <timerPlus> synthesized.

Synthesizing Unit <pCounterPlus\_1>.

Related source file is "C:\Xilinx\codes\p3\Q1\_3counter.v".

p = 8'b00111011

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_2\_o\_add\_2\_OUT> created at line 44.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <pCounterPlus\_1> synthesized.

Synthesizing Unit <pCounterPlus\_2>.

Related source file is "C:\Xilinx\codes\p3\Q1\_3counter.v".

p = 8'b00010111

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_3\_o\_add\_2\_OUT> created at line 44.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <pCounterPlus\_2> synthesized.

Synthesizing Unit <pCounterPlus\_3>.

Related source file is "C:\Xilinx\codes\p3\Q1\_3counter.v".

p = 8'b00011101

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_4\_o\_add\_2\_OUT> created at line 44.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <pCounterPlus\_3> synthesized.

Synthesizing Unit <pCounterPlus\_4>.

Related source file is "C:\Xilinx\codes\p3\Q1\_3counter.v".

p = 8'b00001011

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_5\_o\_add\_2\_OUT> created at line 44.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <pCounterPlus\_4> synthesized.

Synthesizing Unit <pCounterPlus\_5>.

Related source file is "C:\Xilinx\codes\p3\Q1\_3counter.v".

p = 8'b00001010

Found 8-bit register for signal <cnt\_out>.

Found 1-bit register for signal <out>.

Found 8-bit adder for signal <cnt\_out[7]\_GND\_6\_o\_add\_2\_OUT> created at line 44.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 9 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <pCounterPlus\_5> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 6

8-bit adder : 6

# Registers : 12

1-bit register : 6

8-bit register : 6

# Multiplexers : 6

8-bit 2-to-1 multiplexer : 6

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

Synthesizing (advanced) Unit <pCounterPlus\_1>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounterPlus\_1> synthesized (advanced).

Synthesizing (advanced) Unit <pCounterPlus\_2>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounterPlus\_2> synthesized (advanced).

Synthesizing (advanced) Unit <pCounterPlus\_3>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounterPlus\_3> synthesized (advanced).

Synthesizing (advanced) Unit <pCounterPlus\_4>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounterPlus\_4> synthesized (advanced).

Synthesizing (advanced) Unit <pCounterPlus\_5>.

The following registers are absorbed into counter <cnt\_out>: 1 register on signal <cnt\_out>.

Unit <pCounterPlus\_5> synthesized (advanced).

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Counters : 6

8-bit up counter : 6

# Registers : 6

Flip-Flops : 6

=========================================================================

\* Design Summary \*

=========================================================================

Top Level Output File Name : timerPlus.ngc

Primitive and Black Box Usage:

------------------------------

# BELS : 160

# GND : 1

# INV : 1

# LUT1 : 22

# LUT2 : 2

# LUT3 : 7

# LUT6 : 37

# MUXCY : 42

# XORCY : 48

# FlipFlops/Latches : 53

# FDC : 48

# FDE : 5

# IO Buffers : 52

# IBUF : 4

# OBUF : 48

Device utilization summary:

---------------------------

Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice Registers: 53 out of 18224 0%

Number of Slice LUTs: 69 out of 9112 0%

Number used as Logic: 69 out of 9112 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 69

Number with an unused Flip Flop: 16 out of 69 23%

Number with an unused LUT: 0 out of 69 0%

Number of fully used LUT-FF pairs: 53 out of 69 76%

Number of unique control sets: 11

IO Utilization:

Number of IOs: 52

Number of bonded IOBs: 52 out of 232 22%

Specific Feature Utilization:

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-------------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-------------------------------------+------------------------+-------+

secP/out | NONE(minP/out) | 9 |

clk\_stop\_AND\_2\_o(clk\_stop\_AND\_2\_o1:O)| NONE(\*)(secP/out) | 9 |

minP/out | NONE(hrP/out) | 9 |

hrP/out | NONE(dyP/out) | 9 |

dyP/out | NONE(mntP/out) | 9 |

mntP/out | NONE(yrP/cnt\_out\_0) | 8 |

-------------------------------------+------------------------+-------+

(\*) This 1 clock signal(s) are generated by combinatorial logic,

and XST is not able to identify which are the primary clock signals.

Please use the CLOCK\_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.

INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer\_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -3

Minimum period: 3.587ns (Maximum Frequency: 278.781MHz)

Minimum input arrival time before clock: 4.120ns

Maximum output required time after clock: 3.900ns

Maximum combinational path delay: No path found

Timing Details:

---------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'secP/out'

Clock period: 3.504ns (frequency: 285.408MHz)

Total number of paths / destination ports: 297 / 9

-------------------------------------------------------------------------

Delay: 3.504ns (Levels of Logic = 10)

Source: minP/cnt\_out\_7 (FF)

Destination: minP/cnt\_out\_7 (FF)

Source Clock: secP/out rising

Destination Clock: secP/out rising

Data Path: minP/cnt\_out\_7 to minP/cnt\_out\_7

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 3 0.447 0.879 minP/cnt\_out\_7 (minP/cnt\_out\_7)

LUT3:I0->O 7 0.205 0.774 minP/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o<7>\_SW0 (N2)

LUT6:I5->O 1 0.205 0.579 minP/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o\_inv1 (minP/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o\_inv)

MUXCY:CI->O 1 0.019 0.000 minP/Mcount\_cnt\_out\_cy<0> (minP/Mcount\_cnt\_out\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 minP/Mcount\_cnt\_out\_cy<1> (minP/Mcount\_cnt\_out\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 minP/Mcount\_cnt\_out\_cy<2> (minP/Mcount\_cnt\_out\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 minP/Mcount\_cnt\_out\_cy<3> (minP/Mcount\_cnt\_out\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 minP/Mcount\_cnt\_out\_cy<4> (minP/Mcount\_cnt\_out\_cy<4>)

MUXCY:CI->O 1 0.019 0.000 minP/Mcount\_cnt\_out\_cy<5> (minP/Mcount\_cnt\_out\_cy<5>)

MUXCY:CI->O 0 0.019 0.000 minP/Mcount\_cnt\_out\_cy<6> (minP/Mcount\_cnt\_out\_cy<6>)

XORCY:CI->O 1 0.180 0.000 minP/Mcount\_cnt\_out\_xor<7> (minP/Mcount\_cnt\_out7)

FDC:D 0.102 minP/cnt\_out\_7

----------------------------------------

Total 3.504ns (1.272ns logic, 2.232ns route)

(36.3% logic, 63.7% route)

=========================================================================

Timing constraint: Default period analysis for Clock 'clk\_stop\_AND\_2\_o'

Clock period: 3.587ns (frequency: 278.781MHz)

Total number of paths / destination ports: 369 / 9

-------------------------------------------------------------------------

Delay: 3.587ns (Levels of Logic = 10)

Source: secP/cnt\_out\_7 (FF)

Destination: secP/cnt\_out\_7 (FF)

Source Clock: clk\_stop\_AND\_2\_o rising

Destination Clock: clk\_stop\_AND\_2\_o rising

Data Path: secP/cnt\_out\_7 to secP/cnt\_out\_7

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 3 0.447 0.879 secP/cnt\_out\_7 (secP/cnt\_out\_7)

LUT3:I0->O 10 0.205 0.857 secP/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o<7>\_SW0 (N4)

LUT6:I5->O 1 0.205 0.579 secP/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o\_inv1 (secP/cnt\_out[7]\_GND\_2\_o\_equal\_2\_o\_inv)

MUXCY:CI->O 1 0.019 0.000 secP/Mcount\_cnt\_out\_cy<0> (secP/Mcount\_cnt\_out\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 secP/Mcount\_cnt\_out\_cy<1> (secP/Mcount\_cnt\_out\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 secP/Mcount\_cnt\_out\_cy<2> (secP/Mcount\_cnt\_out\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 secP/Mcount\_cnt\_out\_cy<3> (secP/Mcount\_cnt\_out\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 secP/Mcount\_cnt\_out\_cy<4> (secP/Mcount\_cnt\_out\_cy<4>)

MUXCY:CI->O 1 0.019 0.000 secP/Mcount\_cnt\_out\_cy<5> (secP/Mcount\_cnt\_out\_cy<5>)

MUXCY:CI->O 0 0.019 0.000 secP/Mcount\_cnt\_out\_cy<6> (secP/Mcount\_cnt\_out\_cy<6>)

XORCY:CI->O 1 0.180 0.000 secP/Mcount\_cnt\_out\_xor<7> (secP/Mcount\_cnt\_out7)

FDC:D 0.102 secP/cnt\_out\_7

----------------------------------------

Total 3.587ns (1.272ns logic, 2.315ns route)

(35.5% logic, 64.5% route)

=========================================================================

Timing constraint: Default period analysis for Clock 'minP/out'

Clock period: 3.475ns (frequency: 287.782MHz)

Total number of paths / destination ports: 283 / 9

-------------------------------------------------------------------------

Delay: 3.475ns (Levels of Logic = 10)

Source: hrP/cnt\_out\_7 (FF)

Destination: hrP/cnt\_out\_7 (FF)

Source Clock: minP/out rising

Destination Clock: minP/out rising

Data Path: hrP/cnt\_out\_7 to hrP/cnt\_out\_7

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 3 0.447 0.879 hrP/cnt\_out\_7 (hrP/cnt\_out\_7)

LUT3:I0->O 6 0.205 0.745 hrP/cnt\_out[7]\_GND\_3\_o\_equal\_2\_o<7>\_SW0 (N6)

LUT6:I5->O 1 0.205 0.579 hrP/cnt\_out[7]\_GND\_3\_o\_equal\_2\_o\_inv1 (hrP/cnt\_out[7]\_GND\_3\_o\_equal\_2\_o\_inv)

MUXCY:CI->O 1 0.019 0.000 hrP/Mcount\_cnt\_out\_cy<0> (hrP/Mcount\_cnt\_out\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 hrP/Mcount\_cnt\_out\_cy<1> (hrP/Mcount\_cnt\_out\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 hrP/Mcount\_cnt\_out\_cy<2> (hrP/Mcount\_cnt\_out\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 hrP/Mcount\_cnt\_out\_cy<3> (hrP/Mcount\_cnt\_out\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 hrP/Mcount\_cnt\_out\_cy<4> (hrP/Mcount\_cnt\_out\_cy<4>)

MUXCY:CI->O 1 0.019 0.000 hrP/Mcount\_cnt\_out\_cy<5> (hrP/Mcount\_cnt\_out\_cy<5>)

MUXCY:CI->O 0 0.019 0.000 hrP/Mcount\_cnt\_out\_cy<6> (hrP/Mcount\_cnt\_out\_cy<6>)

XORCY:CI->O 1 0.180 0.000 hrP/Mcount\_cnt\_out\_xor<7> (hrP/Mcount\_cnt\_out7)

FDC:D 0.102 hrP/cnt\_out\_7

----------------------------------------

Total 3.475ns (1.272ns logic, 2.203ns route)

(36.6% logic, 63.4% route)

=========================================================================

Timing constraint: Default period analysis for Clock 'hrP/out'

Clock period: 3.475ns (frequency: 287.782MHz)

Total number of paths / destination ports: 269 / 9

-------------------------------------------------------------------------

Delay: 3.475ns (Levels of Logic = 10)

Source: dyP/cnt\_out\_7 (FF)

Destination: dyP/cnt\_out\_7 (FF)

Source Clock: hrP/out rising

Destination Clock: hrP/out rising

Data Path: dyP/cnt\_out\_7 to dyP/cnt\_out\_7

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 3 0.447 0.879 dyP/cnt\_out\_7 (dyP/cnt\_out\_7)

LUT3:I0->O 6 0.205 0.745 dyP/cnt\_out[7]\_GND\_4\_o\_equal\_2\_o<7>\_SW0 (N8)

LUT6:I5->O 1 0.205 0.579 dyP/cnt\_out[7]\_GND\_4\_o\_equal\_2\_o\_inv1 (dyP/cnt\_out[7]\_GND\_4\_o\_equal\_2\_o\_inv)

MUXCY:CI->O 1 0.019 0.000 dyP/Mcount\_cnt\_out\_cy<0> (dyP/Mcount\_cnt\_out\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 dyP/Mcount\_cnt\_out\_cy<1> (dyP/Mcount\_cnt\_out\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 dyP/Mcount\_cnt\_out\_cy<2> (dyP/Mcount\_cnt\_out\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 dyP/Mcount\_cnt\_out\_cy<3> (dyP/Mcount\_cnt\_out\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 dyP/Mcount\_cnt\_out\_cy<4> (dyP/Mcount\_cnt\_out\_cy<4>)

MUXCY:CI->O 1 0.019 0.000 dyP/Mcount\_cnt\_out\_cy<5> (dyP/Mcount\_cnt\_out\_cy<5>)

MUXCY:CI->O 0 0.019 0.000 dyP/Mcount\_cnt\_out\_cy<6> (dyP/Mcount\_cnt\_out\_cy<6>)

XORCY:CI->O 1 0.180 0.000 dyP/Mcount\_cnt\_out\_xor<7> (dyP/Mcount\_cnt\_out7)

FDC:D 0.102 dyP/cnt\_out\_7

----------------------------------------

Total 3.475ns (1.272ns logic, 2.203ns route)

(36.6% logic, 63.4% route)

=========================================================================

Timing constraint: Default period analysis for Clock 'dyP/out'

Clock period: 3.445ns (frequency: 290.267MHz)

Total number of paths / destination ports: 248 / 9

-------------------------------------------------------------------------

Delay: 3.445ns (Levels of Logic = 10)

Source: mntP/cnt\_out\_7 (FF)

Destination: mntP/cnt\_out\_7 (FF)

Source Clock: dyP/out rising

Destination Clock: dyP/out rising

Data Path: mntP/cnt\_out\_7 to mntP/cnt\_out\_7

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 3 0.447 0.879 mntP/cnt\_out\_7 (mntP/cnt\_out\_7)

LUT3:I0->O 5 0.205 0.715 mntP/cnt\_out[7]\_GND\_5\_o\_equal\_2\_o<7>\_SW0 (N10)

LUT6:I5->O 1 0.205 0.579 mntP/cnt\_out[7]\_GND\_5\_o\_equal\_2\_o\_inv1 (mntP/cnt\_out[7]\_GND\_5\_o\_equal\_2\_o\_inv)

MUXCY:CI->O 1 0.019 0.000 mntP/Mcount\_cnt\_out\_cy<0> (mntP/Mcount\_cnt\_out\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 mntP/Mcount\_cnt\_out\_cy<1> (mntP/Mcount\_cnt\_out\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 mntP/Mcount\_cnt\_out\_cy<2> (mntP/Mcount\_cnt\_out\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 mntP/Mcount\_cnt\_out\_cy<3> (mntP/Mcount\_cnt\_out\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 mntP/Mcount\_cnt\_out\_cy<4> (mntP/Mcount\_cnt\_out\_cy<4>)

MUXCY:CI->O 1 0.019 0.000 mntP/Mcount\_cnt\_out\_cy<5> (mntP/Mcount\_cnt\_out\_cy<5>)

MUXCY:CI->O 0 0.019 0.000 mntP/Mcount\_cnt\_out\_cy<6> (mntP/Mcount\_cnt\_out\_cy<6>)

XORCY:CI->O 1 0.180 0.000 mntP/Mcount\_cnt\_out\_xor<7> (mntP/Mcount\_cnt\_out7)

FDC:D 0.102 mntP/cnt\_out\_7

----------------------------------------

Total 3.445ns (1.272ns logic, 2.173ns route)

(36.9% logic, 63.1% route)

=========================================================================

Timing constraint: Default period analysis for Clock 'mntP/out'

Clock period: 3.381ns (frequency: 295.740MHz)

Total number of paths / destination ports: 184 / 8

-------------------------------------------------------------------------

Delay: 3.381ns (Levels of Logic = 10)

Source: yrP/cnt\_out\_7 (FF)

Destination: yrP/cnt\_out\_7 (FF)

Source Clock: mntP/out rising

Destination Clock: mntP/out rising

Data Path: yrP/cnt\_out\_7 to yrP/cnt\_out\_7

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 3 0.447 0.879 yrP/cnt\_out\_7 (yrP/cnt\_out\_7)

LUT3:I0->O 3 0.205 0.651 yrP/cnt\_out[7]\_GND\_6\_o\_equal\_2\_o<7>\_SW0 (N12)

LUT6:I5->O 1 0.205 0.579 yrP/cnt\_out[7]\_GND\_6\_o\_equal\_2\_o\_inv1 (yrP/cnt\_out[7]\_GND\_6\_o\_equal\_2\_o\_inv)

MUXCY:CI->O 1 0.019 0.000 yrP/Mcount\_cnt\_out\_cy<0> (yrP/Mcount\_cnt\_out\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 yrP/Mcount\_cnt\_out\_cy<1> (yrP/Mcount\_cnt\_out\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 yrP/Mcount\_cnt\_out\_cy<2> (yrP/Mcount\_cnt\_out\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 yrP/Mcount\_cnt\_out\_cy<3> (yrP/Mcount\_cnt\_out\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 yrP/Mcount\_cnt\_out\_cy<4> (yrP/Mcount\_cnt\_out\_cy<4>)

MUXCY:CI->O 1 0.019 0.000 yrP/Mcount\_cnt\_out\_cy<5> (yrP/Mcount\_cnt\_out\_cy<5>)

MUXCY:CI->O 0 0.019 0.000 yrP/Mcount\_cnt\_out\_cy<6> (yrP/Mcount\_cnt\_out\_cy<6>)

XORCY:CI->O 1 0.180 0.000 yrP/Mcount\_cnt\_out\_xor<7> (yrP/Mcount\_cnt\_out7)

FDC:D 0.102 yrP/cnt\_out\_7

----------------------------------------

Total 3.381ns (1.272ns logic, 2.109ns route)

(37.6% logic, 62.4% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'secP/out'

Total number of paths / destination ports: 9 / 9

-------------------------------------------------------------------------

Offset: 4.120ns (Levels of Logic = 2)

Source: reset (PAD)

Destination: minP/cnt\_out\_0 (FF)

Destination Clock: secP/out rising

Data Path: reset to minP/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 6 1.222 0.744 reset\_IBUF (reset\_IBUF)

INV:I->O 48 0.206 1.519 reset\_inv1\_INV\_0 (reset\_inv)

FDC:CLR 0.430 minP/cnt\_out\_0

----------------------------------------

Total 4.120ns (1.858ns logic, 2.262ns route)

(45.1% logic, 54.9% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk\_stop\_AND\_2\_o'

Total number of paths / destination ports: 9 / 9

-------------------------------------------------------------------------

Offset: 4.120ns (Levels of Logic = 2)

Source: reset (PAD)

Destination: secP/cnt\_out\_0 (FF)

Destination Clock: clk\_stop\_AND\_2\_o rising

Data Path: reset to secP/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 6 1.222 0.744 reset\_IBUF (reset\_IBUF)

INV:I->O 48 0.206 1.519 reset\_inv1\_INV\_0 (reset\_inv)

FDC:CLR 0.430 secP/cnt\_out\_0

----------------------------------------

Total 4.120ns (1.858ns logic, 2.262ns route)

(45.1% logic, 54.9% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'minP/out'

Total number of paths / destination ports: 9 / 9

-------------------------------------------------------------------------

Offset: 4.120ns (Levels of Logic = 2)

Source: reset (PAD)

Destination: hrP/cnt\_out\_0 (FF)

Destination Clock: minP/out rising

Data Path: reset to hrP/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 6 1.222 0.744 reset\_IBUF (reset\_IBUF)

INV:I->O 48 0.206 1.519 reset\_inv1\_INV\_0 (reset\_inv)

FDC:CLR 0.430 hrP/cnt\_out\_0

----------------------------------------

Total 4.120ns (1.858ns logic, 2.262ns route)

(45.1% logic, 54.9% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'hrP/out'

Total number of paths / destination ports: 9 / 9

-------------------------------------------------------------------------

Offset: 4.120ns (Levels of Logic = 2)

Source: reset (PAD)

Destination: dyP/cnt\_out\_0 (FF)

Destination Clock: hrP/out rising

Data Path: reset to dyP/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 6 1.222 0.744 reset\_IBUF (reset\_IBUF)

INV:I->O 48 0.206 1.519 reset\_inv1\_INV\_0 (reset\_inv)

FDC:CLR 0.430 dyP/cnt\_out\_0

----------------------------------------

Total 4.120ns (1.858ns logic, 2.262ns route)

(45.1% logic, 54.9% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'dyP/out'

Total number of paths / destination ports: 9 / 9

-------------------------------------------------------------------------

Offset: 4.120ns (Levels of Logic = 2)

Source: reset (PAD)

Destination: mntP/cnt\_out\_0 (FF)

Destination Clock: dyP/out rising

Data Path: reset to mntP/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 6 1.222 0.744 reset\_IBUF (reset\_IBUF)

INV:I->O 48 0.206 1.519 reset\_inv1\_INV\_0 (reset\_inv)

FDC:CLR 0.430 mntP/cnt\_out\_0

----------------------------------------

Total 4.120ns (1.858ns logic, 2.262ns route)

(45.1% logic, 54.9% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'mntP/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 4.120ns (Levels of Logic = 2)

Source: reset (PAD)

Destination: yrP/cnt\_out\_0 (FF)

Destination Clock: mntP/out rising

Data Path: reset to yrP/cnt\_out\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 6 1.222 0.744 reset\_IBUF (reset\_IBUF)

INV:I->O 48 0.206 1.519 reset\_inv1\_INV\_0 (reset\_inv)

FDC:CLR 0.430 yrP/cnt\_out\_0

----------------------------------------

Total 4.120ns (1.858ns logic, 2.262ns route)

(45.1% logic, 54.9% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'mntP/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.732ns (Levels of Logic = 1)

Source: yrP/cnt\_out\_4 (FF)

Destination: year<4> (PAD)

Source Clock: mntP/out rising

Data Path: yrP/cnt\_out\_4 to year<4>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 5 0.447 0.714 yrP/cnt\_out\_4 (yrP/cnt\_out\_4)

OBUF:I->O 2.571 year\_4\_OBUF (year<4>)

----------------------------------------

Total 3.732ns (3.018ns logic, 0.714ns route)

(80.9% logic, 19.1% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'dyP/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.791ns (Levels of Logic = 1)

Source: mntP/cnt\_out\_4 (FF)

Destination: month<4> (PAD)

Source Clock: dyP/out rising

Data Path: mntP/cnt\_out\_4 to month<4>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 7 0.447 0.773 mntP/cnt\_out\_4 (mntP/cnt\_out\_4)

OBUF:I->O 2.571 month\_4\_OBUF (month<4>)

----------------------------------------

Total 3.791ns (3.018ns logic, 0.773ns route)

(79.6% logic, 20.4% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'hrP/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.820ns (Levels of Logic = 1)

Source: dyP/cnt\_out\_1 (FF)

Destination: day<1> (PAD)

Source Clock: hrP/out rising

Data Path: dyP/cnt\_out\_1 to day<1>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 8 0.447 0.802 dyP/cnt\_out\_1 (dyP/cnt\_out\_1)

OBUF:I->O 2.571 day\_1\_OBUF (day<1>)

----------------------------------------

Total 3.820ns (3.018ns logic, 0.802ns route)

(79.0% logic, 21.0% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'minP/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.820ns (Levels of Logic = 1)

Source: hrP/cnt\_out\_3 (FF)

Destination: hour<3> (PAD)

Source Clock: minP/out rising

Data Path: hrP/cnt\_out\_3 to hour<3>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 8 0.447 0.802 hrP/cnt\_out\_3 (hrP/cnt\_out\_3)

OBUF:I->O 2.571 hour\_3\_OBUF (hour<3>)

----------------------------------------

Total 3.820ns (3.018ns logic, 0.802ns route)

(79.0% logic, 21.0% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'secP/out'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.820ns (Levels of Logic = 1)

Source: minP/cnt\_out\_5 (FF)

Destination: minute<5> (PAD)

Source Clock: secP/out rising

Data Path: minP/cnt\_out\_5 to minute<5>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 8 0.447 0.802 minP/cnt\_out\_5 (minP/cnt\_out\_5)

OBUF:I->O 2.571 minute\_5\_OBUF (minute<5>)

----------------------------------------

Total 3.820ns (3.018ns logic, 0.802ns route)

(79.0% logic, 21.0% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk\_stop\_AND\_2\_o'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 3.900ns (Levels of Logic = 1)

Source: secP/cnt\_out\_5 (FF)

Destination: second<5> (PAD)

Source Clock: clk\_stop\_AND\_2\_o rising

Data Path: secP/cnt\_out\_5 to second<5>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 11 0.447 0.882 secP/cnt\_out\_5 (secP/cnt\_out\_5)

OBUF:I->O 2.571 second\_5\_OBUF (second<5>)

----------------------------------------

Total 3.900ns (3.018ns logic, 0.882ns route)

(77.4% logic, 22.6% route)

=========================================================================

Cross Clock Domains Report:

--------------------------

Clock to Setup on destination clock clk\_stop\_AND\_2\_o

----------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

----------------+---------+---------+---------+---------+

clk\_stop\_AND\_2\_o| 3.587| | | |

----------------+---------+---------+---------+---------+

Clock to Setup on destination clock dyP/out

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

dyP/out | 3.445| | | |

---------------+---------+---------+---------+---------+

Clock to Setup on destination clock hrP/out

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

hrP/out | 3.475| | | |

---------------+---------+---------+---------+---------+

Clock to Setup on destination clock minP/out

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

minP/out | 3.475| | | |

---------------+---------+---------+---------+---------+

Clock to Setup on destination clock mntP/out

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

mntP/out | 3.381| | | |

---------------+---------+---------+---------+---------+

Clock to Setup on destination clock secP/out

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

secP/out | 3.504| | | |

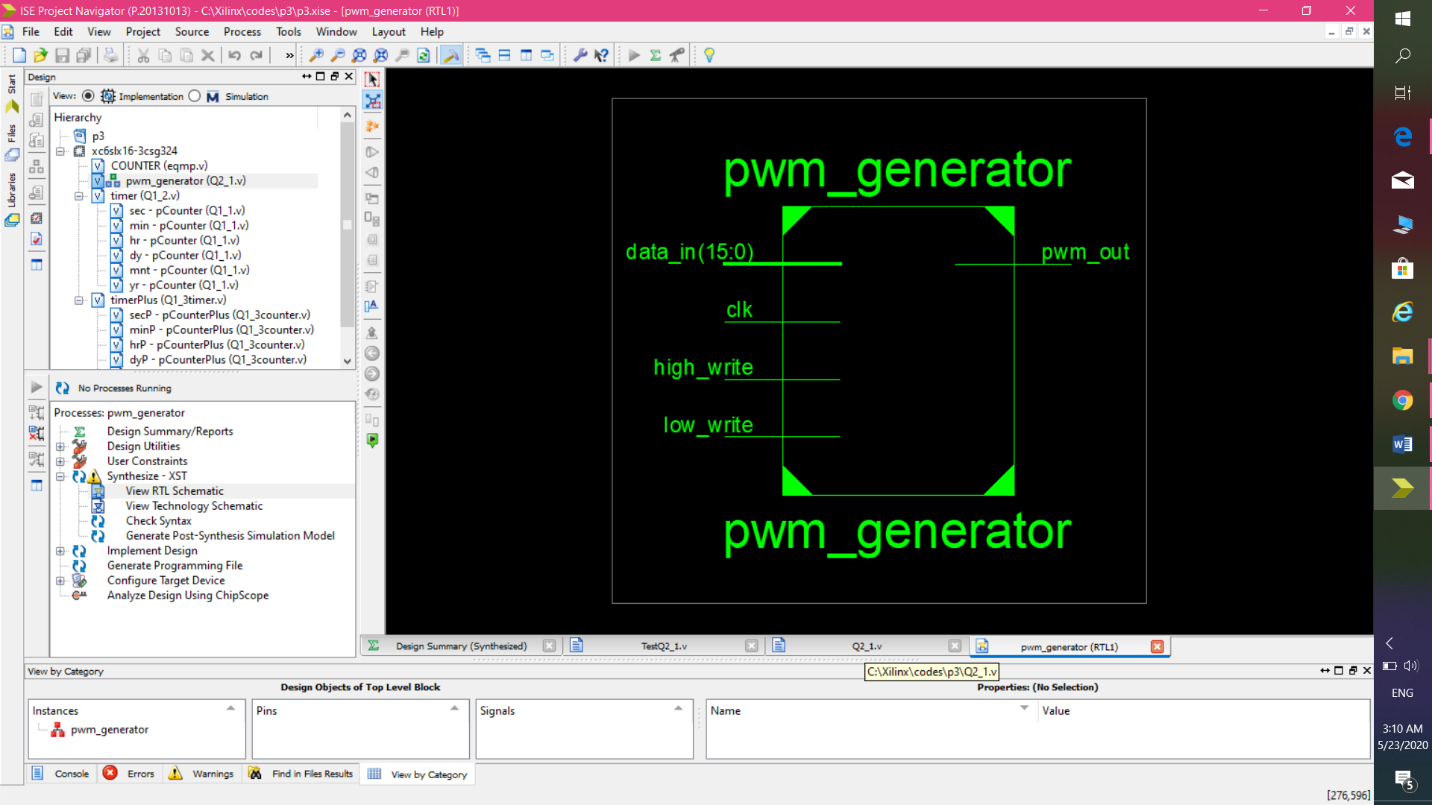
---------------+---------+---------+---------+---------+

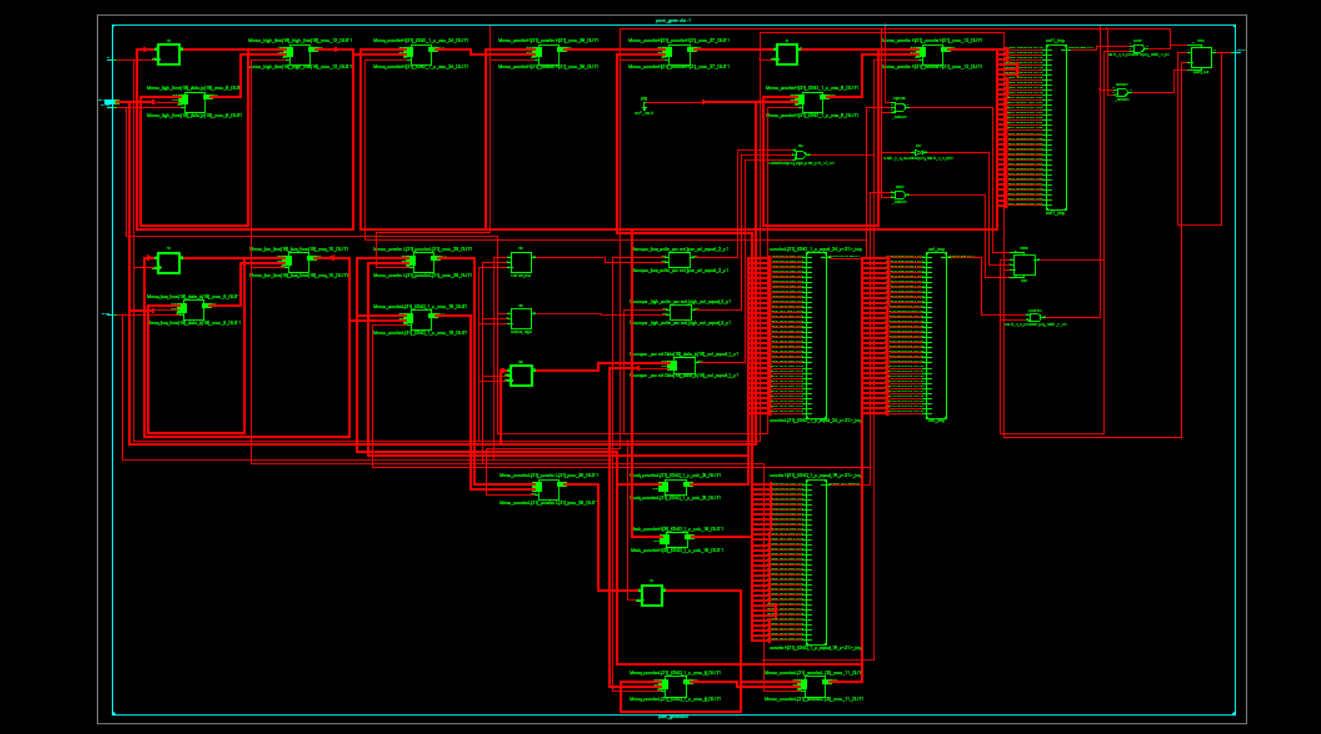
=========================================================================

* Q2-1 :

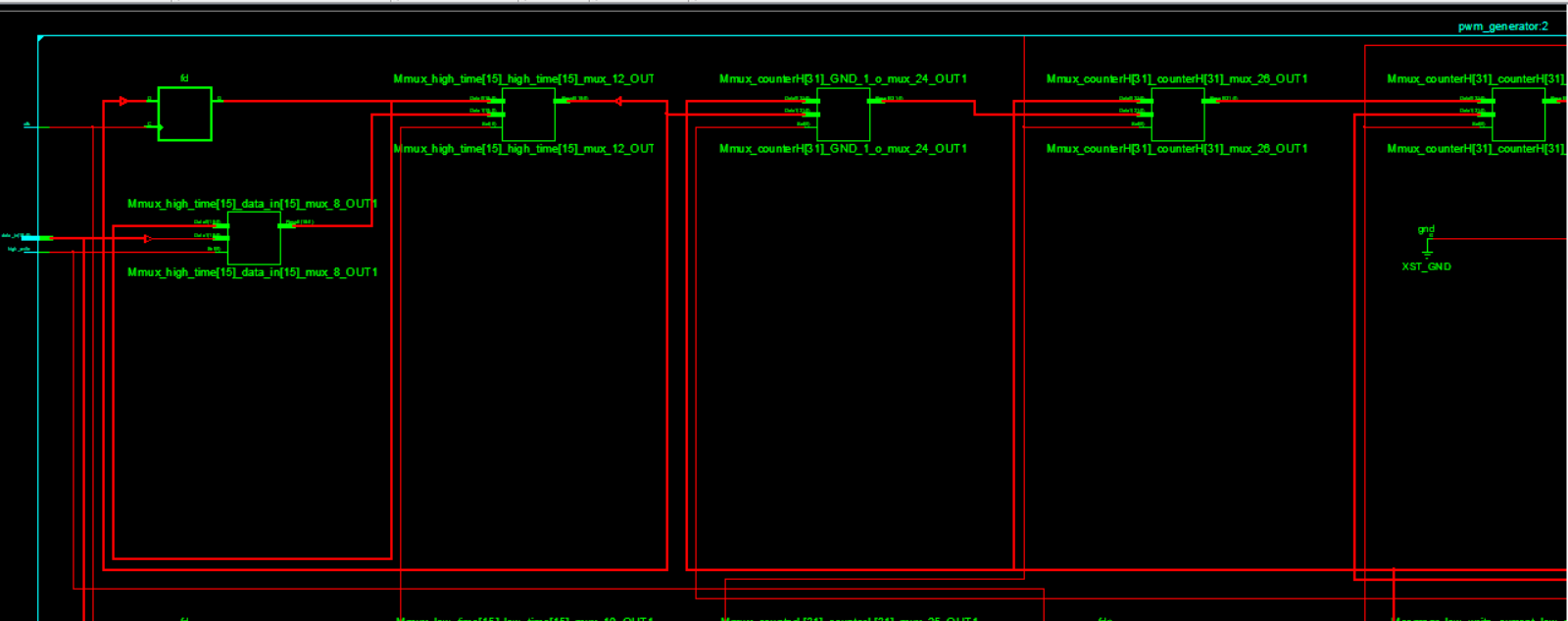
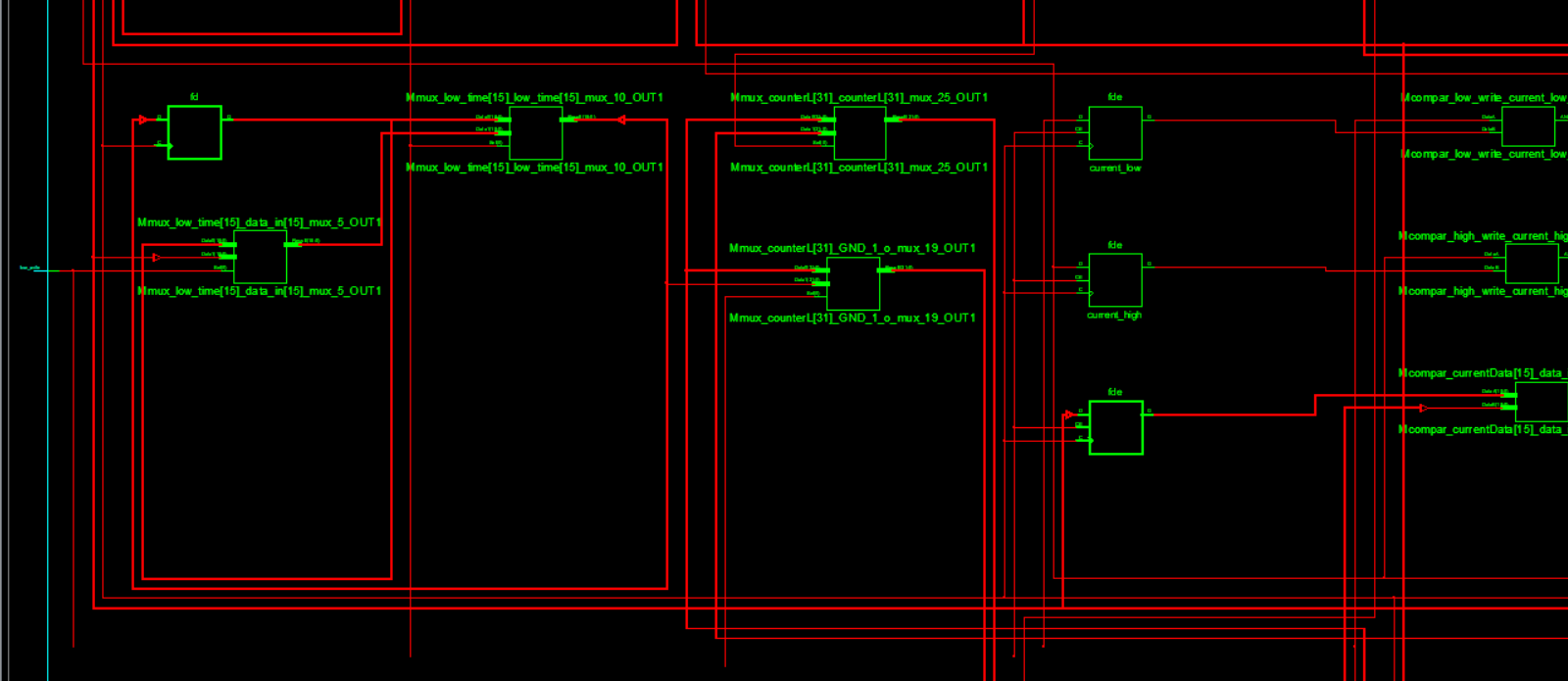
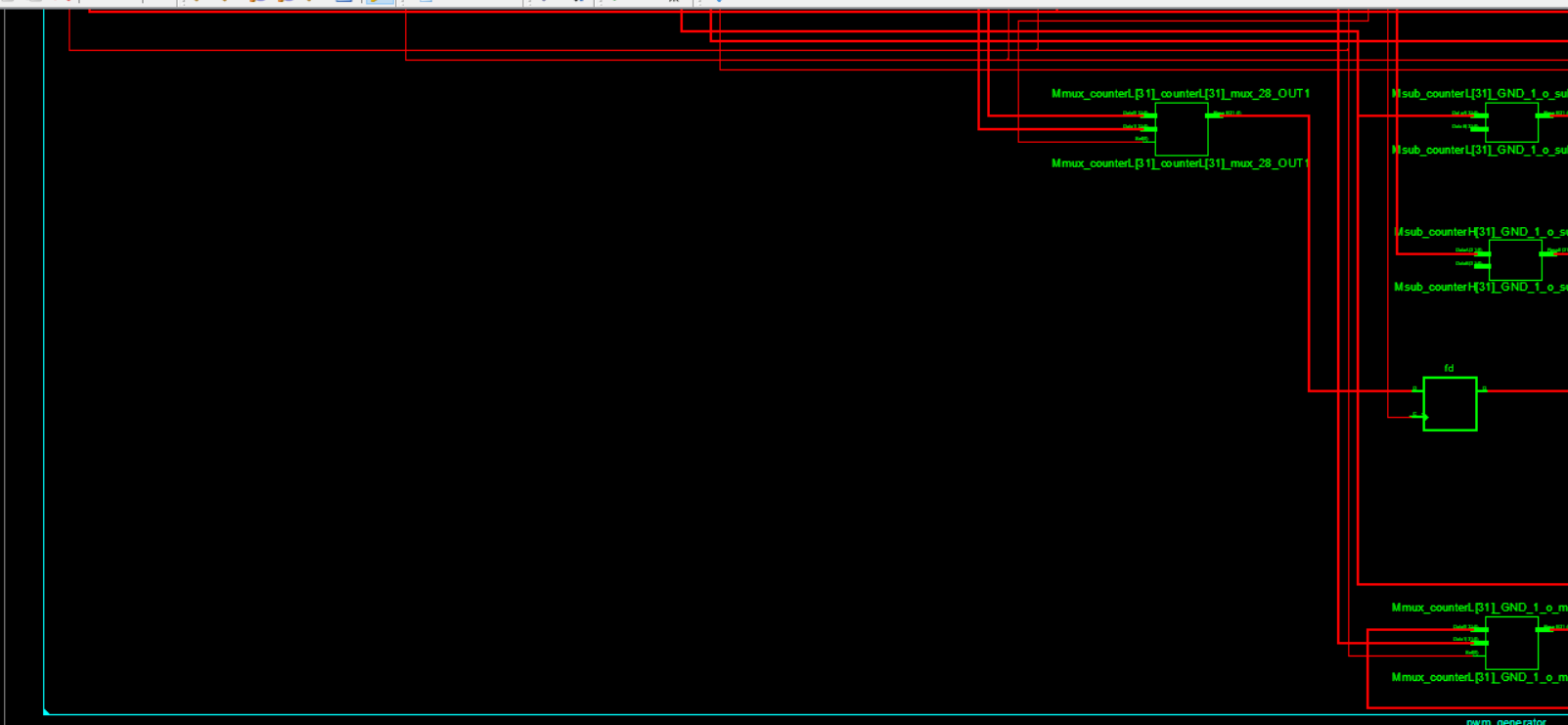
فایلی که برای این بخش فرستاده بودم، قابل سنتز بود. فقط اشتباها برای خروجی 16 بیت در نظر گرفته بودم که لازم نبود. فایل اصلاح شده ضمیمه شد. (تفاوتی در روند اجرا و سنتز ایجاد نمیشود)

نتیجه ی سنتر:

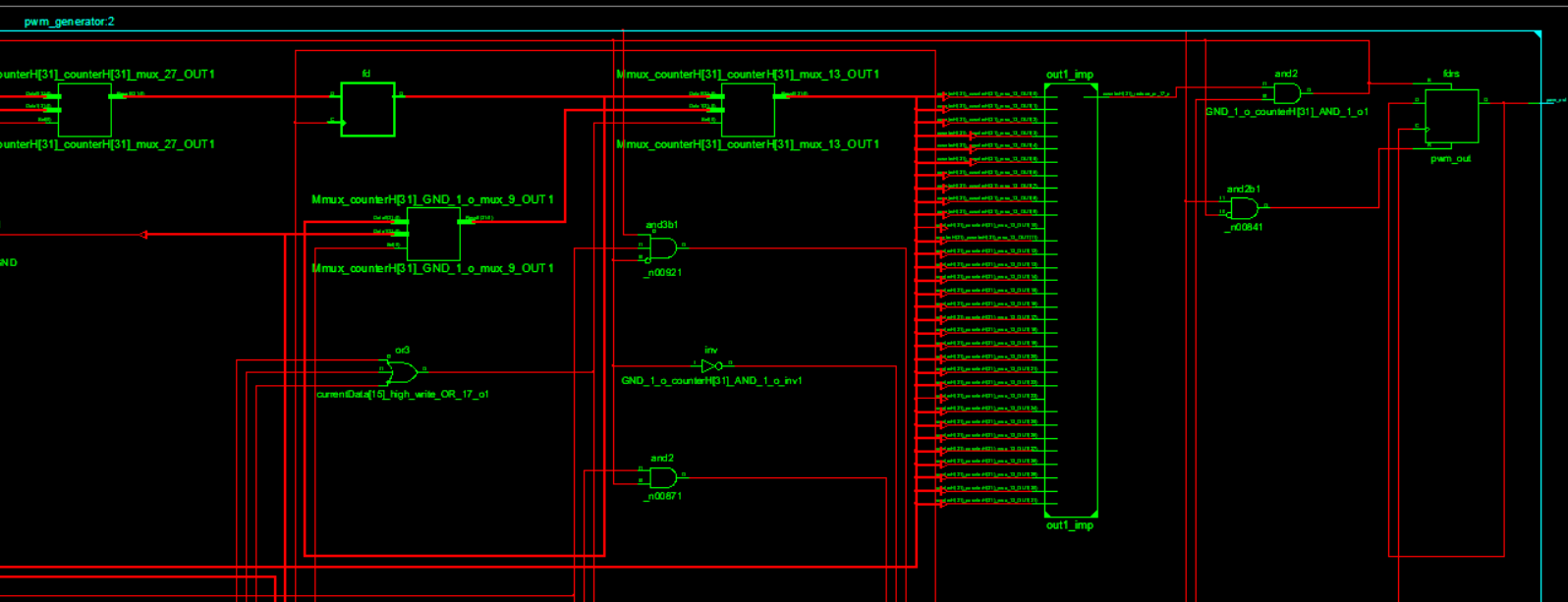
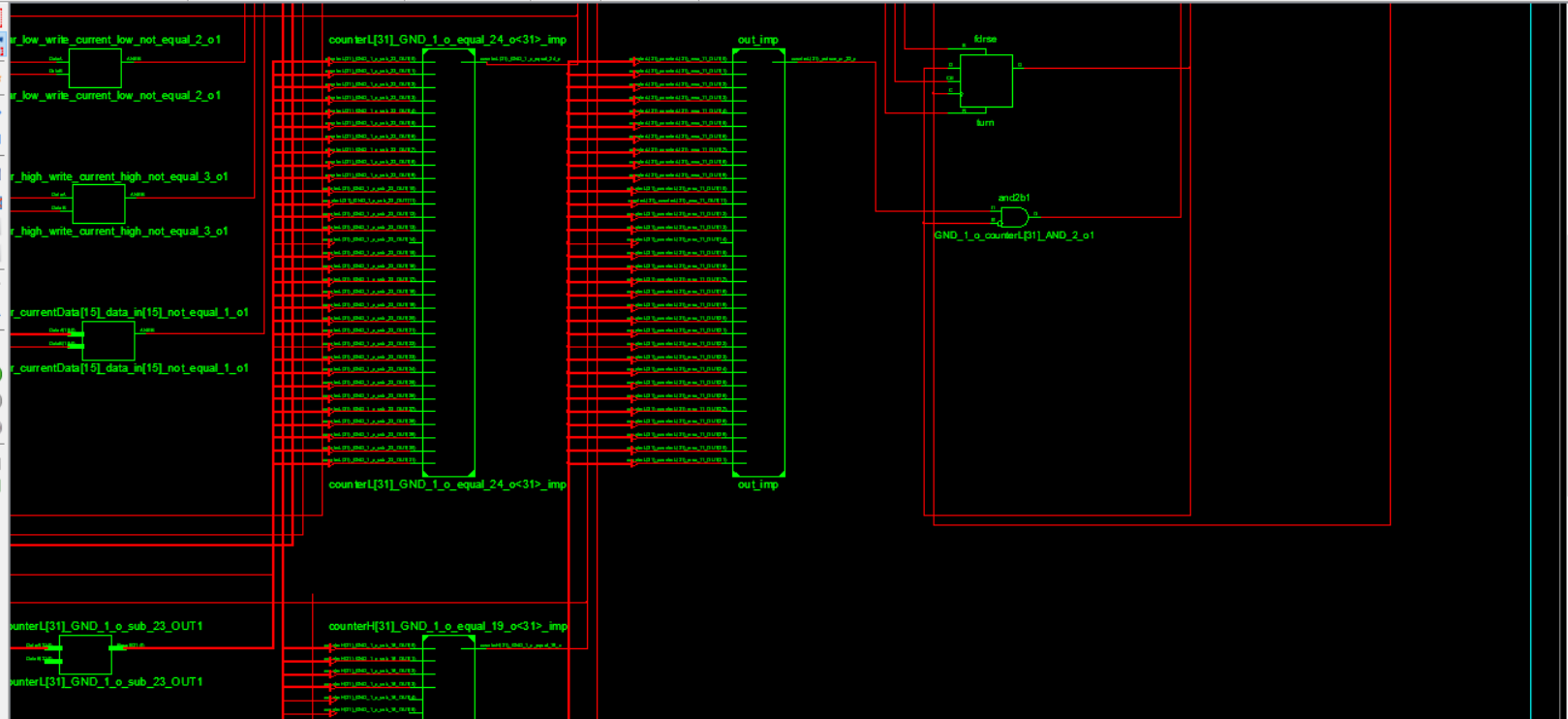
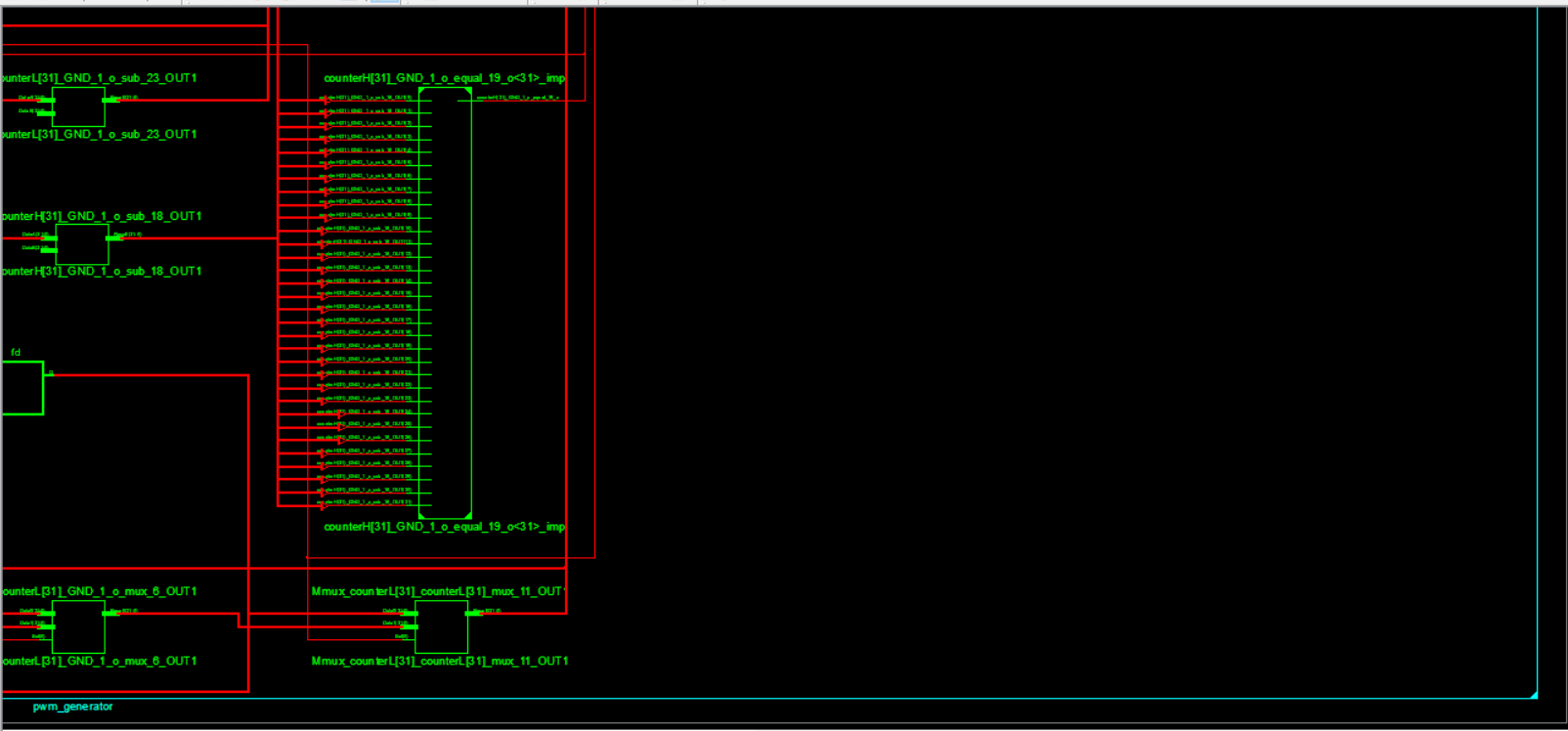




سمت چپ مدار از نزدیک:

سمت راست مدار از نزدیک:

سیاا

اسیبخس\_\_

نسیلسزسیjgeeg

اطلاعات synthesis report :

=========================================================================

\* HDL Synthesis \*

=========================================================================

Synthesizing Unit <pwm\_generator>.

Related source file is "C:\Xilinx\codes\p3\Q2\_1.v".

Found 32-bit register for signal <counterL>.

Found 16-bit register for signal <high\_time>.

Found 32-bit register for signal <counterH>.

Found 16-bit register for signal <currentData>.

Found 1-bit register for signal <current\_low>.

Found 1-bit register for signal <current\_high>.

Found 1-bit register for signal <pwm\_out>.

Found 1-bit register for signal <turn>.

Found 16-bit register for signal <low\_time>.

Found 32-bit subtractor for signal <counterH[31]\_GND\_1\_o\_sub\_18\_OUT> created at line 57.

Found 32-bit subtractor for signal <counterL[31]\_GND\_1\_o\_sub\_23\_OUT> created at line 67.

Found 16-bit comparator not equal for signal <n0000> created at line 37

Found 1-bit comparator not equal for signal <n0002> created at line 37

Found 1-bit comparator not equal for signal <n0005> created at line 37

Summary:

inferred 2 Adder/Subtractor(s).

inferred 116 D-type flip-flop(s).

inferred 3 Comparator(s).

inferred 14 Multiplexer(s).

Unit <pwm\_generator> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 2

32-bit subtractor : 2

# Registers : 9

1-bit register : 4

16-bit register : 3

32-bit register : 2

# Comparators : 3

1-bit comparator not equal : 2

16-bit comparator not equal : 1

# Multiplexers : 14

16-bit 2-to-1 multiplexer : 4

32-bit 2-to-1 multiplexer : 10

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 2

32-bit subtractor : 2

# Registers : 116

Flip-Flops : 116

# Comparators : 3

1-bit comparator not equal : 2

16-bit comparator not equal : 1

# Multiplexers : 136

1-bit 2-to-1 multiplexer : 128

32-bit 2-to-1 multiplexer : 8

=========================================================================

=========================================================================

\* Design Summary \*

=========================================================================

Top Level Output File Name : pwm\_generator.ngc

Primitive and Black Box Usage:

------------------------------

# BELS : 334

# GND : 1

# LUT2 : 3

# LUT3 : 34

# LUT4 : 71

# LUT5 : 2

# LUT6 : 89

# MUXCY : 69

# VCC : 1

# XORCY : 64

# FlipFlops/Latches : 86

# FD : 66

# FDE : 20

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 19

# IBUF : 18

# OBUF : 1

Device utilization summary:

---------------------------

Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice Registers: 86 out of 18224 0%

Number of Slice LUTs: 199 out of 9112 2%

Number used as Logic: 199 out of 9112 2%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 212

Number with an unused Flip Flop: 126 out of 212 59%

Number with an unused LUT: 13 out of 212 6%

Number of fully used LUT-FF pairs: 73 out of 212 34%

Number of unique control sets: 2

IO Utilization:

Number of IOs: 20

Number of bonded IOBs: 20 out of 232 8%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

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=========================================================================

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 86 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: 7.929ns (Maximum Frequency: 126.121MHz)

Minimum input arrival time before clock: 9.694ns

Maximum output required time after clock: 3.634ns

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'

Clock period: 7.929ns (frequency: 126.121MHz)

Total number of paths / destination ports: 291505 / 86

-------------------------------------------------------------------------

Delay: 7.929ns (Levels of Logic = 13)

Source: currentData\_2 (FF)

Destination: turn (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: currentData\_2 to turn

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FDE:C->Q 1 0.447 0.808 currentData\_2 (currentData\_2)

LUT6:I3->O 1 0.205 0.000 Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_lut<0> (Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_lut<0>)

MUXCY:S->O 1 0.172 0.000 Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<0> (Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<1> (Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<2> (Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<3> (Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<4> (Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<4>)

MUXCY:CI->O 33 0.019 0.000 Mcompar\_currentData[15]\_data\_in[15]\_not\_equal\_1\_o\_cy<5> (currentData[15]\_data\_in[15]\_not\_equal\_1\_o)

MUXCY:CI->O 86 0.258 1.785 currentData[15]\_high\_write\_OR\_17\_o1\_cy (currentData[15]\_high\_write\_OR\_17\_o)

LUT4:I3->O 2 0.205 0.981 mux1001221 (counterH[31]\_counterH[31]\_mux\_13\_OUT<4>)

LUT6:I0->O 3 0.203 0.755 GND\_1\_o\_counterH[31]\_AND\_1\_o3 (GND\_1\_o\_counterH[31]\_AND\_1\_o3)

LUT4:I2->O 2 0.203 0.617 GND\_1\_o\_counterH[31]\_AND\_1\_o4\_1 (GND\_1\_o\_counterH[31]\_AND\_1\_o4)

LUT6:I5->O 1 0.205 0.684 turn\_glue\_rst\_SW0 (N98)

LUT6:I4->O 1 0.203 0.000 turn\_glue\_rst (turn\_glue\_rst)

FD:D 0.102 turn

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Total 7.929ns (2.298ns logic, 5.631ns route)

(29.0% logic, 71.0% route)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 278847 / 106

-------------------------------------------------------------------------

Offset: 9.694ns (Levels of Logic = 8)

Source: high\_write (PAD)

Destination: turn (FF)

Destination Clock: clk rising

Data Path: high\_write to turn

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 68 1.222 1.914 high\_write\_IBUF (high\_write\_IBUF)

LUT4:I0->O 1 0.203 0.000 currentData[15]\_high\_write\_OR\_17\_o1\_lut (currentData[15]\_high\_write\_OR\_17\_o1\_lut)

MUXCY:S->O 86 0.411 1.785 currentData[15]\_high\_write\_OR\_17\_o1\_cy (currentData[15]\_high\_write\_OR\_17\_o)

LUT4:I3->O 2 0.205 0.981 mux1001221 (counterH[31]\_counterH[31]\_mux\_13\_OUT<4>)

LUT6:I0->O 3 0.203 0.755 GND\_1\_o\_counterH[31]\_AND\_1\_o3 (GND\_1\_o\_counterH[31]\_AND\_1\_o3)

LUT4:I2->O 2 0.203 0.617 GND\_1\_o\_counterH[31]\_AND\_1\_o4\_1 (GND\_1\_o\_counterH[31]\_AND\_1\_o4)

LUT6:I5->O 1 0.205 0.684 turn\_glue\_rst\_SW0 (N98)

LUT6:I4->O 1 0.203 0.000 turn\_glue\_rst (turn\_glue\_rst)

FD:D 0.102 turn

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Total 9.694ns (2.957ns logic, 6.737ns route)

(30.5% logic, 69.5% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 1 / 1

-------------------------------------------------------------------------

Offset: 3.634ns (Levels of Logic = 1)

Source: pwm\_out (FF)

Destination: pwm\_out (PAD)

Source Clock: clk rising

Data Path: pwm\_out to pwm\_out

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FD:C->Q 2 0.447 0.616 pwm\_out (pwm\_out\_OBUF)

OBUF:I->O 2.571 pwm\_out\_OBUF (pwm\_out)

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Total 3.634ns (3.018ns logic, 0.616ns route)

(83.0% logic, 17.0% route)

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Cross Clock Domains Report:

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Clock to Setup on destination clock clk

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| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | 7.929| | | |

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