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\* HDL Synthesis \*

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Synthesizing Unit <Decision>.

Related source file is "C:\Xilinx\codes\Q1\Decision.v".

Found 2-bit register for signal <result>.

Summary:

inferred 2 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <Decision> synthesized.

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HDL Synthesis Report

Macro Statistics

# Registers : 1

2-bit register : 1

# Multiplexers : 1

2-bit 2-to-1 multiplexer : 1

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\* Advanced HDL Synthesis \*

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Advanced HDL Synthesis Report

Macro Statistics

# Registers : 2

Flip-Flops : 2

# Multiplexers : 1

2-bit 2-to-1 multiplexer : 1

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\* Low Level Synthesis \*

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Optimizing unit <Decision> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Decision, actual ratio is 0.

Final Macro Processing ...

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Final Register Report

Macro Statistics

# Registers : 2

Flip-Flops : 2

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Design Summary \*

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Top Level Output File Name : Decision.ngc

Primitive and Black Box Usage:

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# BELS : 2

# LUT3 : 2

# FlipFlops/Latches : 2

# FD : 2

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 6

# IBUF : 4

# OBUF : 2

Device utilization summary:

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Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice LUTs: 2 out of 9112 0%

Number used as Logic: 2 out of 9112 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 2

Number with an unused Flip Flop: 2 out of 2 100%

Number with an unused LUT: 0 out of 2 0%

Number of fully used LUT-FF pairs: 0 out of 2 0%

Number of unique control sets: 1

IO Utilization:

Number of IOs: 7

Number of bonded IOBs: 7 out of 232 3%

IOB Flip Flops/Latches: 2

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

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clk | BUFGP | 2 |

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Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: 2.337ns

Maximum output required time after clock: 3.597ns

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 6 / 2

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Offset: 2.337ns (Levels of Logic = 2)

Source: out\_wr<0> (PAD)

Destination: result\_0 (FF)

Destination Clock: clk rising

Data Path: out\_wr<0> to result\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 1 1.222 0.808 out\_wr\_0\_IBUF (out\_wr\_0\_IBUF)

LUT3:I0->O 1 0.205 0.000 Mmux\_correct\_guess[1]\_out\_wr[1]\_mux\_2\_OUT11 (correct\_guess[1]\_out\_wr[1]\_mux\_2\_OUT<0>)

FD:D 0.102 result\_0

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Total 2.337ns (1.529ns logic, 0.808ns route)

(65.4% logic, 34.6% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 2 / 2

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Offset: 3.597ns (Levels of Logic = 1)

Source: result\_1 (FF)

Destination: result<1> (PAD)

Source Clock: clk rising

Data Path: result\_1 to result<1>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FD:C->Q 1 0.447 0.579 result\_1 (result\_1)

OBUF:I->O 2.571 result\_1\_OBUF (result<1>)

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Total 3.597ns (3.018ns logic, 0.579ns route)

(83.9% logic, 16.1% route)

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Cross Clock Domains Report:

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Total REAL time to Xst completion: 5.00 secs

Total CPU time to Xst completion: 4.70 secs

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Total memory usage is 4506440 kilobytes