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\* HDL Synthesis \*

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Synthesizing Unit <Frequency\_division>.

Related source file is "C:\Xilinx\codes\Q1\Frequency\_division.v".

Found 3-bit register for signal <cnt>.

Found 1-bit register for signal <newClk>.

Found 3-bit adder for signal <cnt[2]\_GND\_1\_o\_add\_4\_OUT> created at line 21.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 4 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <Frequency\_division> synthesized.

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HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 1

3-bit adder : 1

# Registers : 2

1-bit register : 1

3-bit register : 1

# Multiplexers : 1

3-bit 2-to-1 multiplexer : 1

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\* Advanced HDL Synthesis \*

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Synthesizing (advanced) Unit <Frequency\_division>.

The following registers are absorbed into counter <cnt>: 1 register on signal <cnt>.

Unit <Frequency\_division> synthesized (advanced).

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Advanced HDL Synthesis Report

Macro Statistics

# Counters : 1

3-bit modulo-5 up counter : 1

# Registers : 1

Flip-Flops : 1

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\* Low Level Synthesis \*

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Optimizing unit <Frequency\_division> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Frequency\_division, actual ratio is 0.

Final Macro Processing ...

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Final Register Report

Macro Statistics

# Registers : 4

Flip-Flops : 4

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Design Summary \*

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Top Level Output File Name : Frequency\_division.ngc

Primitive and Black Box Usage:

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# BELS : 4

# LUT2 : 1

# LUT3 : 2

# LUT4 : 1

# FlipFlops/Latches : 4

# FDC : 4

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 2

# IBUF : 1

# OBUF : 1

Device utilization summary:

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Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice Registers: 4 out of 18224 0%

Number of Slice LUTs: 4 out of 9112 0%

Number used as Logic: 4 out of 9112 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 8

Number with an unused Flip Flop: 4 out of 8 50%

Number with an unused LUT: 4 out of 8 50%

Number of fully used LUT-FF pairs: 0 out of 8 0%

Number of unique control sets: 1

IO Utilization:

Number of IOs: 3

Number of bonded IOBs: 3 out of 232 1%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 4 |

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Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: 1.633ns (Maximum Frequency: 612.276MHz)

Minimum input arrival time before clock: 2.335ns

Maximum output required time after clock: 3.634ns

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'

Clock period: 1.633ns (frequency: 612.276MHz)

Total number of paths / destination ports: 12 / 4

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Delay: 1.633ns (Levels of Logic = 1)

Source: cnt\_2 (FF)

Destination: cnt\_0 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: cnt\_2 to cnt\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FDC:C->Q 3 0.447 0.879 cnt\_2 (cnt\_2)

LUT3:I0->O 1 0.205 0.000 Mcount\_cnt21 (Mcount\_cnt2)

FDC:D 0.102 cnt\_2

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Total 1.633ns (0.754ns logic, 0.879ns route)

(46.2% logic, 53.8% route)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 4 / 4

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Offset: 2.335ns (Levels of Logic = 1)

Source: reset (PAD)

Destination: cnt\_0 (FF)

Destination Clock: clk rising

Data Path: reset to cnt\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 4 1.222 0.683 reset\_IBUF (reset\_IBUF)

FDC:CLR 0.430 cnt\_0

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Total 2.335ns (1.652ns logic, 0.683ns route)

(70.8% logic, 29.2% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 1 / 1

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Offset: 3.634ns (Levels of Logic = 1)

Source: newClk (FF)

Destination: newClk (PAD)

Source Clock: clk rising

Data Path: newClk to newClk

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FDC:C->Q 2 0.447 0.616 newClk (newClk\_OBUF)

OBUF:I->O 2.571 newClk\_OBUF (newClk)

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Total 3.634ns (3.018ns logic, 0.616ns route)

(83.0% logic, 17.0% route)

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Cross Clock Domains Report:

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Clock to Setup on destination clock clk

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| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | 1.633| | | |

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Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 4.26 secs