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\* HDL Synthesis \*

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Synthesizing Unit <Winner>.

Related source file is "C:\Xilinx\codes\Q1\Winner.v".

WARNING:Xst:647 - Input <newClk> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Found 32-bit adder for signal <GND\_1\_o\_GND\_1\_o\_add\_15\_OUT> created at line 42.

Found 32-bit adder for signal <GND\_1\_o\_GND\_1\_o\_add\_16\_OUT> created at line 43.

Found 32-bit adder for signal <GND\_1\_o\_GND\_1\_o\_add\_28\_OUT> created at line 53.

Found 32-bit adder for signal <GND\_1\_o\_GND\_1\_o\_add\_29\_OUT> created at line 54.

Found 32-bit adder for signal <GND\_1\_o\_GND\_1\_o\_add\_41\_OUT> created at line 64.

Found 32-bit adder for signal <GND\_1\_o\_GND\_1\_o\_add\_42\_OUT> created at line 65.

Found 32-bit adder for signal <GND\_1\_o\_GND\_1\_o\_add\_54\_OUT> created at line 75.

Found 32-bit adder for signal <GND\_1\_o\_GND\_1\_o\_add\_55\_OUT> created at line 76.

Found 32-bit comparator greater for signal <GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o> created at line 79

Found 32-bit comparator greater for signal <GND\_1\_o\_GND\_1\_o\_LessThan\_64\_o> created at line 81

Found 32-bit comparator equal for signal <GND\_1\_o\_GND\_1\_o\_equal\_65\_o> created at line 83

Summary:

inferred 8 Adder/Subtractor(s).

inferred 3 Comparator(s).

inferred 19 Multiplexer(s).

Unit <Winner> synthesized.

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HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 8

32-bit adder : 8

# Comparators : 3

32-bit comparator equal : 1

32-bit comparator greater : 2

# Multiplexers : 19

2-bit 2-to-1 multiplexer : 3

32-bit 2-to-1 multiplexer : 16

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\* Advanced HDL Synthesis \*

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Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 8

32-bit adder : 8

# Comparators : 3

32-bit comparator equal : 1

32-bit comparator greater : 2

# Multiplexers : 19

2-bit 2-to-1 multiplexer : 3

32-bit 2-to-1 multiplexer : 16

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\* Low Level Synthesis \*

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Optimizing unit <Winner> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Winner, actual ratio is 1.

Final Macro Processing ...

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Final Register Report

Found no macro

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Design Summary \*

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Top Level Output File Name : Winner.ngc

Primitive and Black Box Usage:

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# BELS : 106

# GND : 1

# LUT2 : 4

# LUT3 : 8

# LUT4 : 11

# LUT5 : 12

# LUT6 : 2

# MUXCY : 53

# VCC : 1

# XORCY : 14

# IO Buffers : 12

# IBUF : 10

# OBUF : 2

Device utilization summary:

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Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice LUTs: 37 out of 9112 0%

Number used as Logic: 37 out of 9112 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 37

Number with an unused Flip Flop: 37 out of 37 100%

Number with an unused LUT: 0 out of 37 0%

Number of fully used LUT-FF pairs: 0 out of 37 0%

Number of unique control sets: 0

IO Utilization:

Number of IOs: 13

Number of bonded IOBs: 12 out of 232 5%

Specific Feature Utilization:

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 11.109ns

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis

Total number of paths / destination ports: 2220 / 2

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Delay: 11.109ns (Levels of Logic = 26)

Source: out\_cr<0> (PAD)

Destination: out\_wr<1> (PAD)

Data Path: out\_cr<0> to out\_wr<1>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 7 1.222 1.002 out\_cr\_0\_IBUF (Madd\_GND\_1\_o\_GND\_1\_o\_add\_15\_OUT\_cy<0>)

LUT3:I0->O 1 0.205 0.000 Madd\_GND\_1\_o\_GND\_1\_o\_add\_41\_OUT\_lut<0> (Madd\_GND\_1\_o\_GND\_1\_o\_add\_41\_OUT\_lut<0>)

MUXCY:S->O 1 0.172 0.000 Madd\_GND\_1\_o\_GND\_1\_o\_add\_41\_OUT\_cy<0> (Madd\_GND\_1\_o\_GND\_1\_o\_add\_41\_OUT\_cy<0>)

XORCY:CI->O 2 0.180 0.617 Madd\_GND\_1\_o\_GND\_1\_o\_add\_41\_OUT\_xor<1> (GND\_1\_o\_GND\_1\_o\_add\_41\_OUT<1>)

LUT5:I4->O 1 0.205 0.000 Mmux\_n01231211 (Mmux\_n0123121)

MUXCY:S->O 1 0.172 0.000 Madd\_GND\_1\_o\_GND\_1\_o\_add\_54\_OUT\_cy<1> (Madd\_GND\_1\_o\_GND\_1\_o\_add\_54\_OUT\_cy<1>)

XORCY:CI->O 1 0.180 0.808 Madd\_GND\_1\_o\_GND\_1\_o\_add\_54\_OUT\_xor<2> (GND\_1\_o\_GND\_1\_o\_add\_54\_OUT<2>)

LUT4:I1->O 6 0.205 0.992 Mmux\_GND\_1\_o\_GND\_1\_o\_mux\_60\_OUT231 (GND\_1\_o\_GND\_1\_o\_mux\_60\_OUT<2>)

LUT4:I0->O 1 0.203 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_lut<1> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_lut<1>)

MUXCY:S->O 1 0.172 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<1> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<2> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<3> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<4> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<4>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<5> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<5>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<6> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<6>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<7> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<7>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<8> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<8>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<9> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<9>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<10> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<10>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<11> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<11>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<12> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<12>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<13> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<13>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<14> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<14>)

MUXCY:CI->O 2 0.213 0.961 Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<15> (Mcompar\_GND\_1\_o\_GND\_1\_o\_LessThan\_63\_o\_cy<15>)

LUT5:I0->O 1 0.203 0.579 out\_wr<1>2 (out\_wr\_1\_OBUF)

OBUF:I->O 2.571 out\_wr\_1\_OBUF (out\_wr<1>)

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Total 11.109ns (6.150ns logic, 4.959ns route)

(55.4% logic, 44.6% route)

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Cross Clock Domains Report:

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Total REAL time to Xst completion: 5.00 secs

Total CPU time to Xst completion: 5.16 secs