=========================================================================

\* HDL Synthesis \*

=========================================================================

Synthesizing Unit <Top\_module>.

Related source file is "C:\Xilinx\codes\Q1\Top\_module.v".

N = 8

WARNING:Xst:647 - Input <target\_num<7:4>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:647 - Input <first\_num<7:4>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:647 - Input <second\_num<7:4>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Summary:

no macro.

Unit <Top\_module> synthesized.

Synthesizing Unit <Correlation>.

Related source file is "C:\Xilinx\codes\Q1\Correlation.v".

N = 4

Found 2-bit register for signal <correct\_guess>.

Found 3-bit register for signal <counter>.

Found 10-bit register for signal <out\_cr>.

Found 32-bit adder for signal <GND\_2\_o\_GND\_2\_o\_add\_14\_OUT> created at line 64.

Found 32-bit adder for signal <GND\_2\_o\_GND\_2\_o\_add\_17\_OUT> created at line 64.

Found 32-bit adder for signal <GND\_2\_o\_GND\_2\_o\_add\_20\_OUT> created at line 64.

Found 32-bit adder for signal <GND\_2\_o\_GND\_2\_o\_add\_25\_OUT> created at line 64.

Found 32-bit adder for signal <GND\_2\_o\_GND\_2\_o\_add\_28\_OUT> created at line 64.

Found 32-bit adder for signal <GND\_2\_o\_GND\_2\_o\_add\_31\_OUT> created at line 64.

Found 10-bit adder for signal <out\_cr[7]\_GND\_2\_o\_add\_35\_OUT> created at line 35.

Found 10-bit adder for signal <out\_cr[7]\_GND\_2\_o\_add\_39\_OUT> created at line 42.

Found 10-bit adder for signal <out\_cr[7]\_GND\_2\_o\_add\_43\_OUT> created at line 49.

Found 3-bit adder for signal <counter[2]\_GND\_2\_o\_add\_48\_OUT> created at line 51.

Found 4-bit comparator equal for signal <first\_num[3]\_target\_num[3]\_equal\_2\_o> created at line 18

Found 4-bit comparator equal for signal <second\_num[3]\_target\_num[3]\_equal\_4\_o> created at line 20

Found 1-bit comparator equal for signal <target\_num[0]\_first\_num[0]\_equal\_12\_o> created at line 63

Found 1-bit comparator equal for signal <target\_num[1]\_first\_num[1]\_equal\_14\_o> created at line 63

Found 1-bit comparator equal for signal <target\_num[2]\_first\_num[2]\_equal\_17\_o> created at line 63

Found 1-bit comparator equal for signal <target\_num[3]\_first\_num[3]\_equal\_20\_o> created at line 63

Found 1-bit comparator equal for signal <target\_num[0]\_second\_num[0]\_equal\_23\_o> created at line 63

Found 1-bit comparator equal for signal <target\_num[1]\_second\_num[1]\_equal\_25\_o> created at line 63

Found 1-bit comparator equal for signal <target\_num[2]\_second\_num[2]\_equal\_28\_o> created at line 63

Found 1-bit comparator equal for signal <target\_num[3]\_second\_num[3]\_equal\_31\_o> created at line 63

Found 32-bit comparator greater for signal <GND\_2\_o\_GND\_2\_o\_LessThan\_34\_o> created at line 30

Found 32-bit comparator greater for signal <GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o> created at line 37

Found 32-bit comparator not equal for signal <GND\_2\_o\_GND\_2\_o\_equal\_42\_o> created at line 44

Summary:

inferred 8 Adder/Subtractor(s).

inferred 15 D-type flip-flop(s).

inferred 13 Comparator(s).

inferred 16 Multiplexer(s).

Unit <Correlation> synthesized.

Synthesizing Unit <Frequency\_division>.

Related source file is "C:\Xilinx\codes\Q1\Frequency\_division.v".

Found 3-bit register for signal <cnt>.

Found 1-bit register for signal <newClk>.

Found 3-bit adder for signal <cnt[2]\_GND\_4\_o\_add\_4\_OUT> created at line 21.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 4 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <Frequency\_division> synthesized.

Synthesizing Unit <Winner>.

Related source file is "C:\Xilinx\codes\Q1\Winner.v".

WARNING:Xst:647 - Input <newClk> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Found 32-bit adder for signal <GND\_5\_o\_GND\_5\_o\_add\_15\_OUT> created at line 42.

Found 32-bit adder for signal <GND\_5\_o\_GND\_5\_o\_add\_16\_OUT> created at line 43.

Found 32-bit adder for signal <GND\_5\_o\_GND\_5\_o\_add\_28\_OUT> created at line 53.

Found 32-bit adder for signal <GND\_5\_o\_GND\_5\_o\_add\_29\_OUT> created at line 54.

Found 32-bit adder for signal <GND\_5\_o\_GND\_5\_o\_add\_41\_OUT> created at line 64.

Found 32-bit adder for signal <GND\_5\_o\_GND\_5\_o\_add\_42\_OUT> created at line 65.

Found 32-bit adder for signal <GND\_5\_o\_GND\_5\_o\_add\_54\_OUT> created at line 75.

Found 32-bit adder for signal <GND\_5\_o\_GND\_5\_o\_add\_55\_OUT> created at line 76.

Found 32-bit comparator greater for signal <GND\_5\_o\_GND\_5\_o\_LessThan\_63\_o> created at line 79

Found 32-bit comparator greater for signal <GND\_5\_o\_GND\_5\_o\_LessThan\_64\_o> created at line 81

Found 32-bit comparator equal for signal <GND\_5\_o\_GND\_5\_o\_equal\_65\_o> created at line 83

Summary:

inferred 8 Adder/Subtractor(s).

inferred 3 Comparator(s).

inferred 19 Multiplexer(s).

Unit <Winner> synthesized.

Synthesizing Unit <Decision>.

Related source file is "C:\Xilinx\codes\Q1\Decision.v".

Found 2-bit register for signal <result>.

Summary:

inferred 2 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <Decision> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 17

10-bit adder : 1

3-bit adder : 2

32-bit adder : 14

# Registers : 6

1-bit register : 1

10-bit register : 1

2-bit register : 2

3-bit register : 2

# Comparators : 16

1-bit comparator equal : 8

32-bit comparator equal : 1

32-bit comparator greater : 4

32-bit comparator not equal : 1

4-bit comparator equal : 2

# Multiplexers : 37

10-bit 2-to-1 multiplexer : 7

2-bit 2-to-1 multiplexer : 6

3-bit 2-to-1 multiplexer : 2

32-bit 2-to-1 multiplexer : 22

=========================================================================

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations in this design can share the same physical resources for reduced device utilization. For improved clock frequency you may try to disable resource sharing.

=========================================================================

\* Advanced HDL Synthesis \*

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WARNING:Xst:2677 - Node <out\_cr\_8> of sequential type is unconnected in block <uut1>.

WARNING:Xst:2677 - Node <out\_cr\_9> of sequential type is unconnected in block <uut1>.

Synthesizing (advanced) Unit <Correlation>.

The following registers are absorbed into counter <counter>: 1 register on signal <counter>.

Unit <Correlation> synthesized (advanced).

Synthesizing (advanced) Unit <Frequency\_division>.

The following registers are absorbed into counter <cnt>: 1 register on signal <cnt>.

Unit <Frequency\_division> synthesized (advanced).

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 15

10-bit adder : 1

32-bit adder : 14

# Counters : 2

3-bit modulo-5 up counter : 2

# Registers : 15

Flip-Flops : 15

# Comparators : 16

1-bit comparator equal : 8

32-bit comparator equal : 1

32-bit comparator greater : 4

32-bit comparator not equal : 1

4-bit comparator equal : 2

# Multiplexers : 35

10-bit 2-to-1 multiplexer : 7

2-bit 2-to-1 multiplexer : 6

32-bit 2-to-1 multiplexer : 22

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <Top\_module> ...

Optimizing unit <Correlation> ...

WARNING:Xst:2677 - Node <uut1/counter\_2> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/counter\_1> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/counter\_0> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/out\_cr\_9> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/out\_cr\_8> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/out\_cr\_7> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/out\_cr\_6> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/out\_cr\_5> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/out\_cr\_4> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/out\_cr\_3> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/out\_cr\_2> of sequential type is unconnected in block <Top\_module>.

WARNING:Xst:2677 - Node <uut1/out\_cr\_1> of sequential type is unconnected in block <Top\_module>.

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Top\_module, actual ratio is 1.

FlipFlop uut1/out\_cr\_0 has been replicated 1 time(s) to handle iob=true attribute.

FlipFlop uut1/correct\_guess\_1 has been replicated 1 time(s) to handle iob=true attribute.

FlipFlop uut1/correct\_guess\_0 has been replicated 1 time(s) to handle iob=true attribute.

Final Macro Processing ...

=========================================================================

Final Register Report

Macro Statistics

# Registers : 12

Flip-Flops : 12

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

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No Partitions were found in this design.

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=========================================================================

\* Design Summary \*

=========================================================================

Top Level Output File Name : Top\_module.ngc

Primitive and Black Box Usage:

------------------------------

# BELS : 91

# GND : 1

# LUT2 : 10

# LUT3 : 6

# LUT4 : 5

# LUT5 : 4

# LUT6 : 11

# MUXCY : 47

# VCC : 1

# XORCY : 6

# FlipFlops/Latches : 12

# FD : 2

# FDC : 8

# FDCE : 2

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 20

# IBUF : 13

# OBUF : 7

Device utilization summary:

---------------------------

Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice Registers: 9 out of 18224 0%

Number of Slice LUTs: 36 out of 9112 0%

Number used as Logic: 36 out of 9112 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 37

Number with an unused Flip Flop: 28 out of 37 75%

Number with an unused LUT: 1 out of 37 2%

Number of fully used LUT-FF pairs: 8 out of 37 21%

Number of unique control sets: 3

IO Utilization:

Number of IOs: 33

Number of bonded IOBs: 21 out of 232 9%

IOB Flip Flops/Latches: 3

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

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=========================================================================

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 12 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -3

Minimum period: 1.633ns (Maximum Frequency: 612.276MHz)

Minimum input arrival time before clock: 7.428ns

Maximum output required time after clock: 3.634ns

Maximum combinational path delay: No path found

Timing Details:

---------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 1.633ns (frequency: 612.276MHz)

Total number of paths / destination ports: 16 / 6

-------------------------------------------------------------------------

Delay: 1.633ns (Levels of Logic = 1)

Source: uut2/cnt\_2 (FF)

Destination: uut2/cnt\_0 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: uut2/cnt\_2 to uut2/cnt\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 3 0.447 0.879 uut2/cnt\_2 (uut2/cnt\_2)

LUT4:I1->O 1 0.205 0.000 uut2/newClk\_rstpot (uut2/newClk\_rstpot)

FDC:D 0.102 uut2/newClk

----------------------------------------

Total 1.633ns (0.754ns logic, 0.879ns route)

(46.2% logic, 53.8% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 1754 / 18

-------------------------------------------------------------------------

Offset: 7.428ns (Levels of Logic = 23)

Source: target\_num<1> (PAD)

Destination: uut1/out\_cr\_0 (FF)

Destination Clock: clk rising

Data Path: target\_num<1> to uut1/out\_cr\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 6 1.222 1.089 target\_num\_1\_IBUF (target\_num\_1\_IBUF)

LUT6:I1->O 1 0.203 0.000 uut1/Madd\_GND\_2\_o\_GND\_2\_o\_add\_20\_OUT\_lut<0> (uut1/Madd\_GND\_2\_o\_GND\_2\_o\_add\_20\_OUT\_lut<0>)

MUXCY:S->O 1 0.172 0.000 uut1/Madd\_GND\_2\_o\_GND\_2\_o\_add\_20\_OUT\_cy<0> (uut1/Madd\_GND\_2\_o\_GND\_2\_o\_add\_20\_OUT\_cy<0>)

XORCY:CI->O 1 0.180 0.580 uut1/Madd\_GND\_2\_o\_GND\_2\_o\_add\_20\_OUT\_xor<1> (uut1/GND\_2\_o\_GND\_2\_o\_add\_20\_OUT<1>)

LUT6:I5->O 5 0.205 0.962 uut1/Mmux\_GND\_2\_o\_GND\_2\_o\_mux\_21\_OUT121 (uut1/GND\_2\_o\_GND\_2\_o\_mux\_21\_OUT<1>)

LUT4:I0->O 0 0.203 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_lutdi (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_lutdi)

MUXCY:DI->O 1 0.145 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<0> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<1> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<2> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<3> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<4> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<4>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<5> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<5>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<6> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<6>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<7> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<7>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<8> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<8>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<9> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<9>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<10> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<10>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<11> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<11>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<12> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<12>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<13> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<13>)

MUXCY:CI->O 1 0.019 0.000 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<14> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<14>)

MUXCY:CI->O 2 0.213 0.845 uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<15> (uut1/Mcompar\_GND\_2\_o\_GND\_2\_o\_LessThan\_38\_o\_cy<15>)

LUT3:I0->O 2 0.205 0.616 uut1/\_n0137\_inv1 (uut1/\_n0137\_inv)

FDCE:CE 0.322 uut1/out\_cr\_0

----------------------------------------

Total 7.428ns (3.336ns logic, 4.092ns route)

(44.9% logic, 55.1% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 6 / 6

-------------------------------------------------------------------------

Offset: 3.634ns (Levels of Logic = 1)

Source: uut2/newClk (FF)

Destination: newClk (PAD)

Source Clock: clk rising

Data Path: uut2/newClk to newClk

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 2 0.447 0.616 uut2/newClk (uut2/newClk)

OBUF:I->O 2.571 newClk\_OBUF (newClk)

----------------------------------------

Total 3.634ns (3.018ns logic, 0.616ns route)

(83.0% logic, 17.0% route)

=========================================================================

Cross Clock Domains Report:

--------------------------

Clock to Setup on destination clock clk

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | 1.633| | | |

---------------+---------+---------+---------+---------+

=========================================================================

Total REAL time to Xst completion: 6.00 secs

Total CPU time to Xst completion: 6.13 secs

-->

Total memory usage is 4509832 kilobytes