Experiment #3 – Function Generator

Student Name: Marzieh Bagheri Nia Amiri
Student ID: 810197682

First Part: Design Waveform Generator

1. As stated in instruction, I wrote a Verilog code and test it in Modelsim. The waveform of all 7 functions can be seen in the following picture**.**

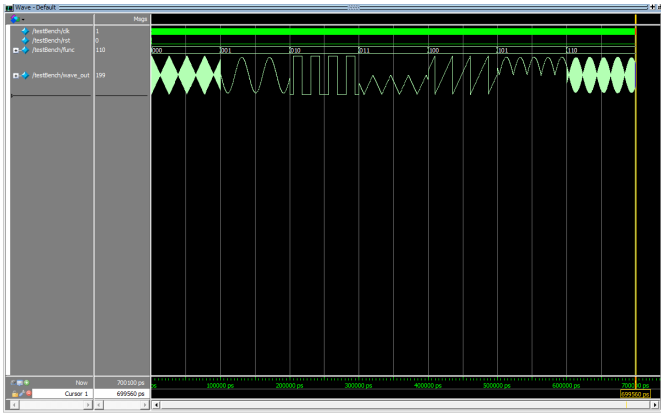

Figure 1

● A clearer picture of Figure1 exists in LAB3 \ WaveformGenerator\ Modelsim folder.
All the above project exists in LAB3\WaveformGenerator\ Modelsim folder.

2, 3. Then we put the written code in Quartus and then we add the 1-port ROM to it; So our waveform Generator is ready. The block diagram of waveform generator can be seen below:

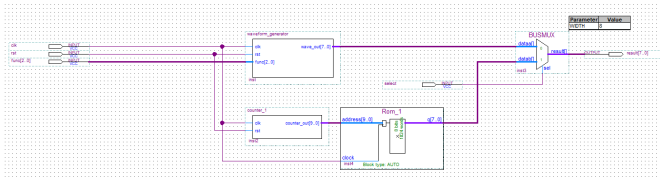

Figure 2

● A clearer picture of Figure2 exists in LAB3 \ Waveform Generator\ Quartus folder.

4. In this section, I write a testbench for my circuit and test it in Modelsim. The waveform of ROM's output can seen below:

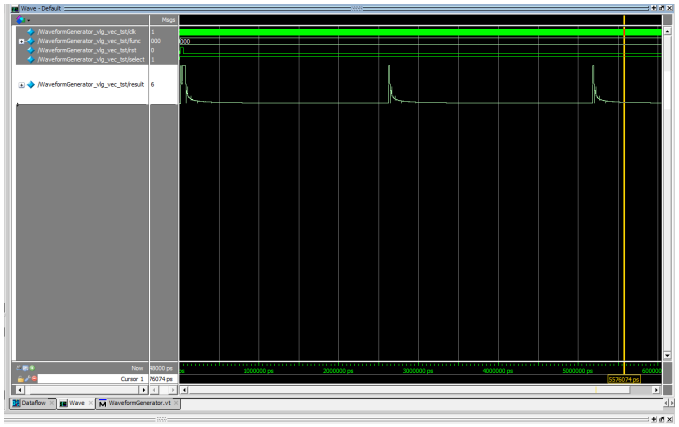

Figure 3

● A clearer picture of Figure3 exists in LAB3 \ WaveformGenerator\ Quartus folder.
All the above project exists in LAB3\WaveformGenerator\ Quartus folder.

Second Part: Design Frequency Regulator

● In last Experiment, I could not complete this section properly, so I used the second method, which was said to be permissible to use. At first, I test my design in Modelsim. In this test, I turned the clock that came out of the ring oscillator into a pulse with 50MHz frequency (T = 20ns). The result of this test can seen below:

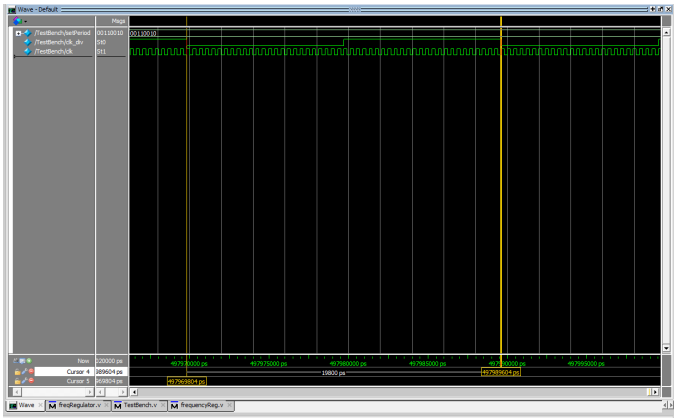

Figure 4

● A clearer picture of Figure4 exists in LAB3 \ FrequencyRegulator\Modelsim folder.
All the above project exists in LAB3\ FrequencyRegulator \Modelsim folder.

1. In this section, we add the FrequencyRegulator to waveform Generator and then we synthesize the whole circuit. The block diagram of waveform generator + frequency selector can be seen below:

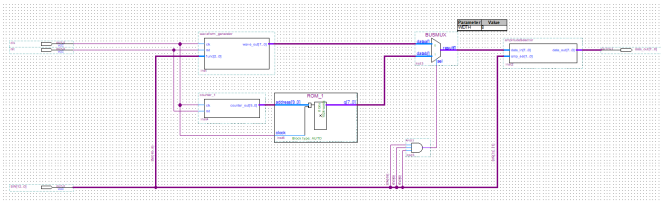

Figure 5

- A clearer picture of Figure5 exists in LAB3\FunctionGenerator \FreqPlusWaveGen folder.

All the above project exists in LAB3\FunctionGenerator \FreqPlusWaveGen folder.

2. I write a simple testbench for this circuit and test it in modelsim with 3 different setPeriods. The following pictures show the result of these three different values:

setPeriod	Achieved Freq	Figure number
25	8MHz	6
50	4MHz	7
100	2MHz	8

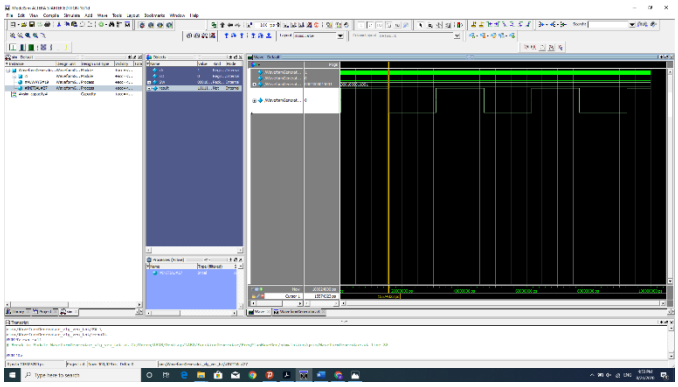

Figure 6

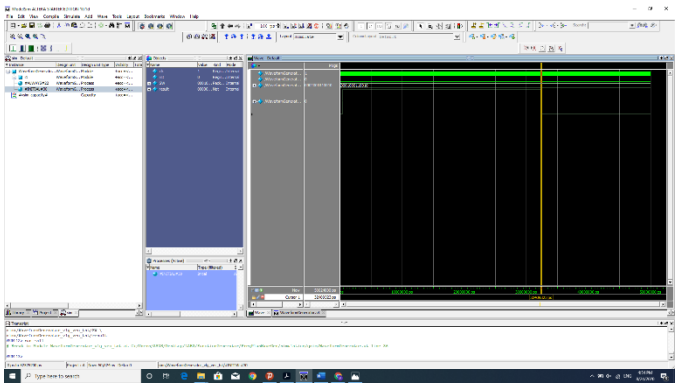

Figure 7

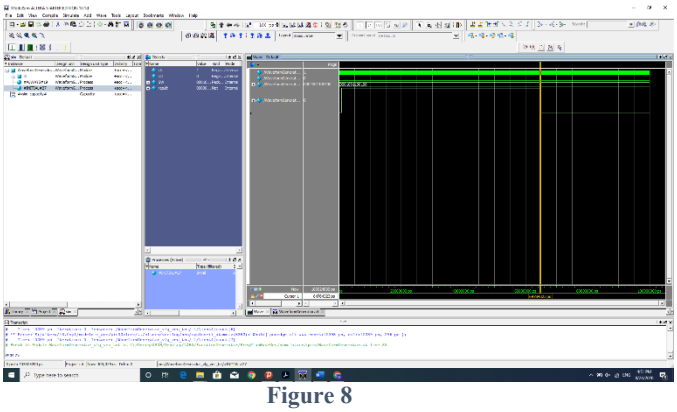

Figure 8

- A clearer pictures of Figure6, Figure7, Figure8 exist in LAB3\FunctionGenerator \FreqPlusWaveGen folder.

Third Part: Design Amplitude Selector

In this part, I write a Verilog code for Amplitude Selector and then test it with a simple testbench in Modelsim. The result can be seen below:

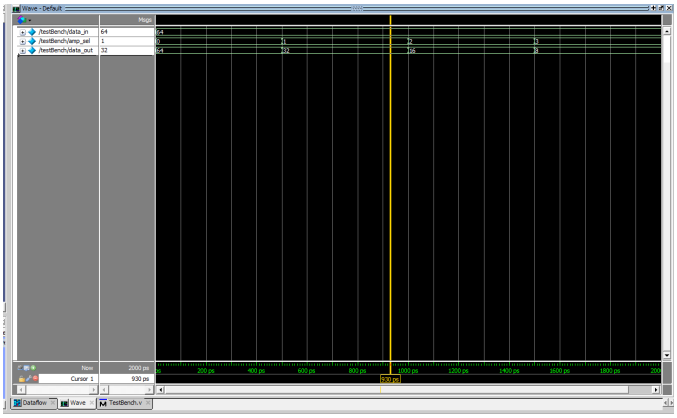

Figure 9

- A clearer picture of Figure9 exists in LAB3 \ AmplitudeSelector folder.

All the above project exists in LAB3 \ AmplitudeSelector folder.

Forth Part: Design Whole project

1. At first we combine Waveform generator, Frequency Selector and Amplitude Selector together. The block diagram of top_level design can be seen below:

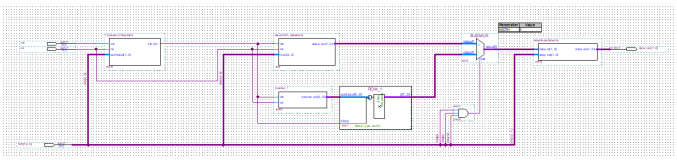

Figure 10

● A clearer picture of Figure10 exists in LAB3\FunctionGenerator \ FunctionGenerator folder.

2. We write a simple testbench for design and test it in Modelsim. The following pictures show two examples of tests performed on the design:

Function	Amplitude Select	Figure number
Square	01	11
Sine	10	12

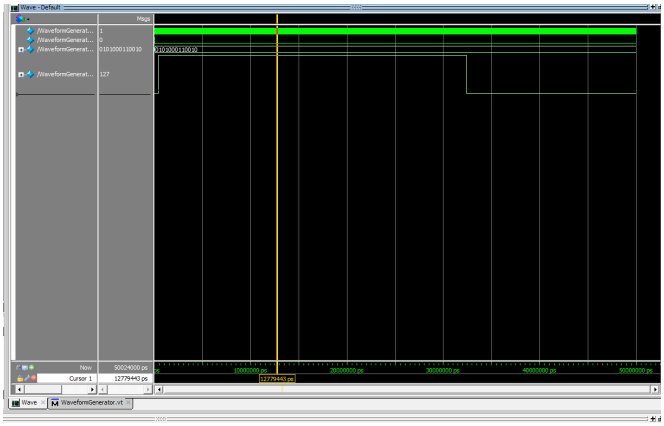

Figure 11

● A clearer picture of Figure11 exists in LAB3\FunctionGenerator \ FunctionGenerator folder.

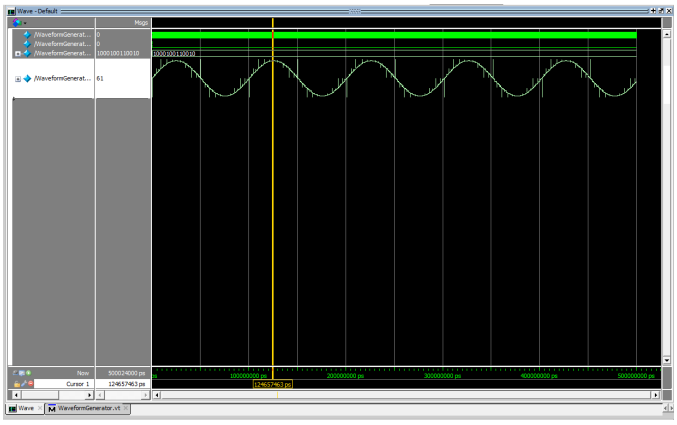

Figure 12

● A clearer picture of Figure12 exists in LAB3\FunctionGenerator \ FunctionGenerator folder.