CCS Model analysis

Sachin

November 3, 2014

1 Introduction

Accurate delay calculation is critical for timing closure of complex digital designs. A delay model is needed that enables accuracy close to circuit simulation. The model must support calculation of cell delay, interconnect delay, pin slew (also called "transition time") and input pin capacitance for stages. This document analyses Synopsys Composite Current Source model for timing (CCS Timing) while answering some other key questions related to the topic.

1.1 What is a timing model?

Delay calculation is performed for one stage at a time, where a stage consists of the driving cell arc, the output RC network, and the capacitance of the network load pins. The goal is to compute the response at the driver output and at the network load pins, given an input slew or waveform at the driver input. The computed responses are then used to determine the cell delay for the driver and the input slews at the load pins
To perform stage delay calculation efficiently, three models are created: the driving cell arc is replaced by a driver model; the interconnect RC network is replaced by a reduced order model, and the load pins are replaced by a receiver model
Some key definitions

1. slew rate/slew: the maximum rate of change of output voltage per unit of time and is expressed as volt per second
2. Output load: voltage metric of whatever device connected at the end of the circuit which consumes the current.
3. Delay tables: input slew vs output capacitance values. i.e all diff delay values for each combn of input slew and o/p cap

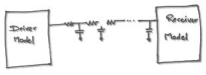

Figure 1: Driver-Receiver model

2 Problems with existing timing models

The widely available Non-Linear Delay and Power Models (NLDM/NLPM) have served the IC design industry for over 5 years. These models consist of tables capturing a cell's delay or power for each combination of input slew and output load. At process geometries of 90-nm and below, many new effects can no longer be modeled using this approach. They include:

1. High impedance interconnect: impedance(z) is opposition to current flow. $z = R + jXc$ - reistance + reactance(due to capacitor,inductor etc). So, at 90nm or below, the immpedance due to interconnect would be huge
2. Miller Effect - the Miller effect accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of the effect of capacitance between the input and output terminals. The virtually increased input capacitance due to the Miller effect is given by $C_M = C(1 + A_v)$ where $-A_v$ is the gain of the amplifier and C is the feedback capacitance.
3. Dynamic IR drop - Due to the resistance of the interconnects constituting the network, there is a voltage drop across the network, commonly referred to as the IR-drop
4. Multi Voltage - beacuase of the drop, there will be more than one voltage runnninng through the circuit
5. Temperature Inversion - With increase in temperature, the free electrons acquire more energy and start to travel faster inside the pn-junction. this causes a decrease in delay.
6. Large number of cells
7. Increasing variations

3 Solution: CCS model for timing analysis

The timing calulation in the CCS model has the following requirements

1. Driver model - drive arbitrary interconnect, including high impedance nets
2. Receiver model - complex input capacitance
3. Vdd (drain) and temp scaling for IR drop, mmulti-Vdd, DVFS(dynamic voltage frequency scaling)

In this model, the driver model is a time and voltage dependent current source with an essentially infinite drive-resistance, which provides high accuracy even when R_d is much less than Z_{net}. It describes how a timing arc propagates a transition from input to output, and how it can drive arbitrary RC networks. The receiver model describes the capacitance that an input pin presents to driving cells. Now consider driving a detailed parasitic network. At a given timestep we can apply the output currents from our pre-characterization to the network. There

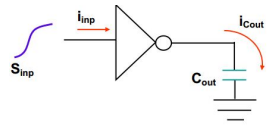

Figure 2: CCS Characterization

will be a unique current that will elicit the same voltage on both a lumped capacitance and the network at the given timestep. This current is the chosen value for the given timestep, and we reapply this procedure at every subsequent timestep CCS Timing delay calculation uses advanced interpolation technology to determine a current waveform when the input slew and/or output load values do not match those used during cell characterization. Additionally, interpolation is used for intermediate values of VDD and temperature by using data from multiple libraries.

4 CCS Characterization

Characterizing a cell timing arc for CCS Timing is very similar to characterization for nonlinear delay models (NLDM): an input stimulus is chosen to produce a specific input slew time (Sinp) ; a load capacitance (Cout) is connected to the output pin; and a circuit simulation is run in the same way as for NLDM. But instead of measuring voltage thresholds at the output pin, current is measured through the load capacitor and into the input pin. The current through Cout is used for the driver model, and the current into the input pin is used to determine the receiver model.

5 Comparison of the CCS and NLDM models

	NLDM	CCS
Measurement at input	input current and voltage at input pin for receiver model	input current and voltage at input pin for receiver model
Measurement at output	cell delay and output slew	current through load capacitance for driver model
capacitances	Has only one Capacitance	Has 2 capacitances C1 and C2.

The two capacitances C1 and C2 are used to accurately reflect effect of miller capacitance on input capacitance and net-delay. For STA delay calculation, C1 is used in net delay calculation before receiver waveform hits delay threshold point and C2 is used in net delay calculation after receiver waveform hits delay threshold point.

Synopsys delay calculation with CCS Timing includes powerful nonlinear Vdd scaling for timing check arcs. This results in better correlation to circuit simulation than with simple linear interpolation approaches

6 Conclusion

CCS Timing is an enabling technology for high-accuracy delay calculation at 90nm and below. Stage delay accuracy is typically within 2% of golden circuit simulation results. The powerful receiver model captures dependence on input slew, output load, direction of switching, and cell state. The (two-capacitance)(why and how?) approach enables a dynamic calculation that closely matches circuit simulation for inputs susceptible to Miller effect. The CCS driver model can be applied to arbitrary interconnect networks, and produces excellent results on difficult high-impedance nets.
CCS Timing enables scaling for intermediate VDD and temperature values. Library characterization is done for a small number of Vdd values, with advanced current waveform interpolation at runtime. Calculation can be done for any instance-specific value in a continuous range of Vdd. This is a key element of flows considering the timing effect of IR drop, and also supports multi-Vdd and DVFS (Dynamic Voltage and Frequency Scaling) designs. CCS Timing scaling also supports delay calculation for arbitrary temperature values between characterization points.