Quiz 10 Chapter 9

Multiple Choice Questions

1. Computing systems need cache because
A) accessing main memory is slow and cache speeds it up.
B) register access is slow and cache speeds it up.
C) main memory is expensive and cache offsets the cost.
D) All of the about.

2. Which of the following statement is correct?
A) Base register holds the size of a process.
B) Limit register holds the size of a process.
C) Base and limit registers can be loaded by the standard load instructions in the instruction set.
D) Any attempt by a user program to access memory at an address higher than the base register value results in a trap to the operating system.

3. If the base register is loaded with value 12345 and limit register is loaded with value 1000, which of the following memory address access will not result in a trap to the operating system?
A) 12500
B) 12200
C) 13346
D) 12344

4. Assume the value of the base and limit registers are 1200 and 350 respectively. Which of the following addresses is legal?
A) 355
B) 1200
C) 1551
D) all of the above

5. _____ is the method of binding instructions and data to memory performed by most general-purpose operating systems.
A) Interrupt binding
B) Compile time binding
C) Execution time binding
D) Load-time binding

6. If the starting address location changes, in which of the following cases, the program has to be recompiled?
A) Execution time binding.
B) Load time binding.
C) Compile time binding
D) Both compile and load time bindings.

7. If execution time binding is used,
A) logical addresses of process may change over time but physical addresses remain the same.
B) physical addresses of process may change over time but logical addresses remain the same.
C) both physical and logical addresses may change over time.
D) both physical and logical addresses remain the same over time.

Quiz 10 Chapter 9

8. Suppose the size of a process is 10,000 bytes and the relocation register is loaded with value 5000, which of the following memory address this process can access?
A) logical address 10,350
B) physical address 4,500
C) physical address 10,350
D) None of the above

9. An address generated by a CPU is referred to as a ____.
A) physical address
B) logical address
C) post relocation register address
D) Memory-Management Unit (MMU) generated address

11. Which of the following is true about dynamic storage allocation?
A) Worst fit provides the best storage utilization.
B) First fit requires less time for allocation than worst fit on average.
C) Best fit is clearly better than first fit in terms of time and storage utilization.
D) First fit is clearly better than best fit in terms of time and storage utilization.

12. External fragmentation is
A) when there is some unused memory that cannot be allocated to a process.
B) when the amount of available memory is less than the size of a process.
C) when a process is broken up into smaller parts for memory allocation.
D) when there is enough total memory space to satisfy a request but the available spaces are not contiguous.

13. Consider a logical address with 18 bits used to represent an entry in a conventional page table. How many entries are in the conventional page table?
A) 262,144 (2^18)
B) 1,024 (2^10)
C) 1,048,576 (2^30)
D) 18

15. A large page size results in
A) lower internal fragmentation
B) larger page table overhead
C) efficient disk I/O
D) All of the above

16. A frame table stores
A) which frames are allocated.
B) which frames are free.
C) total number of frames.
D) All of the above.

17. A(n) _____ matches the process with each entry in the TLB.
A) address-space identifier
B) process id
C) stack
D) page number

Quiz 10 Chapter 9

18. A page-table base register stores
A) a pointer to the page table in memory.
B) the starting logical address of the page currently being accessed.
C) the starting physical address of the frame currently being addressed.
D) the page size of the page currently being accessed.

19. A translation look-aside buffer is used to
A) cache page table entries.
B) store the address of the page table in memory.
C) size of the logical address space of the currently running process.
D store page size.

20. The protection bit in a page table
A) provides protection against unauthorized updates in the page table.
B) marks a page table as read-only or read-write.
C) marks a frame as read-only or read-write.
D) All of the above.

21. Reentrant code is easier to share when paging is used, because
A) each process can modify that code its own way.
B) the code doesn't change during execution.
C) the code changes are identical for each process.
D) All of the above.

24. The _____ binding scheme facilitates swapping.
A) interrupt time
B) load time
C) assembly time
D) execution time

25. The roll out, roll in variant of swapping is used ____.
A) when a backing store is not necessary
B) for the round-robin scheduling algorithm
C) for priority-based scheduling algorithms
D) when the load on the system has temporarily been reduced

26. A page out operation
A) moves a page from memory to the backing store.
B) moves a page from the backing store to memory.
C) moves a page from one frame to another.
D) deletes a page from the backing store.

Essay Questions
2. What is the advantage of using dynamic loading?

better space utilization

Quiz 10 Chapter 9

3. When does external fragmentation occur?

4. Distinguish between internal and external fragmentation.

5. Explain the basic method for implementing paging.

cpu scheduling increases priority of process

6. Describe how a logical address is translated to a physical address.

10. What is the context switch time, associated with swapping, if a disk drive with a transfer rate of 2 MB/s is used to swap out part of a process that is 200 KB in size? Assume that no seeks are necessary and that the average latency is 15 ms. The time should reflect only the amount of time necessary to swap out the process.

200 KB = 0.2 MB || 0.2 MB / 2 MB/s = 0.1 s || 0.1 s + 15 ms = 0.115 s

True/False Questions

1. A relocation register is used to check for invalid memory addresses generated by a CPU.
F

2. Fragmentation does not occur in a paging system.
F

3. A 32-bit logical address with 8 KB page size will have 1,000,000 entries in a conventional page table.
F

4. Without a mechanism such as an address-space identifier, the TLB must be flushed during a context switch.
T

5. There is a 1:1 correspondence between the number of entries in the TLB and the number of entries in the page table.
F

6. Reentrant code cannot be shared.
F

12. In swapping with paging technique, individual pages of a process are swapped in or out.
T

Quiz 10 Chapter 9