**Lab 8-9: Time**

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CPET 241 Digital Systems Design

Lab Section 1

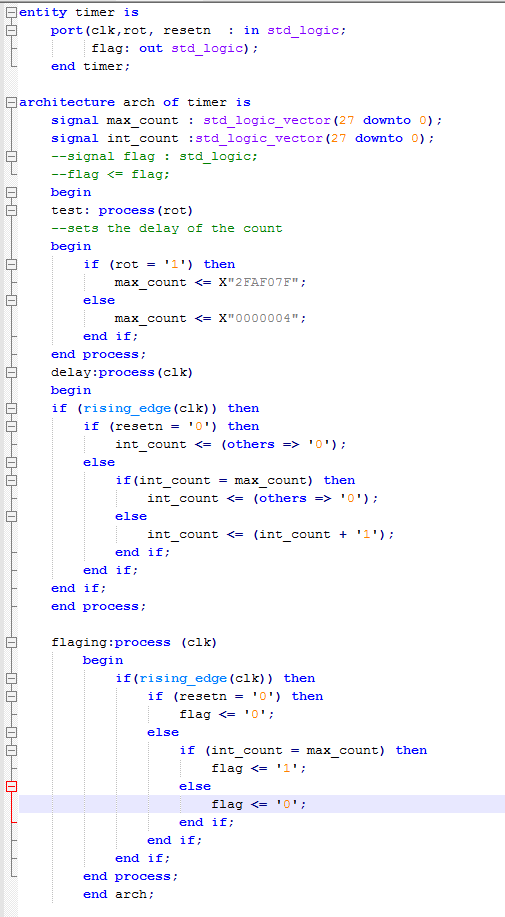
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**Abstract:** Over the course of two weeks, time tracking was tested digitally. This was done by the first deisigning a real time clock, and then a stopwatch. Both of these timers were designed using VHDL and tested on the Altera DE2 board where it was displayed on a Seven Segment Display and then the stopwatch was tested using an oscilloscope

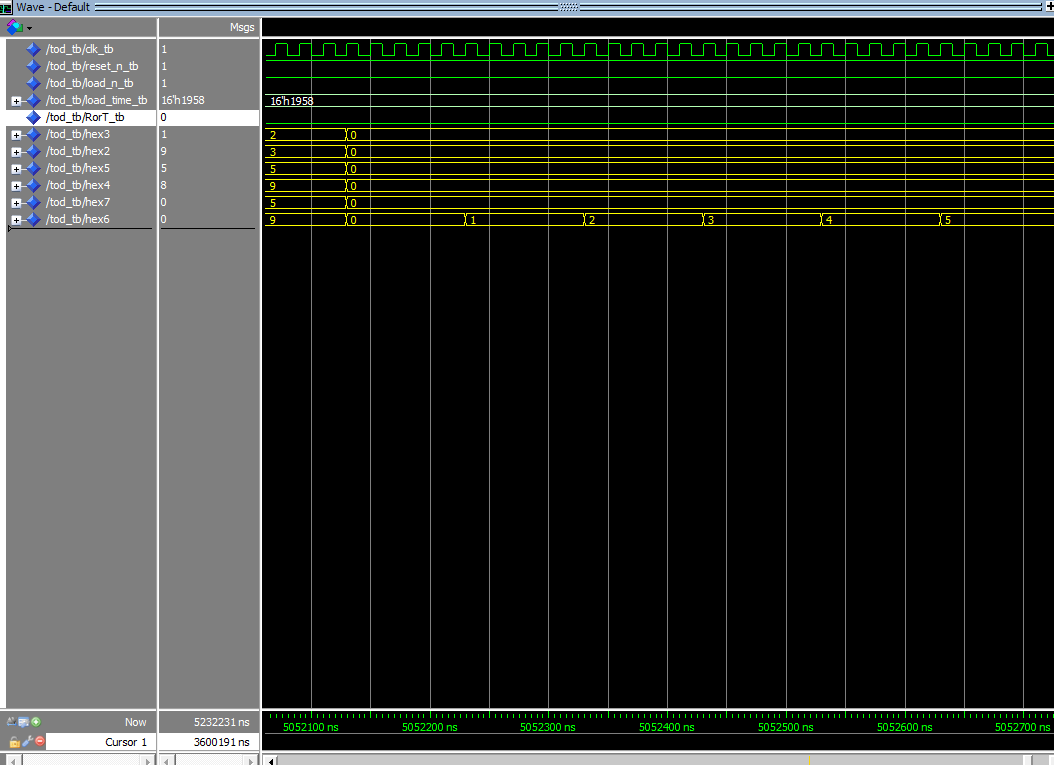
**Procedure:** For the first week of the exercise, a real time clock was developed in Quartus II using VHDL. The main file is shown in Figure 1

**Figure 1**

Figure 1 does not show all the code of the main vhdl file. What it shows is how the program will make sure the timer does not go over numerically at all, meaning that seconds and minute will rollover at 59, and hour will rollover at 23. The timer is shown in Figure 2.

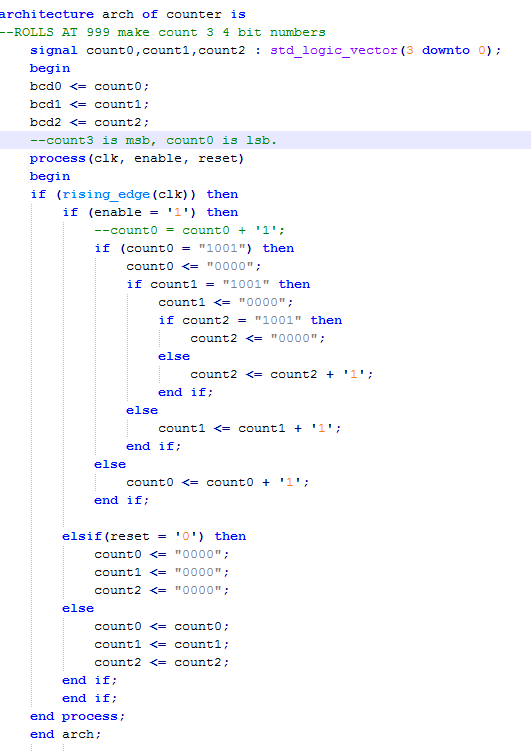
**Figure 2**

Rot picks whether the delay should be on or not. This lets us test the timer more efficiently. The flag that is outputted in this VHDL file is the count in the main file. The program is also set up so that the time can be set by the switches on the Altera DE2 board. Once the VHDL was written and complied correctly, the program was tested using modelsim. When the count equals the max count, a flag will be sent out. This Flag is used during the Osicilloscope test during the second week.The results of this test are shown by Figure 3.



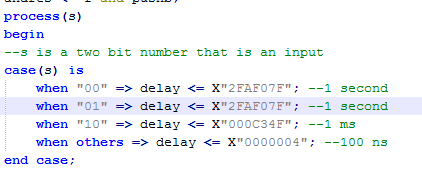
**Figure 3**

Figure 3 shows that Hour, minutes and seconds all rollover correctly. Now that this is verified to be correct, the program was uploaded to the Altera DE2 board where the results also matched the waveform shown in Figure 3.

 The next week, a stopwatch was developed using the same process. Since the timer that is shown in Figure 2 was already written, it was used in the stopwatch as well. The VHDL for this is shown in Figure 4.

**Figure 4**

Figure 4 is written similarly to the code written in Figure 1, however this program counts to only 999 with count0 being the least significant bit, and count2 being the most significant. This program also had a delay however it was done a little differently as shown in Figure 5.

**Figure 5**

In this program, the delay is selected by s, a two bit number that is an input. When the select is 0 or 1, the delay equals 1 second, when the select is 2 the delay is 1 ms, and when the select is 3 the delay is 100 ns. Once the program complied correctly the program was tested in Modelsim using the waveform generator as shown by Figure 6.

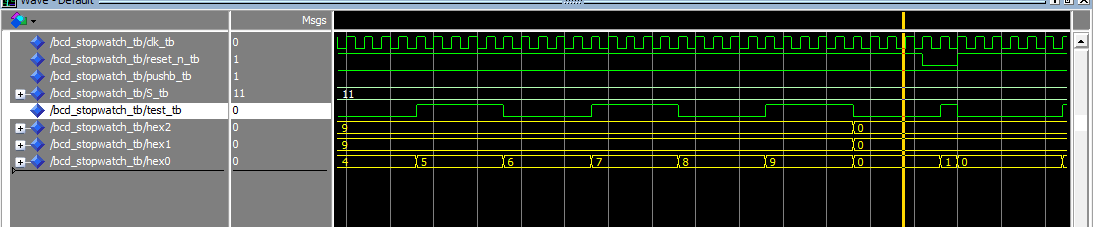
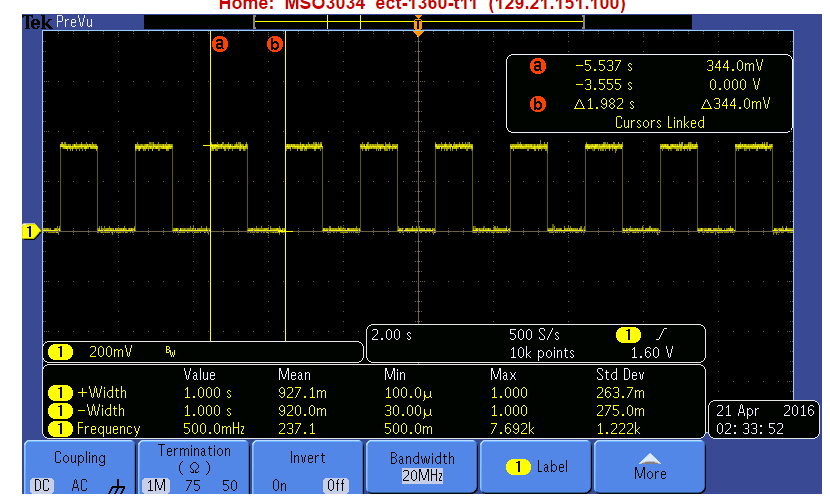
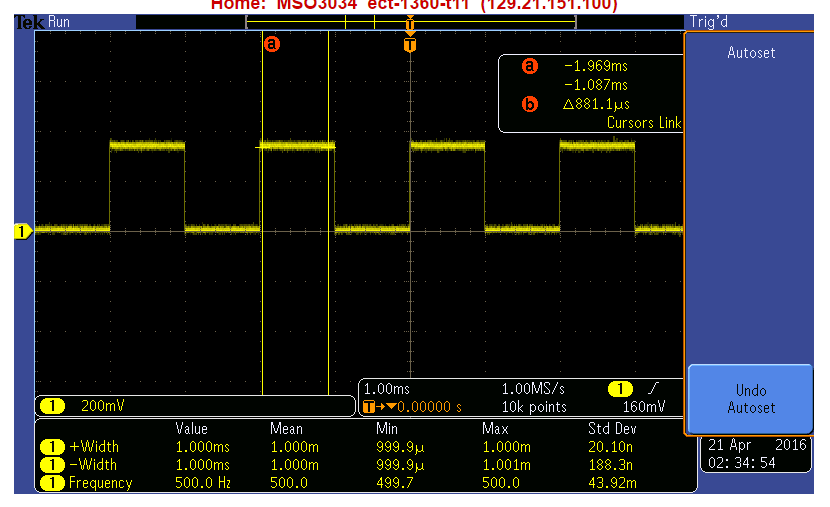
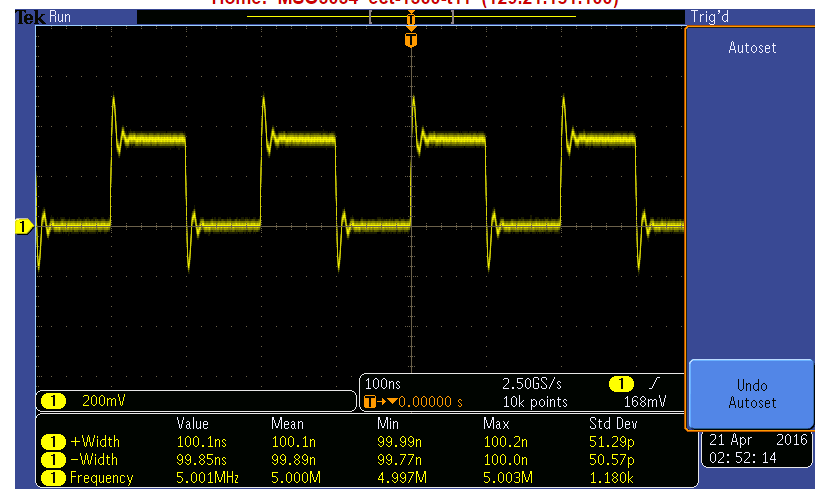
**Figure 6**

Figure 6 shows that at 999, the stopwatch resets to 000. This verified that the program works as intended. The program was then uploaded to the Altera DE2 board, where the results were also correct. The last and final test was testing it with the oscilloscope. The flag that was made in Figure 2 is used here. The Flag actually generates a square wave since it goes to 1 whenever the count is equal to the Max count. This is shown by Figures 7 to 9.



**Figure 7- 1 second delay**

**Figure 8 – 1 ms delay**

**Figure 9- 100 ns**

The oscilloscope measure the width to be the appropriate time in each figure meaning that the data is correct.

Conclusion: The purpose of this experiment, was to track time using digital logic and to then to have it test it using the oscilloscope. This was done over two weeks by first making a Real time Digital Clock, and then a stopwatch.