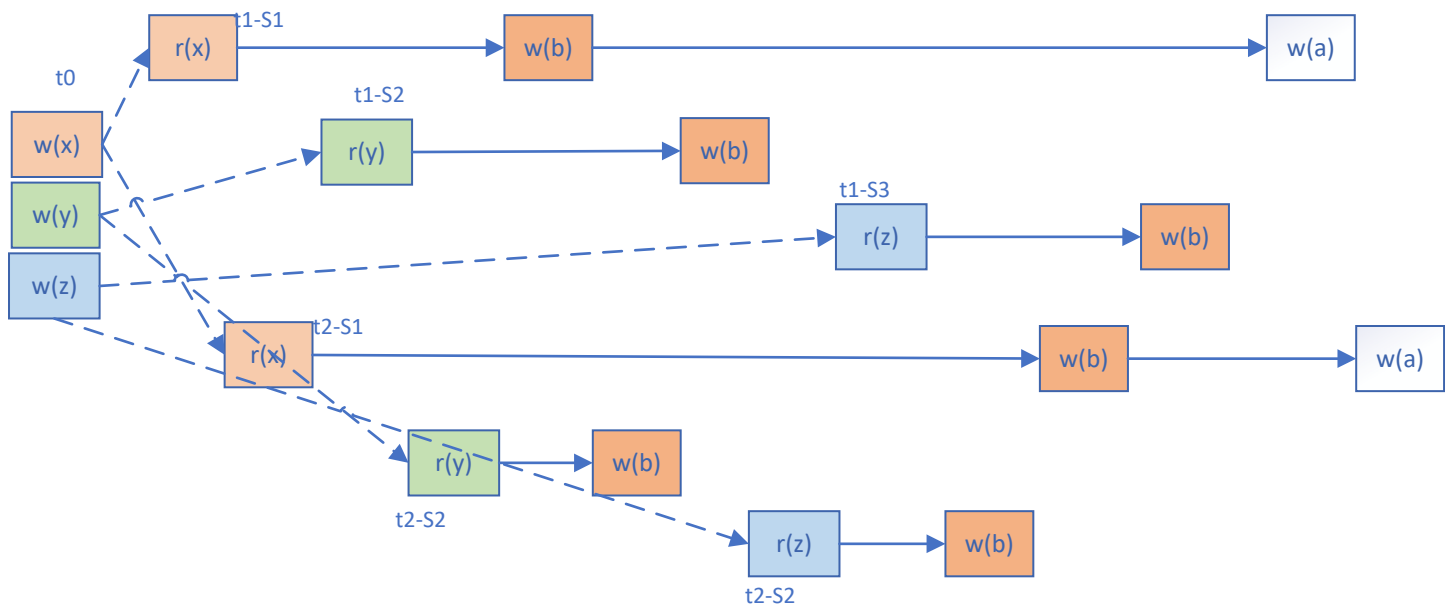
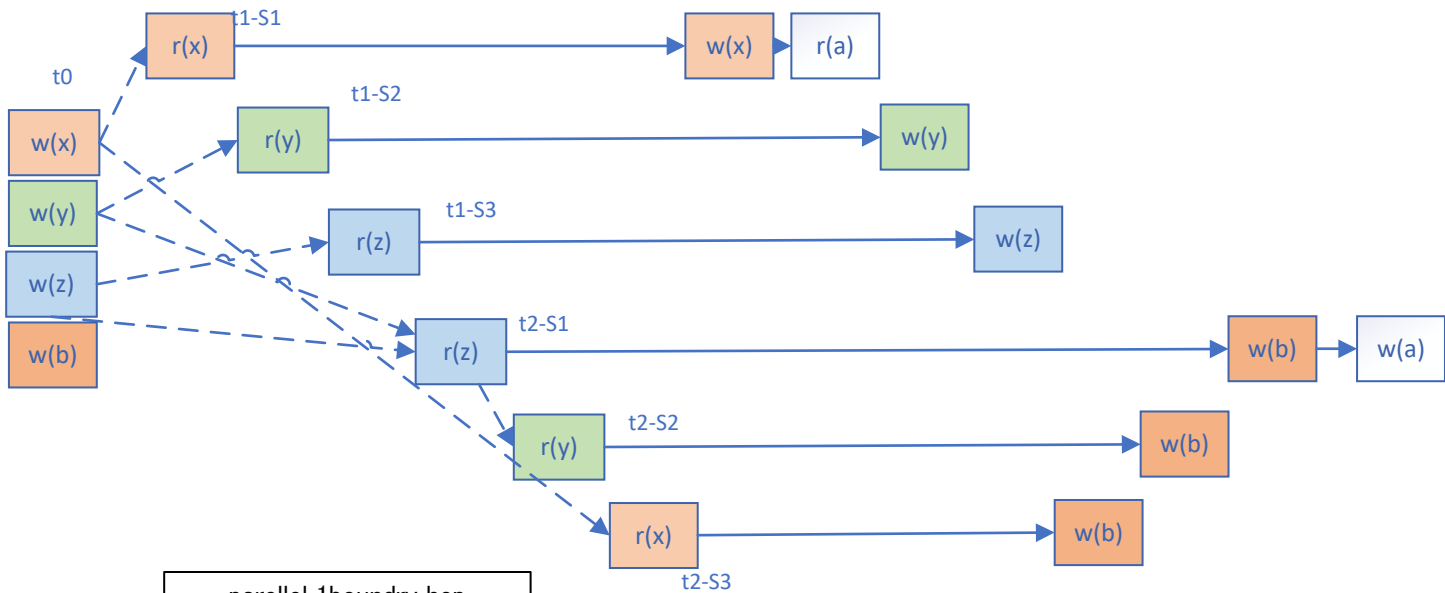


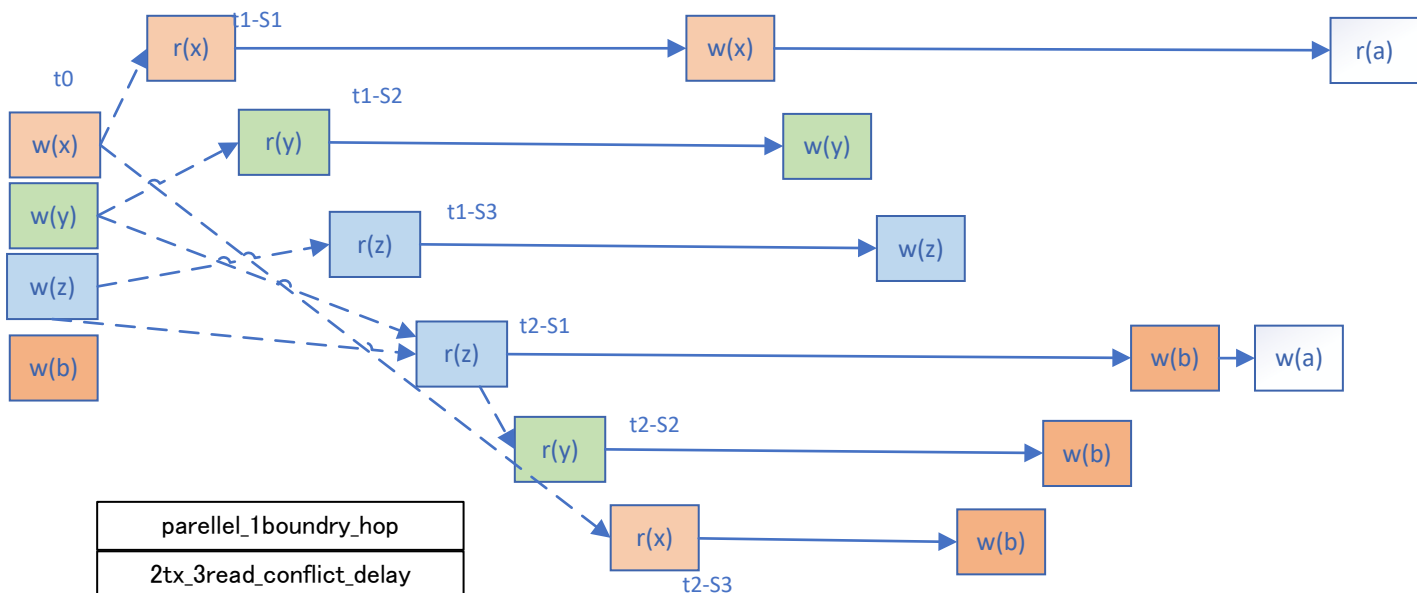
parallel	
2tx_3read_1write_no_conflict	
t_1	c bd:t1
t_2	c bd:t2
read b	t_2



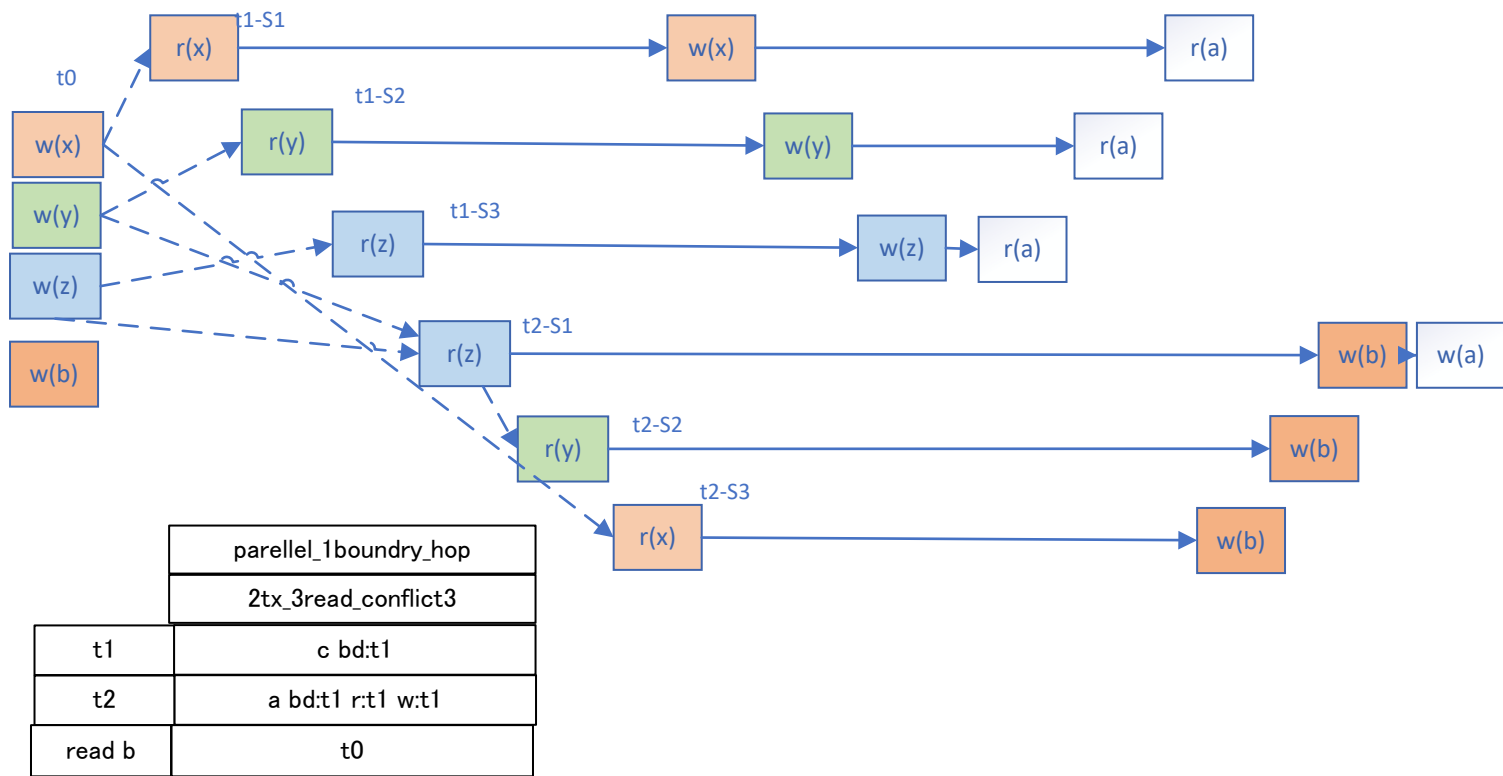
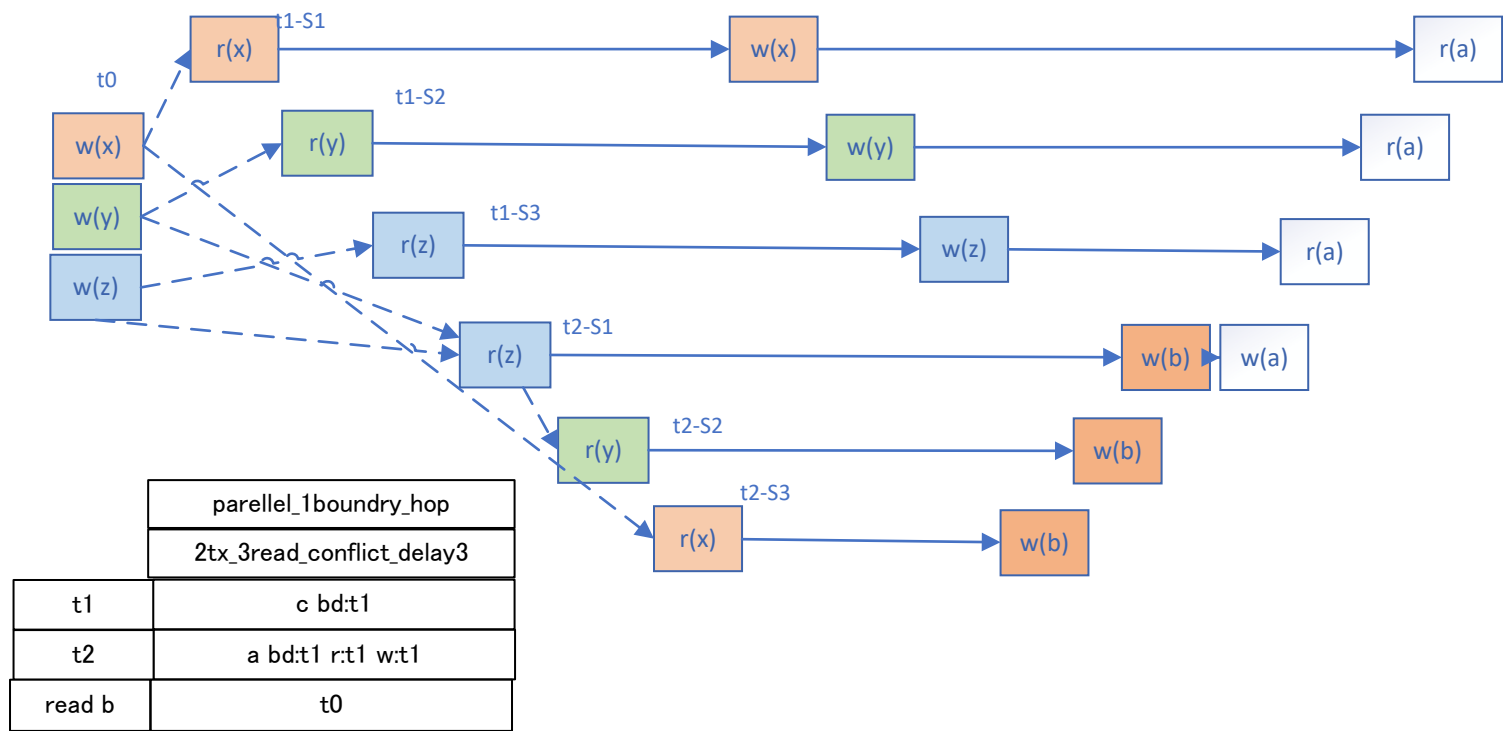
parallel	
2tx_3read_3write_no_conflict	
t_1	c bd:t1
t_2	c bd:t2
read b	t_2 :S1

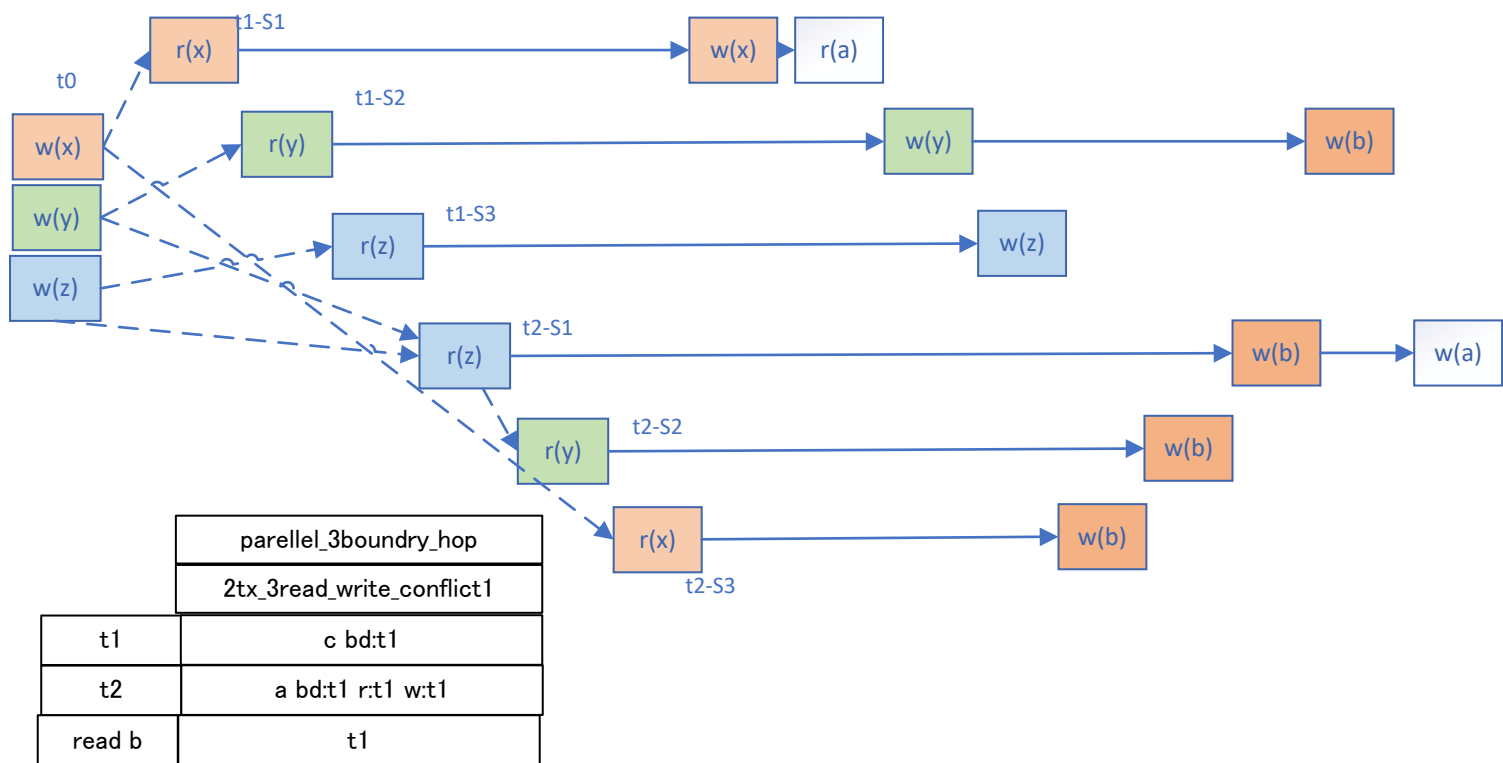
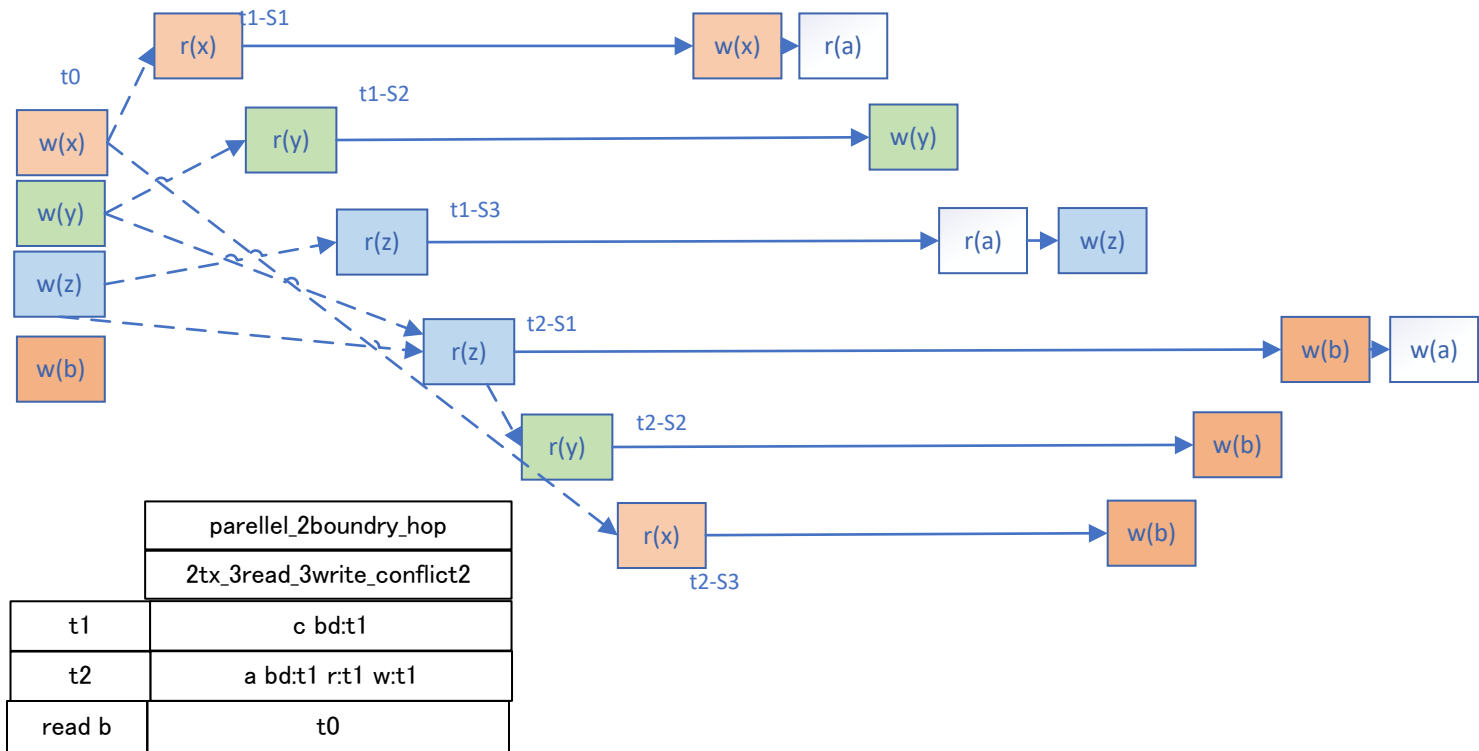


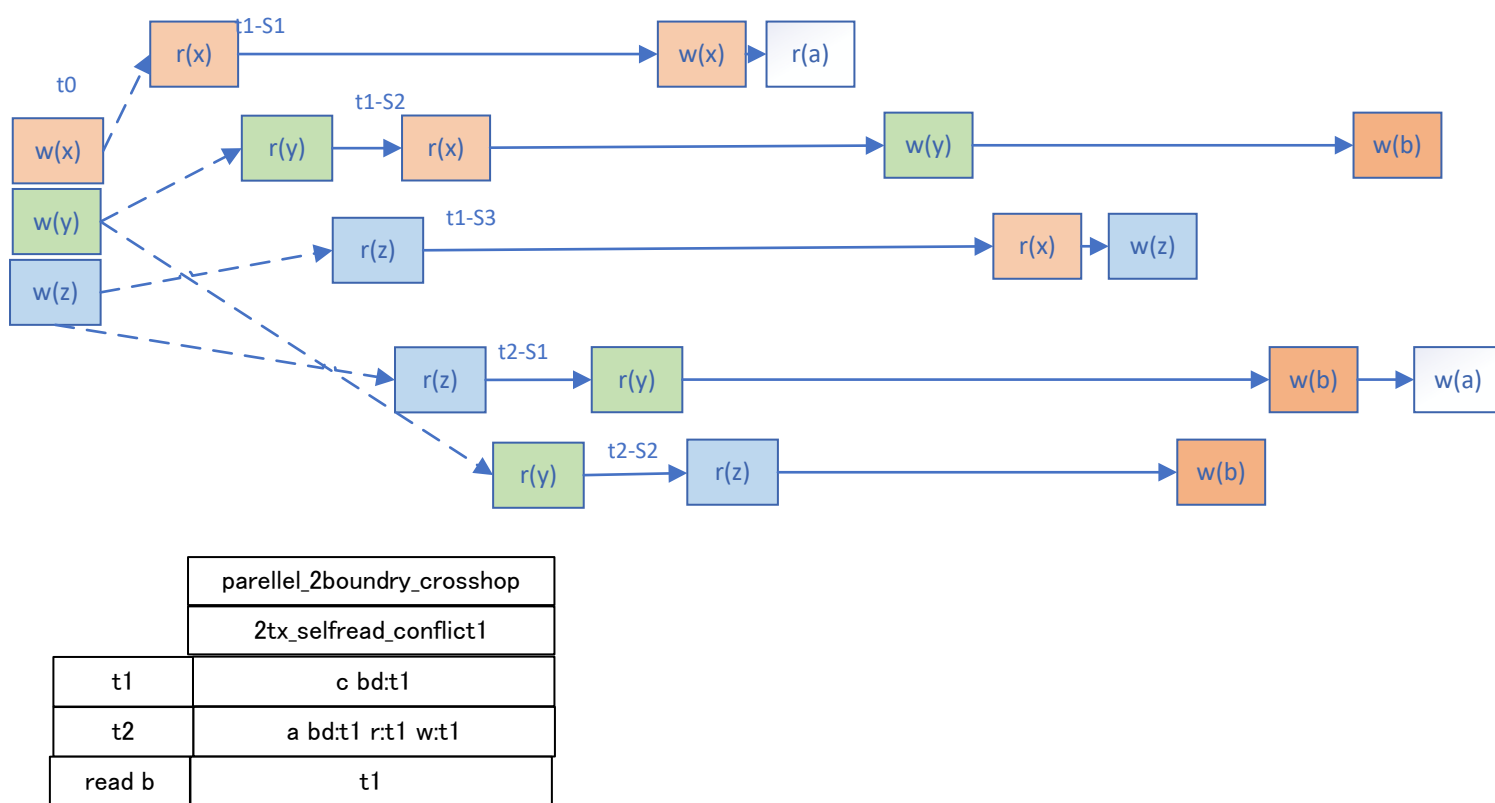
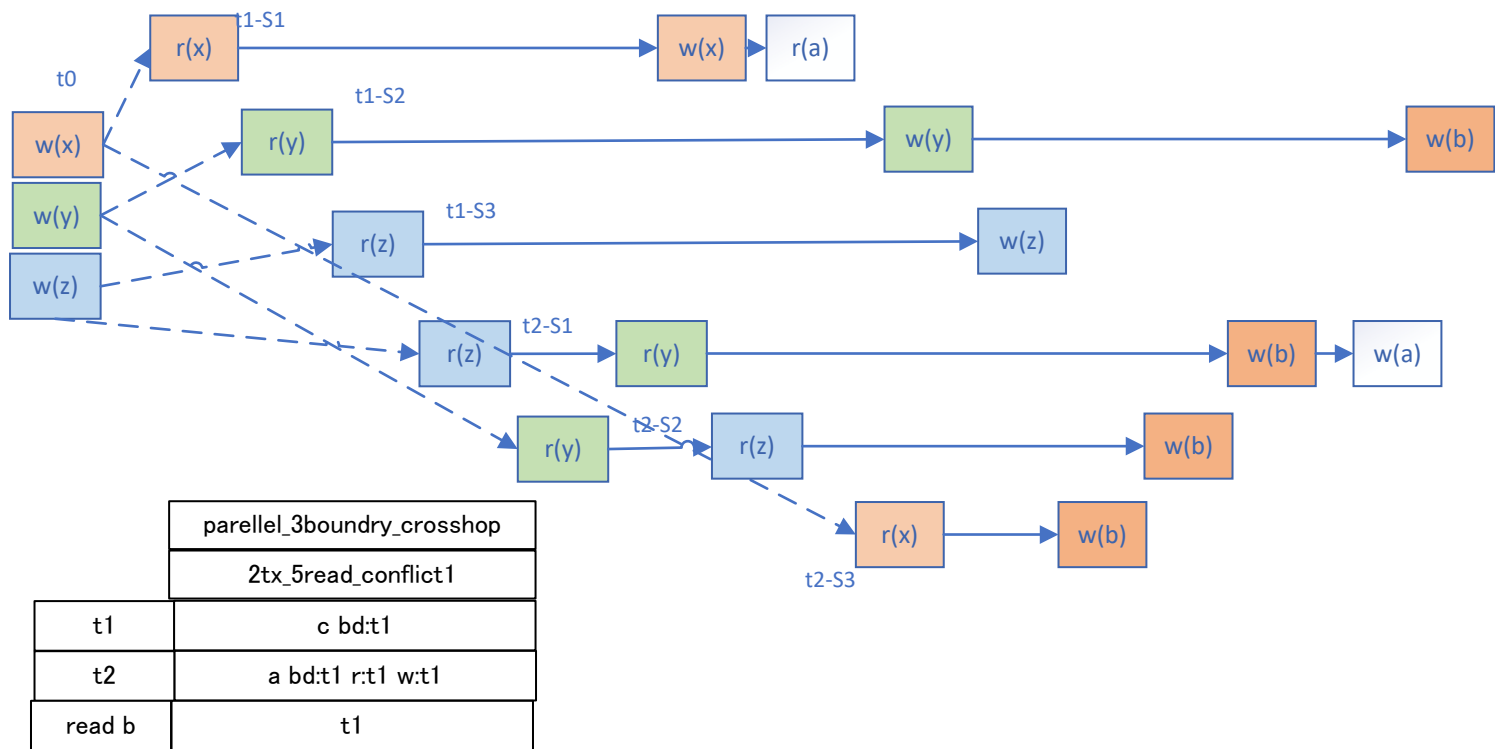
	parallel_1boundary_hop
	2tx_3read_conflict
t1	c bd:t1
t2	a bd:t1 r:t1 w:t1
read b	t0

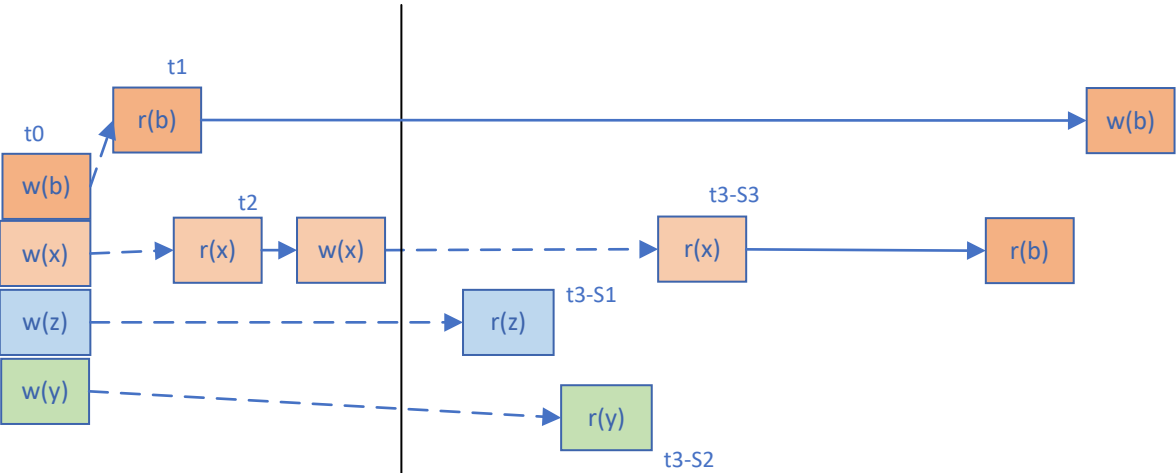


	parallel_1boundary_hop
	2tx_3read_conflict_delay
t1	c bd:t1
t2	a bd:t1 r:t1 w:t1
read b	t0

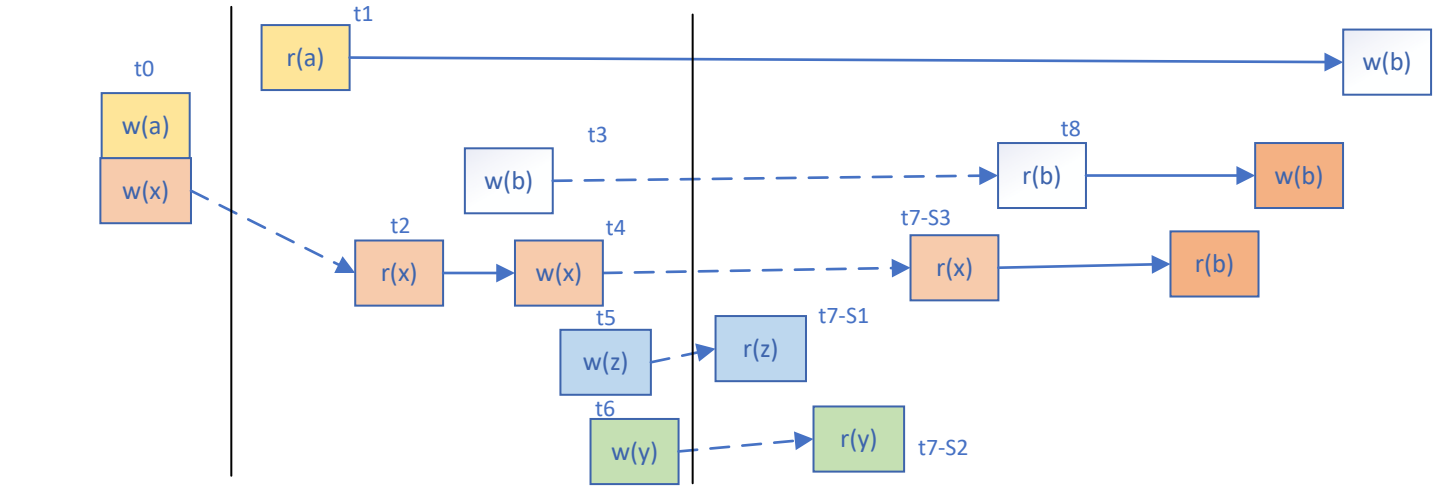








	parallel_read_crown
	2tx_3read_single_boundary
t3	a bd:t1 RUB:t2



	parallel_read_crown
	3tx_3read_boundary_hop
t7	a bd:t1 RUB:t6