- CPU fetches, decodes and executes instructions. May not do it on its own but directs hardware to execute it.
- Datapath consists of the ALU and registers which are connected to main memory.
- Control unit directs hardware.
- Registers hold data which can be accessed by the CPU.
- ALU carries out arithmetic operations. Control unit determines what to do next

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Buses

- CPU shares data with other components by data bus
- Data, control and address info.
- Data lines convey bits from one device to another.
- Control lines determine the direction of data flow.
- Address lines determine the location.

Clocks

- Every computer has at least one clock.
- Fixed number of clock cycles required to carry out an operation.
- Megahertz, GHz
- Clock cycle time is the reciprocal of clock freq.

How many instructions per program

$$\text{CPU Time} = \frac{\text{seconds}}{\text{program}} = \frac{\text{instructions}}{\text{program}} \times \frac{\text{avg. cycles}}{\text{instruction}} \times \frac{\text{seconds}}{\text{cycle}}$$

how many cycles per instruction

secs per cycle

Memory@AMI

• Locations similar to regathers, can be accessed by bytes, bits etc

By replacing the memorator, the quarter.

- Memory made of RAM chips..

. 4M * 16 Ram chips Series 4µg of Il-

b. it memory.

- Memory locations correspond to patrular addresses.

es. 4M can be expressed as 22×220 -

2" words.

- Memory locators are numbered ok 271

. Address lines count hour 0 to 222-1.

Low and High order interleaving

For small programs , High-order will be more efficient as you don't have to jump through disherent chips . whereas & bigger programs, will be more effort outs low as

you jamp less.

Marie Simulator

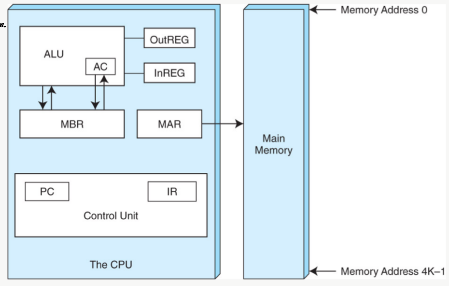
Machine
Architecture (which is)
Really
Intuitive (and)
Easy

Characteristics

1) 2's C binary data representation
2) Stored program, fixed word length
3) 4K words of word addressable main-memory
4) 16-bit data words
5) 16-bit instructions, 4 for the Opcode and 12 for the address

Registers

6) 16-bit accumulator (AC)
7) 16-bit instruction register (IR)
8) 16-bit memory buffer (MBR)
9) 12-bit program counter (PC)
10) 12-bit memory address register (MAR)
11) 8-bit input register (InREG)
12) 8-bit output register (OutREG)



6) Holds the operator which you will be using, holds the result of the most recent operation.

10) Holds the address of an instruction or the operand of an instruction.

8) temporary storage place.

9) Holds the address of the next program.

7) IR. Instruction which is currently being executed.

ISA - INSTRUCTION SET ARCHITECTURE

- ISA is the interface between the hardware and software of a computer.
- MARIE has 13 instructions
- Opcode - what instruction, what to do.

$$\text{CPU Time} = \frac{\text{seconds}}{\text{program}} = \frac{\text{instructions}}{\text{program}} \times \frac{\text{avg. cycles}}{\text{instruction}} \times \frac{\text{seconds}}{\text{cycle}}$$

Number of instructions per program

Number of cycles per instruction

secs per cycle.