

16-bit DFF Up Counter

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Group Name: **Up Counter**

Introduction

- This is a 16-bit up counter that counts from lowest 16-bit unsigned integer to highest 16-bit integer
- Our design is created using D flip flop and it is asynchronous.
- Our circuit is constructed in electric schematic and electric layout design using transistors.
- The structure and functionality of DFF as well as the complete counter will be explained.
- Schematic and Layout design will be verified through LTSPICE Simulation.
- Schematic and Layout design will be verified through IRSIM Simulation.
- Design analysis with delay measurement and chip details will be shown and the result will be discussed.

Background

- A 16-bit up counter is a sequential circuit that counts upward in binary from 0 to 65535 ($2^{16} - 1$).
- Utilizes 16 D flip-flops, each representing a bit in the 16-bit binary number.
- The counter increments by 1 on each clock pulse, cycling through binary values.
- We will be using rising edge triggered D flip flop which means the least significant bit will change at every rising edge of clock pulse
- All 16 D flip flops or DFF are cascaded together to make the counter work
- A rising edge triggered DFF is made from 4 NOT gates and 8 NAND gates, with a master D latch and slave D latch
- We will create an asynchronous design which means all DFF are not connected through a common clock.
- Asynchronous counters will take the inverted output from previous flip-flop as the clock of current flip flop. (Only 1st DFF gets fed with designer's choice of clock input).
- Reset Functionality: Once the counter reaches maximum value, it resets back to 0 to restart the count
- Application: Widely used in digital circuits for timing applications, frequency division, and as address counters in memory devices.

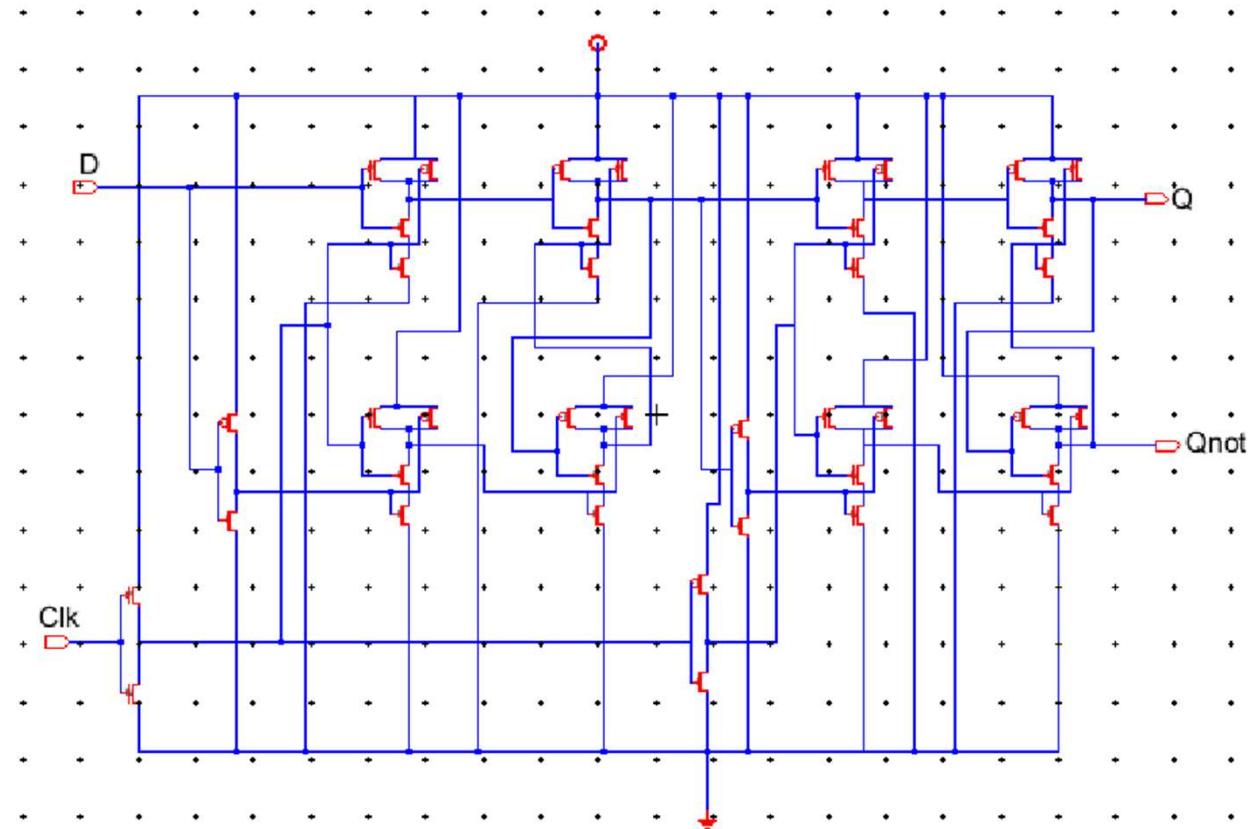
Introduction

- Truth Table:

Schematic

- D Flip Flop

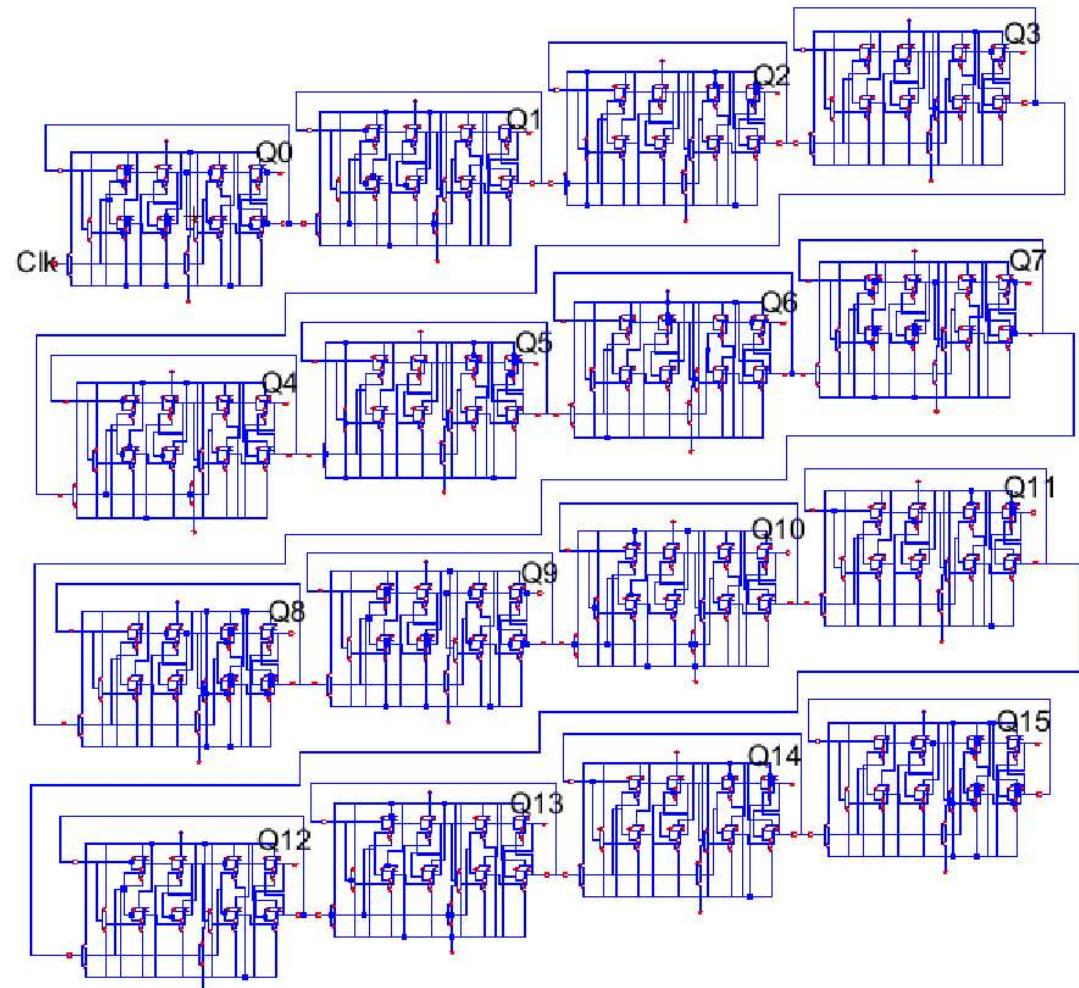
→ A DFF delays the output of a digital circuit until next clock pulse. This is a rising edge master slave design of D flip flop. The output changes to next state during the rising edge of the clock pulse. This master slave design is made of two D latches with each consisting of 4 NAND gates and an inverter. Two additional inverter are used to connect the two latches to create this design of D flip flop which functions on the rising edge of the clock. By delaying output, it allows us to implement the incrementation functionality which is the fundamental part of a counter.



Schematic

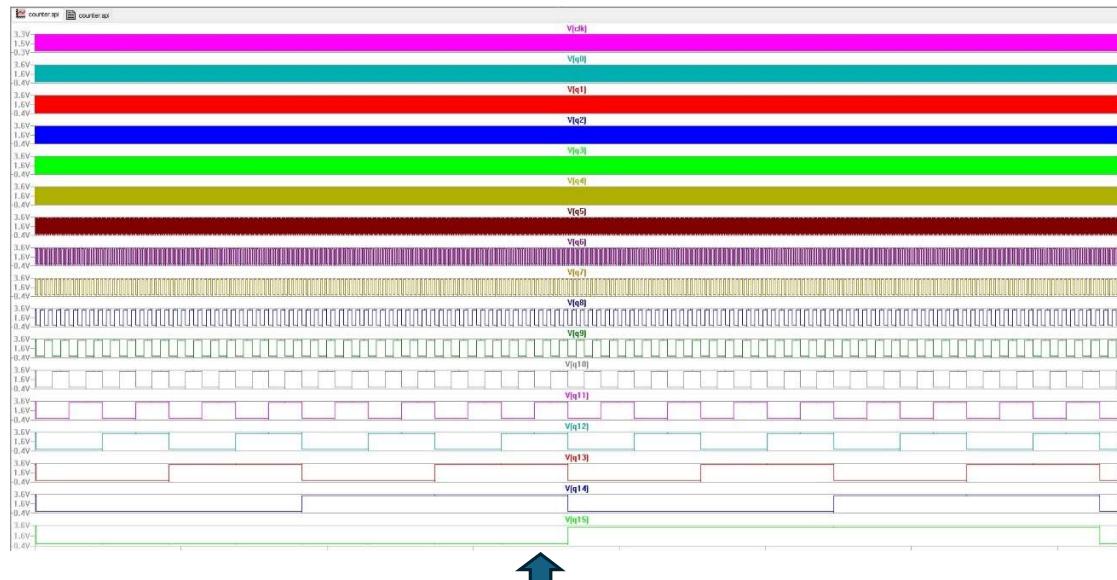
- 16-bit Up Counter:

→ This is the complete design of the 16-bit asynchronous up counter using D flip flop. The design is created by cascading 16 DFFs together. The 1st DFF gets a clock input of designer's choice. Each following DFF is then connected by feeding the Q' output of a DFF to the clock input of next DFF while the same Q' also connects back as D input of the same DFF. Due to using Q' of a previous DFF to be the clock input of current DFF, the clock input is different each time making it asynchronous which means the output of each DFF is independent of the other functioning based on its own clock pulse and D input. This counter counts from 0 to 65535 (highest 16-bit unsigned integer) by incrementing by 1 at each rising edge of clock. The design verification will be shown with simulations next.



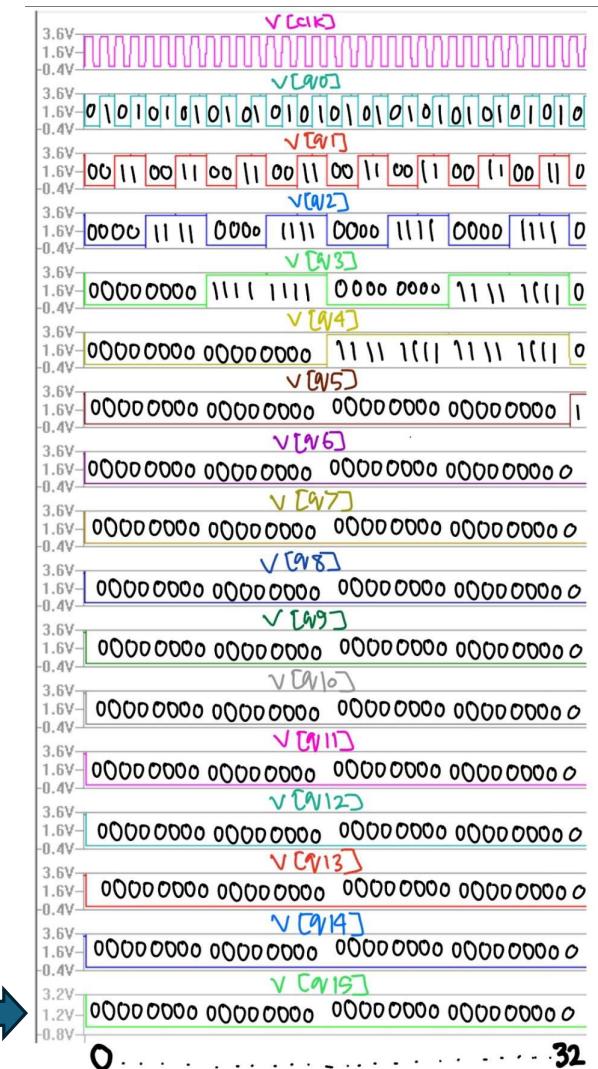
Schematic Simulations

- LT SPICE:



The LTSPICE simulation above shows the full functionality of the 16-bit asynchronous DFF up counter designed in electric schematic. As we can see, the counter starts with all Q bits at 0 starting the counter at 0000000000000000 (0_{10}) and keep incrementing by 1 at the rising edge of the clock cycle until it reaches 11111111111111 (65535_{10}) and then it resets back to 0 as 65535 is the maximum unsigned integer that can be held within 16bits. The detailed outputs according to clock pulses will be shown below.

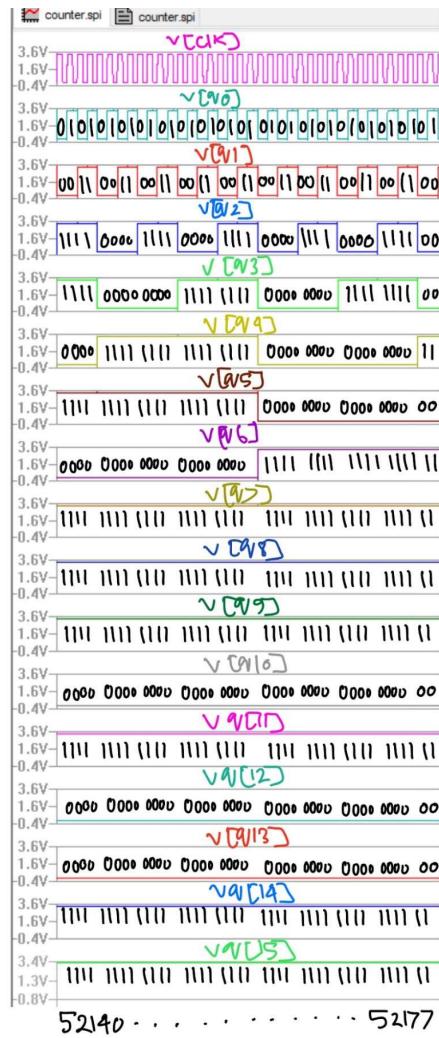
Here, we look at the early parts of the simulation where the simulation above shows how the outputs changes based on rising edge of clock pulses to count from 0 to 32 by incrementing by 1 each time.



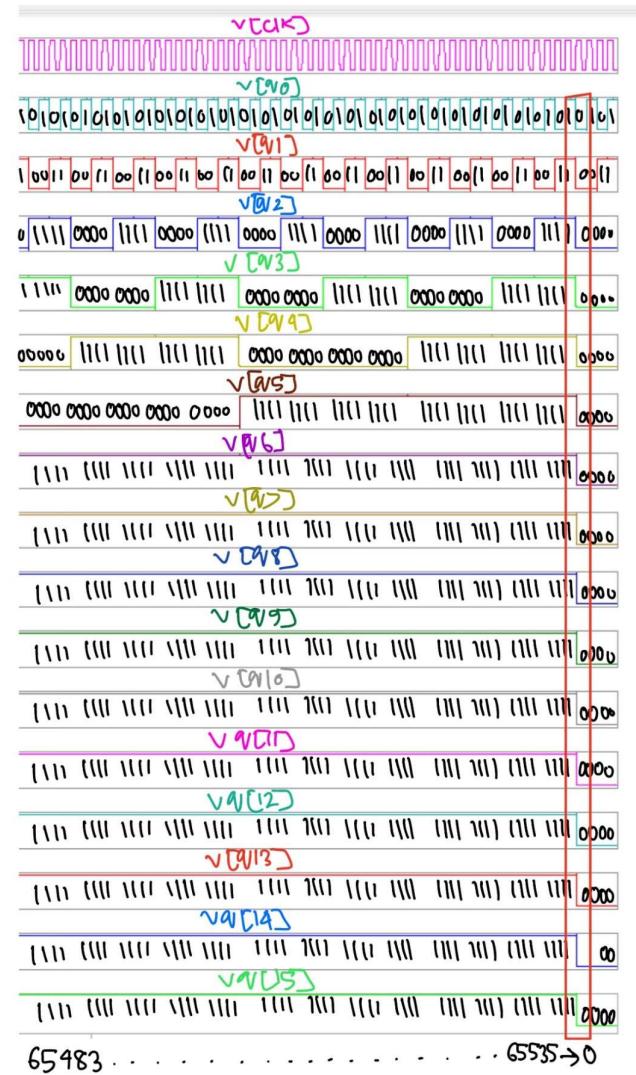
Schematic Simulations

- LT SPICE:

This picture above now shows the later part of the count as it continues into the thousands where we show the simulation proving our design still counts correctly from 52140 to 52177.

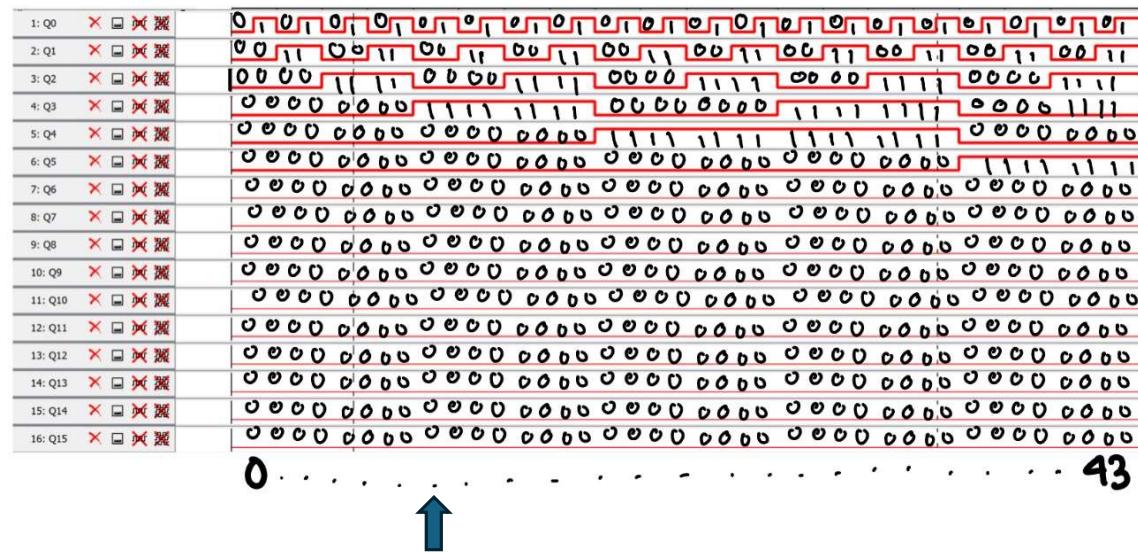


This segment of schematic simulation shows the moment the counter resets. Here we show the counting starting from 65483 until 65535 which is the maximum value that can be held in 16 bits and then the counter resets back to all zeroes to start the count again.

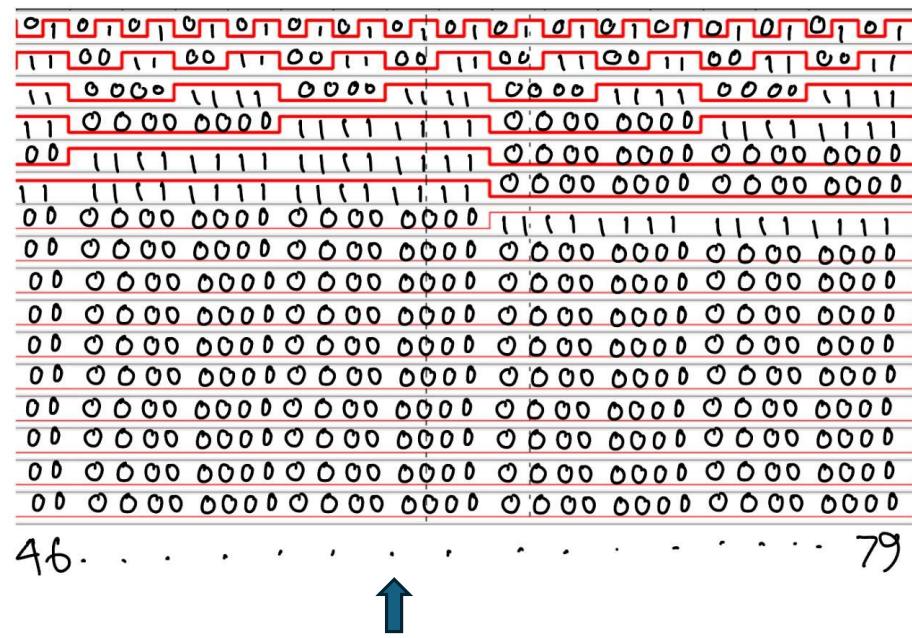


Schematic Simulations

- IRSIM:



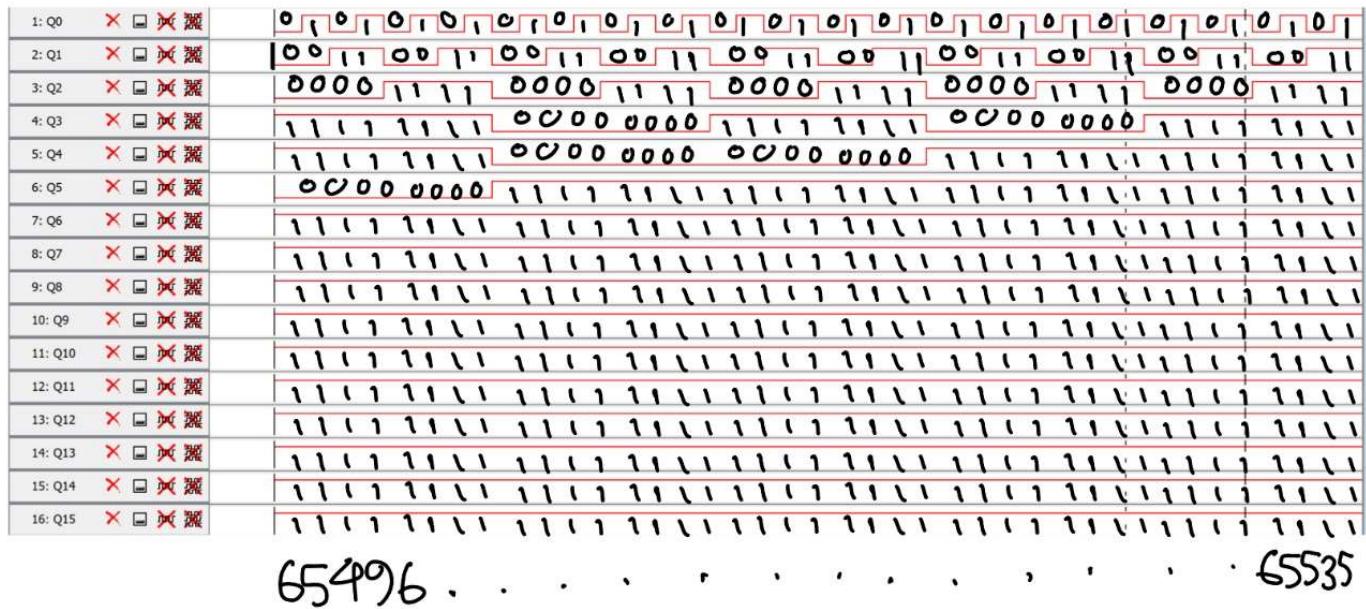
The picture above shows the simulation to verify our design in schematic using IRSIM. Here, we show that counter starts counting from all zeroes properly and we show the counting being performed correctly with 1-bit incrementing at each rising edge of the clock until counter reaches 43.



Here, we continue the counting to show our deign is still performing as it's supposed to by showing that our counter reached 46 by now and keeps counting (here we show it till 79).

Schematic Simulations

- IRSIM:

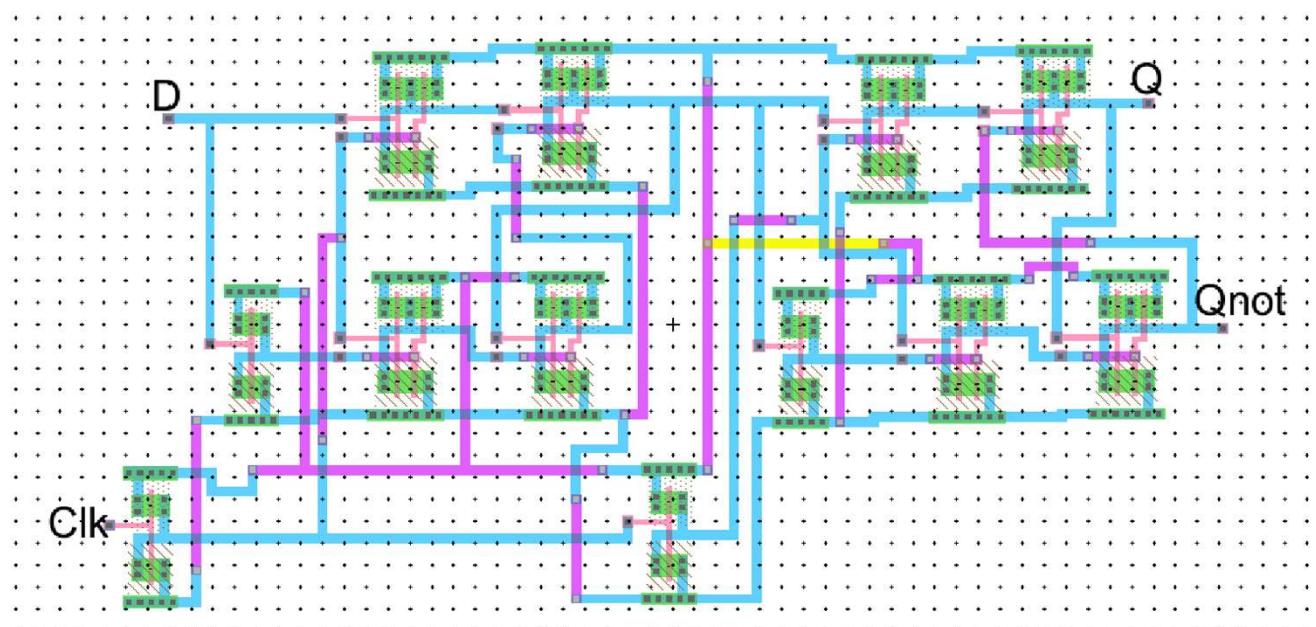


This part of the IRSIM simulation as the counter reaches towards the end where the counter continues counting to 65496 and towards 65535 which is the largest unsigned 16-bit integer.

Layout

- D Flip Flop

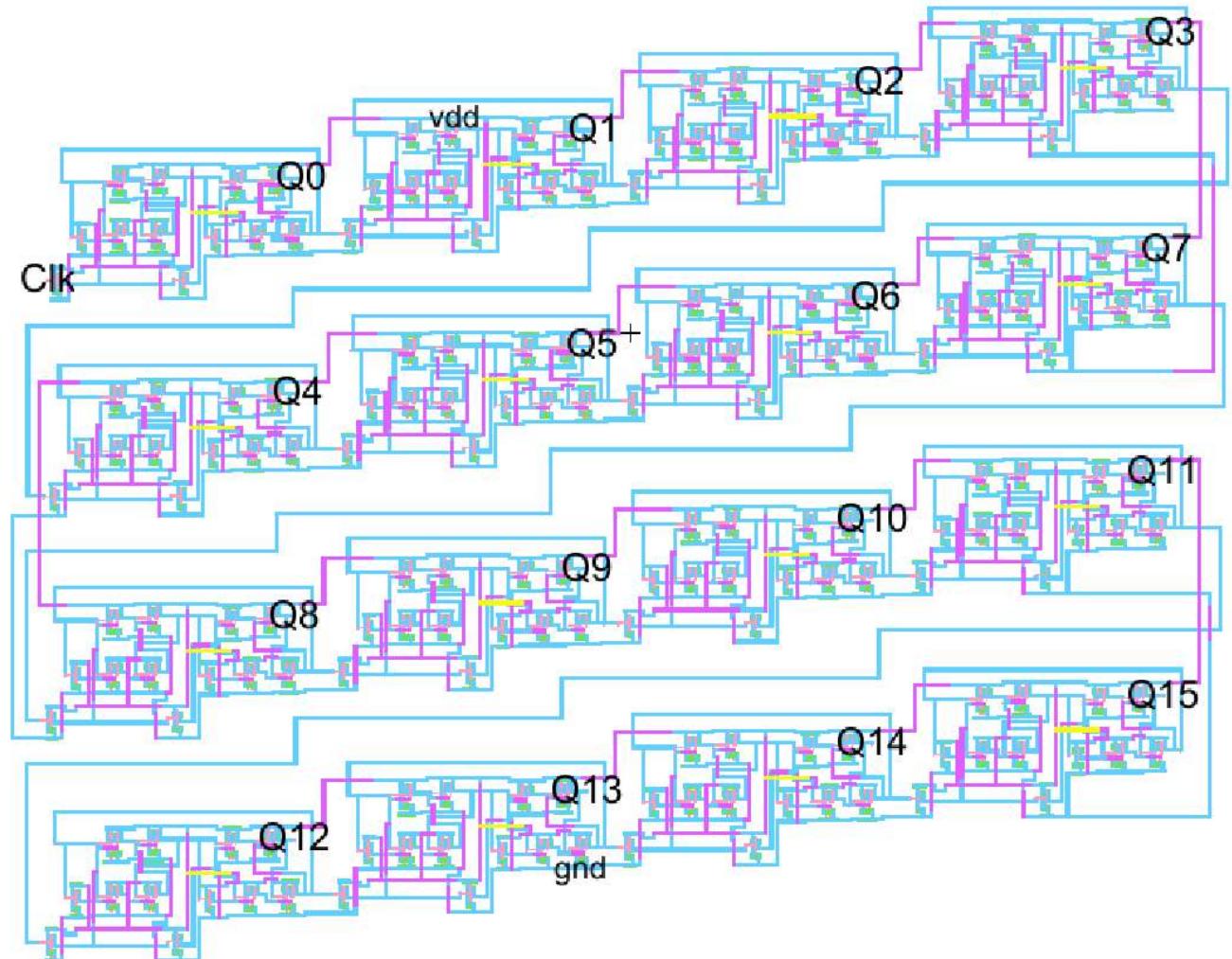
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Layout

- 16-bit Up Counter:

→ This is the complete design of the 16-bit asynchronous up counter using D flip flop. The design is created by cascading 16 DFFs together. The 1st DFF gets a clock input of designer's choice. Each following DFF is then connected by feeding the Q' output of a DFF to the clock input of next DFF while the same Q' also connects back as D input of the same DFF. Due to using Q' of a previous DFF to be the clock input of current DFF, the clock input is different each time making it asynchronous which means the output of each DFF is independent of the other functioning based on its own clock pulse and D input. This counter counts from 0 to 65535 (highest 16-bit unsigned integer) by incrementing by 1 at each rising edge of clock. The design verification will be shown with simulations next.



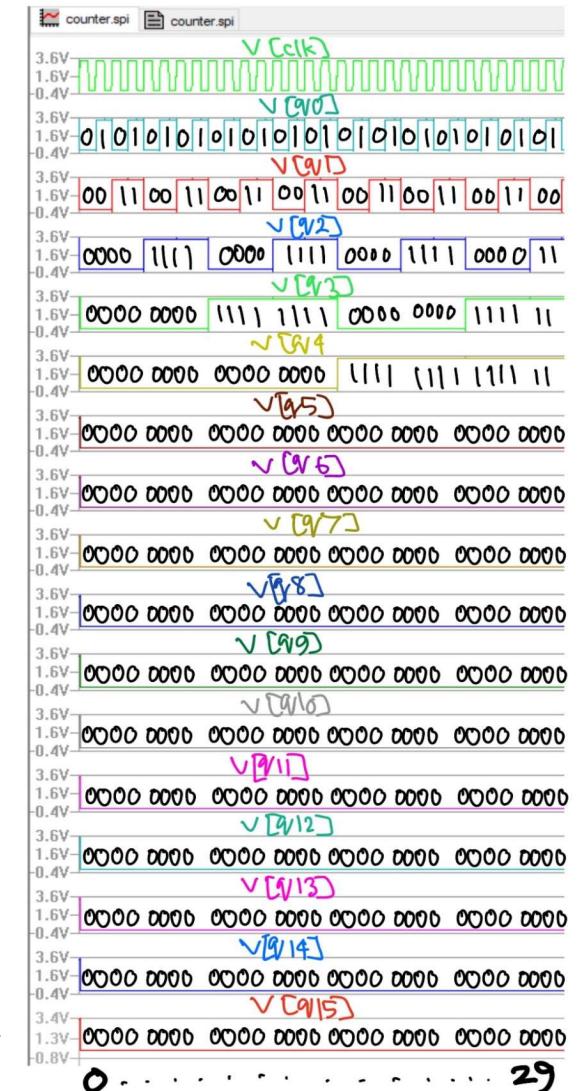
Layout Simulations

- LT SPICE:



The picture above shows the full simulation in LTSPICE of our layout design of the 16-bit asynchronous DFF up counter. The counting starts at 0000000000000000 (0_{10}) and keeps counting until 1111111111111111 (65535_{10}). Once it reaches the largest 16-bit unsigned integer, the counter resets back to all zeroes to restart the count. The detailed segments from different parts of the counting process will be shown below.

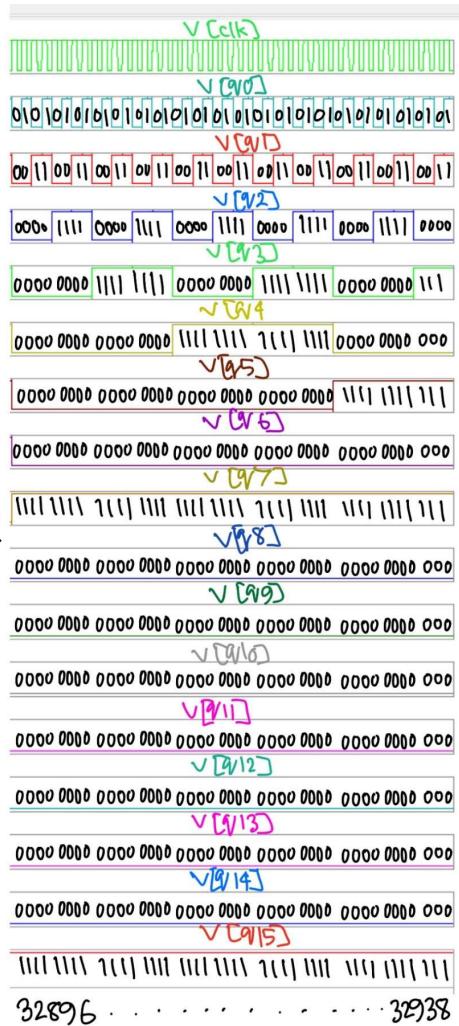
This demonstrates that our layout design of the counter starting count from all zeroes. We see that the counter keeps counting till 29.



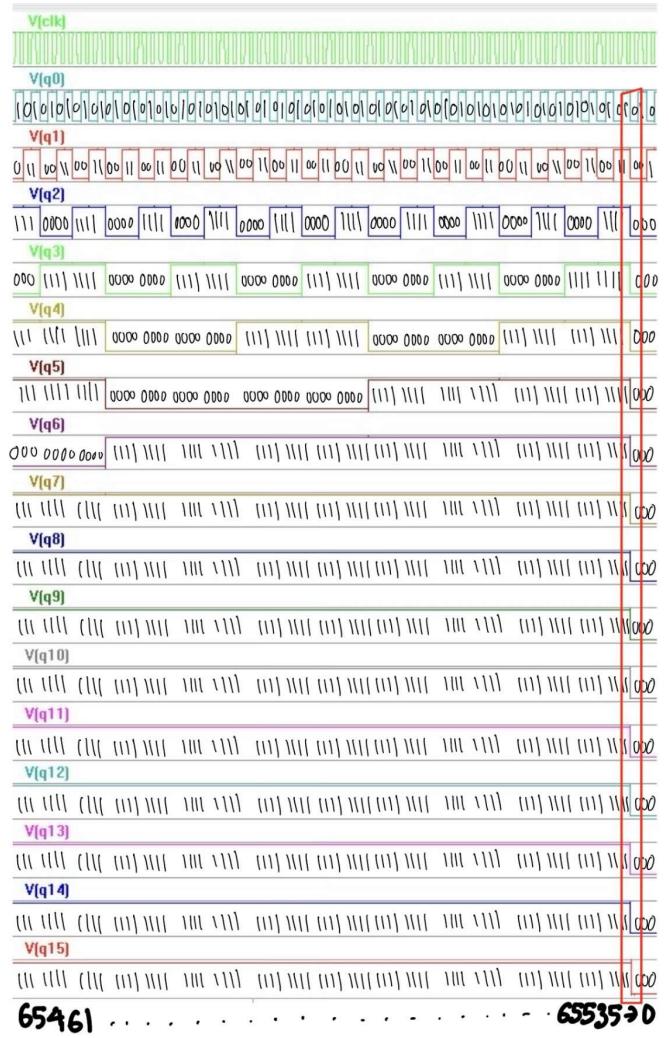
Layout Simulations

- LTSPICE:

Here we show the segment of simulation where our counter already counted halfway through. The simulation segment above shows that our counter is still performing as intended where we show the count from 32896 till 32938.

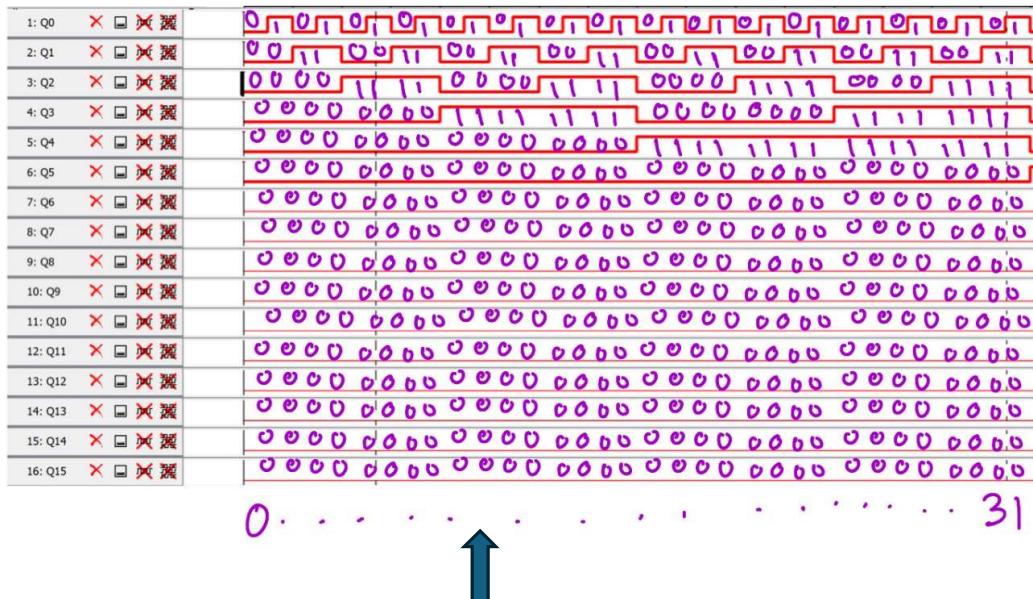


This is the end part of the simulation where it shows our layout counter continues counting to 65461 and goes beyond till 65535 which is the maximum integer in 16 bits and then counter restarts counting from 0.

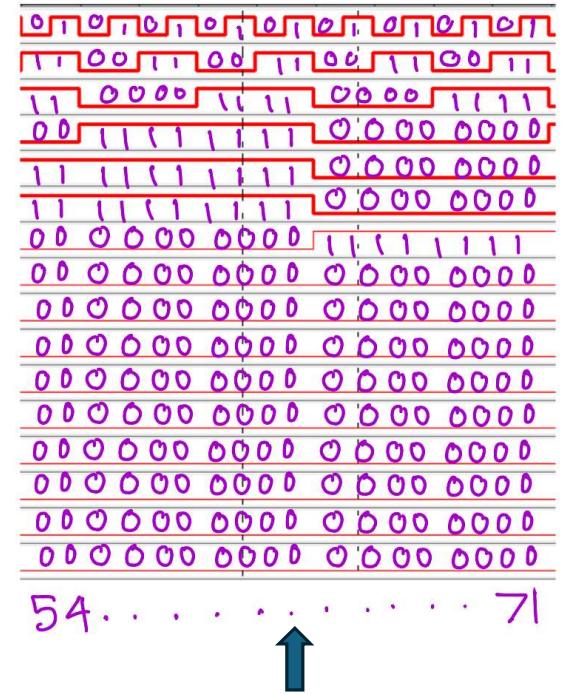


Layout Simulations:

- IRSIM:



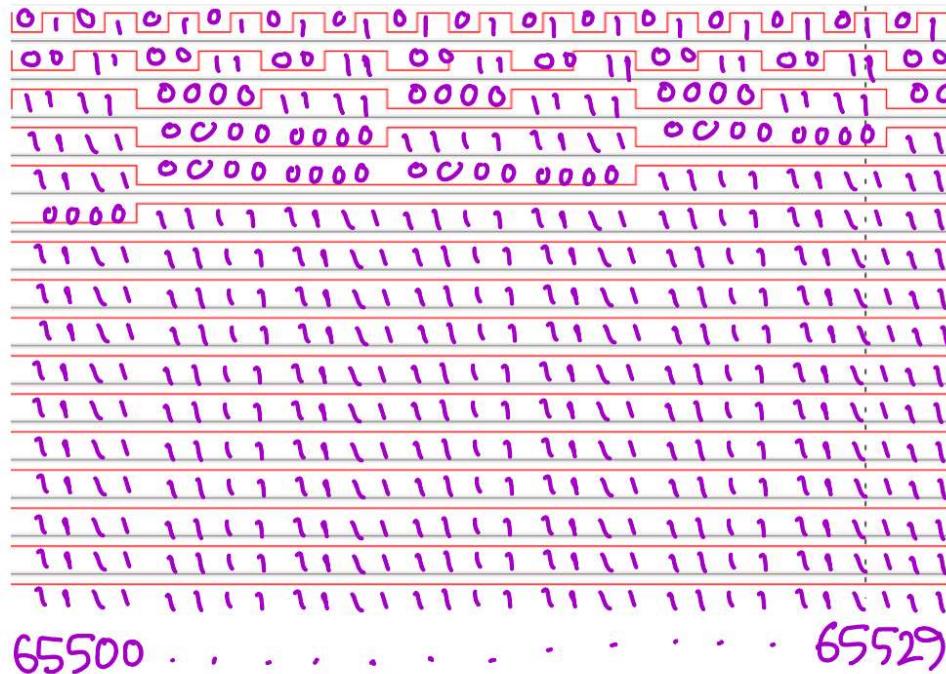
This IRSIM simulation shows the functionality of the layout counter. We started the count from all zeroes and in this segment of the simulation, the counting goes till 31.



Here we show the continuation of the counter to demonstrate the counter we have built in layout is still functioning as it keeps counting from 54 till 71 and continues.

Layout Simulations

- IRSIM



This shows the ending segment of layout up counter where we show the counting from 65500 to 65529. This is very close to the largest integer that is possible to store in 16 bits which is 65535 proving our counter works all the way through.

Results & Analysis

- As you can see from our simulations the counter works great with a relatively low clock frequency.
- Although the clock frequency is low it still takes the counter a long time to get 1 full cycle of Q15 as 65535 is a large number to make regardless of how fast the clock frequency is.
- A faster clock frequency causes distortion in the waveforms in the first couple of bits, so it was hard to reduce that amount of time to create 16 bits max output.

Results & Analysis

- Delay Measurements

	Rise Time	Fall Time	TPHL	TPLH	Propagation Delay(TP)
CMOS Schematic	15.585 ns	9.834 ns	5712.131 ns	2746.341 ns	4229.236 ns
CMOS Layout	23.369 ns	10.324 ns	6003.120 ns	3316.819 ns	4659.970 ns

- Chip Measurements

	Transistor size (W x L)	Transistor Count	Chip Area
CMOS Schematic	PMOS (10 x 2) NMOS (10 x 2)	(40*16) = 640	31636.307 μm^2
CMOS Layout	PMOS (10 x 2) NMOS (10 x 2)	(40*16) = 640	141852.063 μm^2

Conclusion

In this Project:

- We were able to successfully identify the functionality and structure of a D flip flop as well as the 16-bit up counter
- We were able to successfully build D flip flop in schematic and layout
- We were able to successfully cascade 16 DFF together to build the entire circuit of 16-bit asynchronous up counter in both electric schematic and layout
- We have successfully run simulation of our designs in LTSPICE and IRSIM to verify our counter sets, resets and counts with incrementation of 1 at each time as intended.
- We have provided further analysis on our design by calculating rise and fall time
- We have measured chip areas and chip measurements
- We have successfully summarized the result of our design and analyze its functionalities.

References

- Teja, R. (2024b, March 22). Asynchronous counter. ElectronicsHub USA.
<https://www.electronicshub.org/asynchronous-counter/>
- Urias, O. M. (2023, February 21). The D flip-flop (QuickStart tutorial). Build Electronic Circuits.
<https://www.build-electronic-circuits.com/d-flip-flop/>
- Technology, E. (2018, May 6). Digital Asynchronous Counter (Ripple counter) – types, working & application. ELECTRICAL TECHNOLOGY.
https://www.electricaltechnology.org/2018/05/digital-asynchronous-counter-ripple-counter-types.html#google_vignette
- Teja, R. (2024b, March 22). Asynchronous counter. ElectronicsHub USA.
<https://www.electronicshub.org/asynchronous-counter/#:~:text=Asynchronous%20counters%20can%20be%20easily,also%20used%20as%20Truncated%20counters.>