DESIGN AND SIMULATION OF INTELLECTUAL PROPERTIES PROTECTION USING MIXED MODUL LEVEL AND SIGNAL OBFUSCATION

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**Abstract**

System on a Chip (SoC) is an embedded system module that has functionality in a silicon chip board that can also be called Very Large Scale Integration (VLSI). The owner of the SoC design owns the copyright on the design of the system that has been created. Fabless manufacturing is a way of printing hardware modules that Integrated Circuit (IC) designers are outsourching from outside the printing factory. Fabless manufacturing from IC design has gap design theft When the design will be printed or when the project requires multiple module With various functions from various designers. Therefore every module is VLSI Of this chip designer requires proof of ownership of the designer or Production companies. In this study plans to make the verification of ownership design with 2 specific key verification that is Polygate as the main key that will activate the second key, and the second key will be active which process using digital filter algorithm.

Keywords: *VLSI, Intellectual Property Protection, Digital Signal Processing, Polygate Watermark.*

1. **Introduction**

Providing a series of watermarks as a safeguard to a printed VLSI blueprint that indicates ownership of the designer or module manufacturer will protect against cheating others who will steal the design. So the possibility of theft or plagiarism that causes losses to the company or designer because of its design is stolen or plagiarism reduced.

Broadly speaking the technique of Intellectual Property Protection (IPP) watermarking can be classified into 2 classes namely Dynamic Watermarking and Static Watermarking. Dynamic Watermarking is a watermark that can not be detected except by running a watermarked IP to detect the resulting signal, such as digital signal processing (DSP), or finite state mechine (FSM) watermarking. Static Watermarking is a watermark that refers to the properties of a design, and can only be detected in different static ways, such as paths and watermarking placements.\cite{chapman} One of the other safeguards is to convert the simulated file from a file. The RTL source code that enables is not easy to be reverse-engineered by third parties, so the model can not be changed and reused with other purposes by third parties and irresponsible users. However, this way only protects from the softwere side that protects the IP from being misused by third party users.\cite{water} For IP security used in project sharing and reusable projects can be used with the security of Digital Signal Processing cell that allows integration in the system.

In this research will perform a combination of polymorph gate IP protection with digital filter algorithm. Using a combination of these two techniques will provide additional security to IP protection that is likely to over write a smaller watermark. Therefore in this study proposed a combination of existing methods to improve security capabilities in an existing VLSI module. Combine polygate as a combination key to enable the digital filter module to be used as a watermark.

1. **LSI Development Flow**

Transistor is the most important component in the development of modern computer technology. Be-fore the invention of the transistor. The Engineer must use a vacuum tube. Vacuum tubes can work as an electronic switch. However, vacuum tubes require power and large space, expensive, and slow execution capabilities make vacuum tubes replaced by transistors.

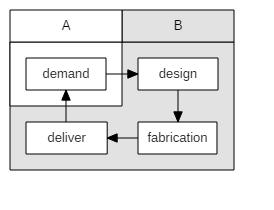
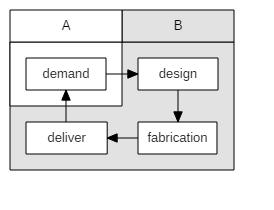
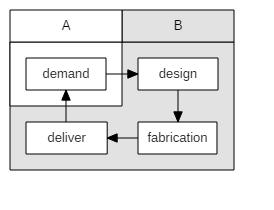
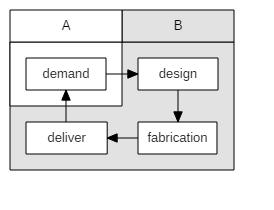
With the discovery of transistors whose size and power requirements are small but still effec-tive, Electronic Engineers in the 1950s saw many possibilities for their implementation in more ad-vanced electronic circuits. With the increasing complexity in electronic circuits new problems arise.

One of them is the size of the circuit. A com-plex circuit like a computer depends heavily on speed. If the number of components on the com-puter is too much then the connection between the components is also more and more long, causing the transfer of electrical signal speed becomes re-duced which causes the process on the computer to be slow.

In 1958 this problem could be solved by the idea of Jack S Kilby whose idea was to assemble electronic components in a silicon block (Mono-lithic Idea). The idea not only reduces the size of the circuit but also reduces the need for cable connections between circuits and their manufac-turing can be automated. But the idea still has many other problems. Nevertheless, the idea was awarded a nobel prize in 2000.

Half a year after Kilby sparked his idea of the Monolithic series. Robert Noyce has the answer to some problems on Kilby’s idea. Namely intercon-nection between circuits. It adds a metal layer to the last layer and removes some layers so that the connection between components can be formed.

Possibility type of attack is changing over time. It is caused based of how bussiness flow in VLSI Design are olso changed. In the early day of VLSI development, a system from designing a module until design is delivered to custommer is done by solo manufacturrer industries.



*Figure 1: Old Bussiness*

##### **Sections and Subsections**

Sections and subsections should be numbered and titled as 1.0, 2.0, etc.  and 1.1, 1.2, 2.1, 2.2, 2.2.1, etc. Capital letters should be used for the section titles. For subsections, the first letter of each word should be in capital letter and followed by small letters. One line space should be given above the sub section while no space should be given below the heading and text

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Subsub section has to be in sentense case with no spacing above or blow the srat of it.

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# *Table 1: Center Table Captions Above The Tables.*

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| --- | --- |
| Relevancy (%) | Score (%) |
| 88.5 | 87.3 |
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*Figure 1: Description Is Placed Right Below The Figure*

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Netj = w0 + xiwij (1)

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[1] Author No.1, Author No 2 Onward, “Paper Title Here”, *Proceedings of xxx Conference or Journal (ABCD)*, Institution name (Country), February 21-23, year, pp. 626-632.

[2] B.N. Singh, Bhim Singh, Ambrish Chandra, and Kamal Al-Haddad, “Digital Implementation of an Advanced Static VAR Compensator for Voltage Profile Improvement, Power Factor Correction and Balancing of Unbalanced Reactive Loads”, *Electric Power Energy Research*, Vol. 54, No. 2, 2000, pp. 101-111**.**

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