CSE 206 (Digital Logic Design Sessional)

Experiment No.: 07

Name of the Experiment:

Flip-Flops and Registers

Group No.:	06
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Problem 1.

Problem specification:

Design and implement a master-slave JK flip-flop using only NAND gates.

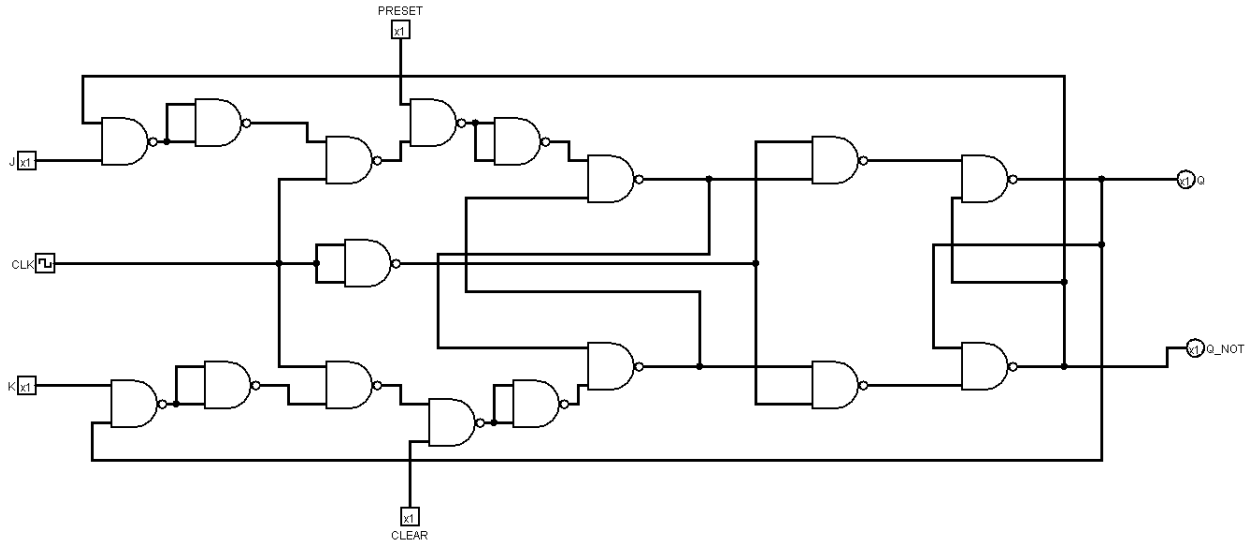
Excitation Table:

PRESET	CLEAR	J	K	CLK	Q_{n+1}	Mode
0	0	X	X	X	Not allowed	Not allowed
0	1	X	X	X	1	Set
1	0	X	X	X	0	clear
1	1	X	X	0	Q_n	Hold
1	1	0	0	1	Q_n	Hold
1	1	0	1	1	0	Reset
1	1	1	0	1	1	Set
1	1	1	1	1	$(Q_n)'$	Toggle

Required instruments:

No	**Name**	**Model**	**Quantity**
01	Logisim Software		
02	IC(Quad 2-Input NAND Gate)	7400	5
05	Wires		
06	Input Pins		2
07	Output Pins		2

Circuit diagram:



Observations:

1) Since Q and Q' had no preset values at first, the connection was not duly established. Therefore, to solve this problem we have used Preset and Clear to give an initial value in the circuit.
2) The Master-slave paradigm solves the race around problem of a single J-K flip-flop.
3) We tried to make the circuit such a way that it was not too dense with wires.
4) We have used the documentations of the ICs to make sure the connections were given through the right pins.
5) We checked the output according to the excitation table.

Problem No.2:

Problem Specification:

Design and implement a 4-bit universal shift register.

Required Instruments:

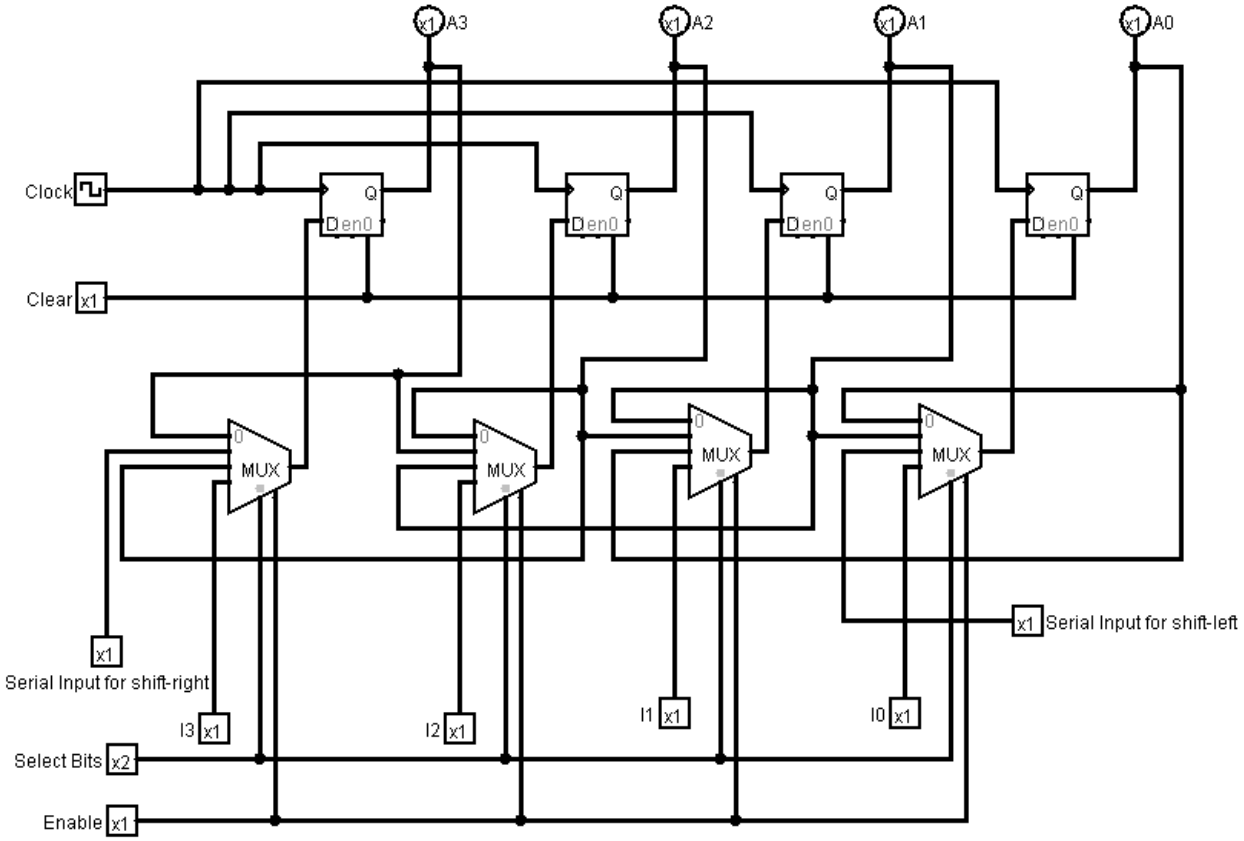
No	Name	Model	Quantity
01	Logisim Software		
03	IC (Dual 4:1 MUX)	74153	2

04	IC (D-Flip flop)	7474	2
05	Wires		
06	Input Pins		8
07	Output Pins		4

Excitation Table:

Input					Output				
Clear	Clock	S_1	S_0	Internal Signal, D_i(i = 0, 1, 2, 3)	A_3	A_2	A_1	A_0	Mode
0	X	X	X	X	0	0	0	0	Asynchronous
1	X	0	0	X	A_3	A_2	A_1	A_0	Data Hold
1	⬆	0	1	A_{i-1}	I_0	A_3	A_2	A_1	Shift Right
1	⬆	1	0	A_{i+1}	A_2	A_1	A_0	I_2	Shift Left
1	⬆	1	1	A_i	I_3	I_2	I_1	I_0	Parallel Load

Circuit Diagram:



Observations:

1) We tried to make the circuit such a way that it was not too dense with wires. The combinational part of the circuit could alternately be built with a set of AND gates. We have avoided that method due the increased complexity in the circuit.
2) We have used the documentations of the ICs to make sure the connections were given through the right pins.
3) We checked the output according to the excitation table.