## OBJECTIVES

- Understand how a BJT, a JFET, or a MOSFET can amplify a signal.
- Visualize why a transistor can clip or limit a signal.
- Differentiate between the common-emitter, common-base, and common-collector configurations in BJT amplifiers.
- Differentiate between the common-source, common-gate, and common-drain configurations in field-effect transistor amplifiers.
- Understand the difference between capacitively-coupled stages and direct-coupled stages.
- Recognize the hybrid-π model for a common-emitter amplifier.
- Perform analysis of BJT amplifiers using *h*-parameters.
- Develop an understanding of amplification based on field-effect transistors.

## 7–1 INTRODUCTION

In Chapters 4 and 5 we learned about the characteristics of bipolar and field-effect transistors and their behavior in dc circuits. We discussed their regions of operation (cutoff, active, saturation) and how to bias them in order to establish a desired quiescent condition.

In Chapter 6 we covered amplifier fundamentals in the general sense, that is, without regard to what device or devices are used for the amplification function.

In this chapter we will look at amplifiers based on transistors of both bipolar and field-effect types in discrete form. We will make extensive use of the models we learned in Chapter 6 and will expand more on concepts and characteristics that are specific for the particular device and configuration being considered.

At this point it is important that the reader understands that in modern electronics, amplification of low-level signals is seldom done with discrete components. That approach was the only choice several decades ago. Nevertheless, it is important to understand the behavior of discrete transistors in amplification as foundation material for more advanced topics in integrated-circuit amplification as well as in power amplifiers.

Bipolar junction transistors can be used in three distinct amplifying configurations: common emitter (CE), common base (CB), and common collector (CC). Similarly, field-effect transistor amplifiers, whether junction type or MOSFET, can be configured as common source (CS), common gate (CG), and common drain (CD). Each configuration must be properly biased in the center of its active region and capacitively coupled to the input signal source and to the load resistance.



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## The Purpose of Bias

In most single-transistor amplifiers, the output voltage must always be positive or must always be negative. When that is the case, it is not possible for the output to be a pure ac waveform. By definition, an ac waveform is alternately positive and negative. The purpose of bias in a transistor amplifier is to set a dc output level somewhere in the middle of the total range of possible output voltages so that an ac waveform can be superimposed on it. Figure 7–1 illustrates the point. The ac input causes the output voltage to vary above and below the bias voltage, but the instantaneous values of the output are always positive (in this example). In other words, the output is of the form

$$v_o(t) = V_B + A \sin \omega t$$

where $V_B$ is the bias voltage, or dc component, of the output, and $A$ is the peak value of the sinusoidal, ac component.

It is apparent that the values of $V_B$ and $A$ must be such that $V_B + A$ is not greater than the maximum possible output voltage and $V_B - A$ is not less than the minimum possible output voltage. If these conditions are not satisfied, then the output voltage will reach its minimum or maximum extremes before the total ac variation can take place. The result is a flattening of the output waveform called *clipping*. Figure 7–2 illustrates positive and negative clipping caused by values of $V_B$ that are too large or too small and by values of $A$ that are too large. When clipping is caused by the amplitude $A$ being too large, as shown in Figure 7–2(c), the amplifier is said to be *overdriven*.

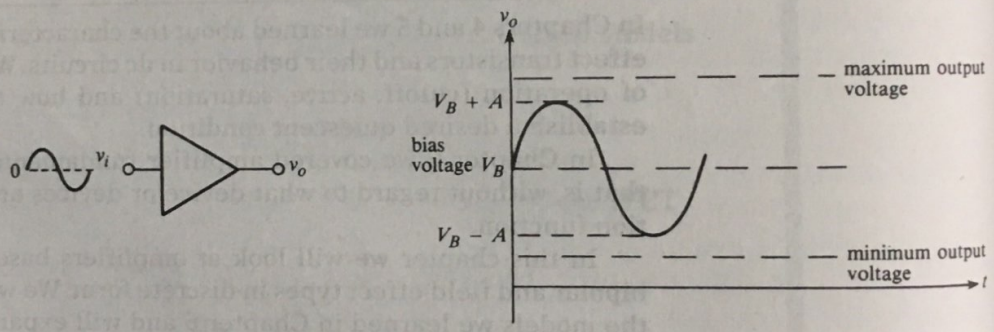
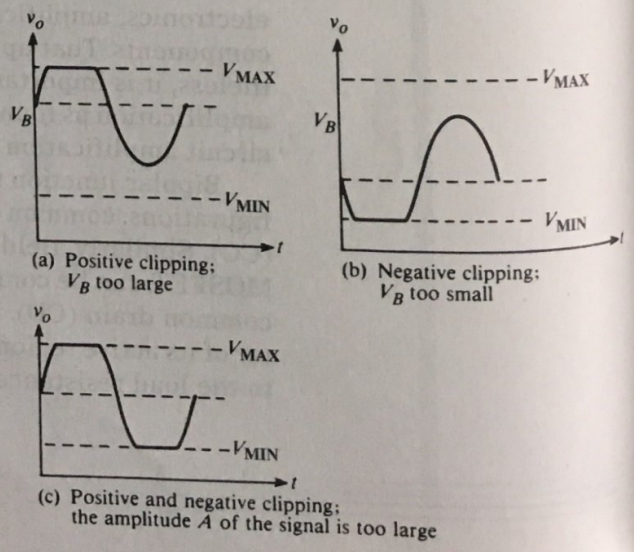



**FIGURE 7–1** The purpose of bias is to provide a dc level about which ac variations can occur

**FIGURE 7–2** Clipping caused by improper setting of the bias voltage and by overdriving

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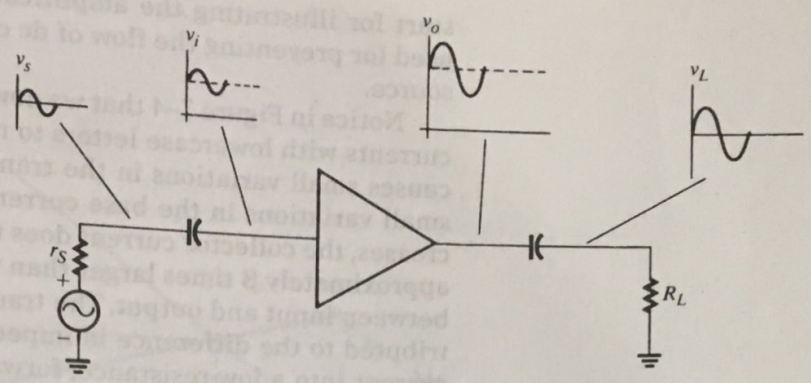


FIGURE 7–3 Coupling capacitors are used to block the flow of dc current between the amplifier and the signal source and between the amplifier and load

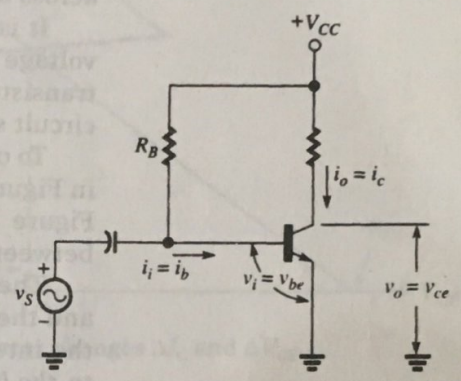


FIGURE 7–4 A common-emitter amplifier

The purpose of an ac amplifier is to produce an output waveform that is an amplified version of the input waveform. Because clipping defeats this purpose, it is said to *distort* the signal, and clipping is an example of amplitude *distortion*. In a transistor amplifier, the minimum and maximum output voltages are typically the voltages at saturation and cutoff, respectively. Thus, the minimum output may be a saturation voltage of a few tenths of a volt, and the maximum output may be a cutoff voltage equal to the supply voltage.

## Coupling Capacitors

In many amplifier applications, the source or the load, or both, cannot be subjected to a dc voltage or be permitted to conduct dc current. For example, an electromagnetic speaker is designed to respond to ac fluctuations only and may not operate properly if it conducts a dc current. To prevent the dc component of an amplifier's output voltage from producing dc current in the load, a capacitor is connected in series with the load. Similarly, to prevent the flow of dc current from the amplifier into the signal source (or vice versa), a capacitor is connected in series with the source. These connections are shown in Figure 7–3. The capacitors are called *coupling* capacitors, or *blocking* capacitors, because they block the flow of dc current. The capacitors must be large enough to present negligible impedance to the ac signals.

## 7–2 ANALYSIS OF THE CE AMPLIFIER

Our study of transistor amplifiers begins with an analysis of the common-emitter circuit because that is the most widely used configuration. Figure 7–4 shows the CE bias circuit we studied in Chapter 4 modified by the inclusion of an ac signal source in series with a capacitor connected to the base. As we will see later, this simple configuration has several drawbacks, but it is a good

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start for illustrating the amplification principle. The coupling capacitor is used for preventing the flow of dc current from the transistor into the signal source.

Notice in Figure 7–4 that we now designate input and output voltages and currents with lowercase letters to represent ac quantities. The signal source causes small variations in the transistor input voltage, which in turn cause small variations in the base current. As the base current decreases and increases, the collector current does the same. Because the collector current is approximately β times larger than the base current, we achieve current gain between input and output. The transistor's ability to produce gain can be attributed to the difference in impedance levels at input and output: A small current into a low-resistance, forward-biased junction controls current flow across a high-resistance, reverse-biased junction.

It is instructive to view ac operation in terms of the variation in output voltage and output current that occurs along a load line plotted on a set of transistor output characteristics. We will perform a graphical analysis of the circuit shown in Figure 7–4.

To observe the total variation in base current caused by the signal source in Figure 7–4, we use the input characteristic shown in Figure 7–5. We see in Figure 7–5 that the input voltage variation causes $I_B$ to vary sinusoidally between a minimum and a maximum value producing $\Delta I_B$ as indicated.

The load line for the circuit in Figure 7–4 intersects the $V_{CE}$-axis at $V_{CC}$ and the $I_C$-axis at $V_{CC}/R_C$. It is shown in Figure 7–6. The Q-point is located at the intersection of the load line with the base current curve corresponding to *the base current that flows when* $V_S = 0$, or $I_{BQ}$. By definition, the Q-point locates the *dc* bias values of $V_{CEO}$ and $I_{CO}$, which are the output values when no ac signal is present.

Recall that the load line is a plot of all *possible* combinations of $I_C$ and $V_{CE}$. Therefore, as the base current alternates between its extreme values, the values of $I_C$ and $V_{CE}$ change along the load line producing $\Delta V_{CE}$ and $\Delta I_C$, as indicated in the figure.

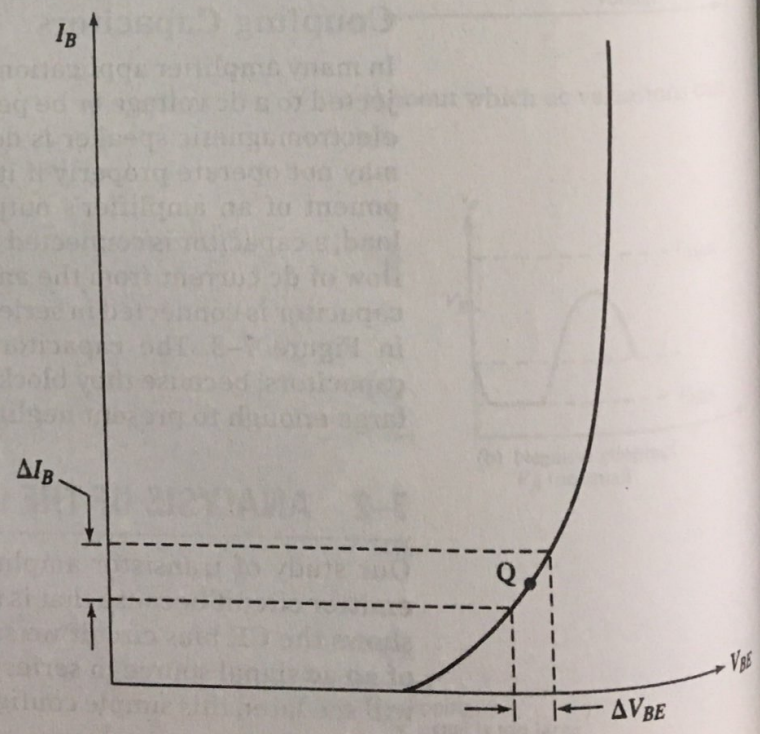


**FIGURE 7–5** A signal voltage produces the change $\Delta V_{BE}$, which translates into $\Delta I_B$

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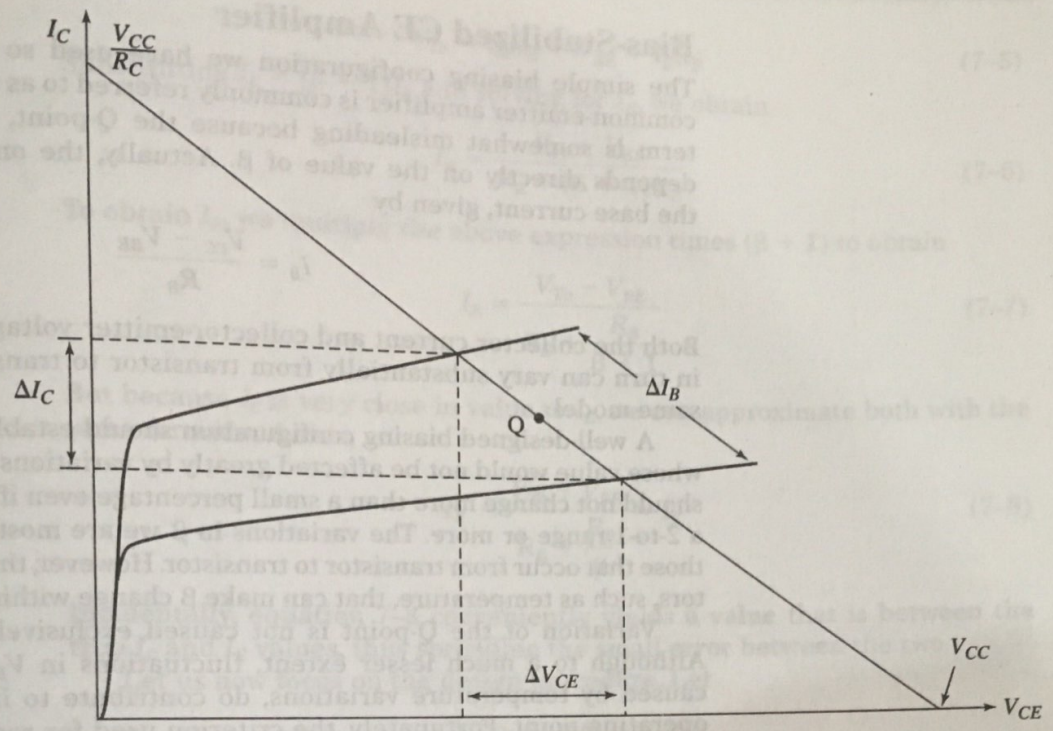


**FIGURE 7–6** The base current change $\Delta I_B$ produces changes $\Delta I_C$ and $\Delta V_{CE}$

Note carefully that $V_{CE}$ *decreases* when $I_B$ and $I_C$ are increasing, and vice versa. Therefore, the sinusoidal voltage $v_{ce}$ is 180° out of phase with each of the sinusoidal currents $i_b$ and $i_c$. Because $i_b$ is in phase with $v_{be}$, we conclude that $v_{ce}$ is also 180° out of phase with $v_{be}$. In other words, *the ac output voltage from a common-emitter amplifier is 180° out of phase with the ac input voltage.* This fact can also be deduced from the load line equation:

$$I_C = \frac{-1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \tag{7–1}$$

or

$$V_{CE} = V_{CC} - I_C R_C$$

Because the term $I_C R_C$ in equation 7–1 subtracts from the constant $V_{CC}$, we observe that an increase in $I_C$ causes a decrease in $V_{CE}$. Thus, as input voltage increases, $I_B$ increases, $I_C$ increases, and $V_{CE}$ decreases. The common-emitter voltage amplifier is said to cause *phase inversion*, or to *invert* voltage.

Concluding, we can also relate this graphical analysis to gains and resistances. The current gain is

$$A_i = \frac{\Delta I_c}{\Delta I_B} \tag{7–2}$$

the voltage gain is

$$A_v = \frac{\Delta V_{CE}}{\Delta V_{BE}} \tag{7–3}$$

and the input resistance looking into the base-emitter junction is

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \tag{7–4}$$

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## Bias-Stabilized CE Amplifier

The simple biasing configuration we have used so far for analyzing the common-emitter amplifier is commonly referred to as a *fixed* bias circuit. The term is somewhat misleading because the Q-point, far from being fixed, depends directly on the value of β. Actually, the only "fixed" variable is the base current, given by

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Both the collector current and collector-emitter voltage depend on β, which in turn can vary substantially from transistor to transistor, even within the same model.

A well-designed biasing configuration should establish a collector current whose value would not be affected greatly by variations in β. In other words, $I_C$ should not change more than a small percentage even if β were to change over a 2-to-1 range or more. The variations in β we are mostly concerned with are those that occur from transistor to transistor. However, there are some other factors, such as temperature, that can make β change within the same transistor.

Variation of the Q-point is not caused exclusively by variations in β. Although to a much lesser extent, fluctuations in $V_{BE}$ and $I_{CBO}$, primarily caused by temperature variations, do contribute to instability of the bias operating point. Fortunately, the criterion used for reducing the effect of β on the Q-point applies also to both $V_{BE}$ and $I_{CBO}$.

Figure 7–7(a) shows the biasing scheme known as the voltage-divider biasing circuit, which can be made arbitrarily insensitive to β variations. The smaller $R_1$ and $R_2$ are made, the "stiffer" the base voltage and collector current will be. However, making $R_1$ and $R_2$ too small will result in an impractically low input resistance. With this trade-off in mind, a good design should allow for some, albeit small, variation in collector current in order to avoid an excessively low input resistance to the amplifying stage.

To simplify the dc analysis of the circuit, it is convenient to use Thévenin's theorem at the voltage divider, resulting in the equivalent circuit shown in Figure 7–7(b), where

$$V_{Th} = \frac{R_2}{R_1 + R_2} V_{CC} \quad \text{and} \quad R_{Th} = R_1 \| R_2 = R_B$$

To obtain an expression for the base current we first write the KVL equation

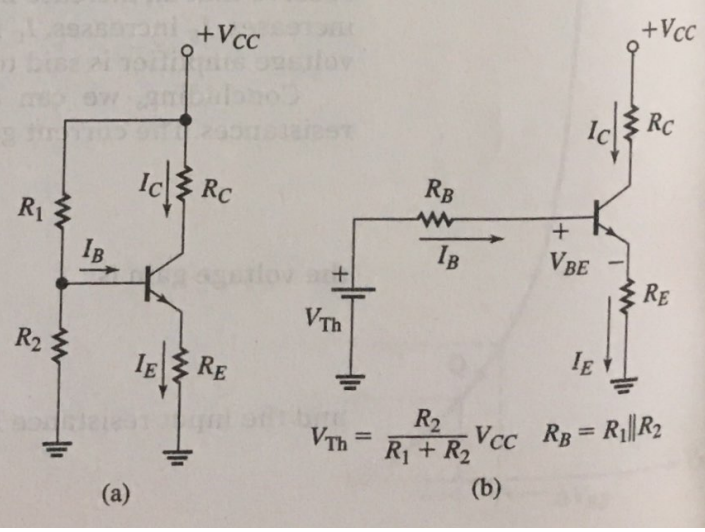


**FIGURE 7–7** Voltage-divider biasing circuit and its Thévenin equivalent

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$$V_{Th} = I_B R_B + V_{BE} + I_E R_E \tag{7–5}$$

Substituting $I_E = (\beta + 1)I_B$ and solving for $I_B$, we obtain

$$I_B = \frac{V_{Th} - V_{BE}}{R_B + (\beta + 1)R_E} \tag{7–6}$$

To obtain $I_E$, we multiply the above expression times $(\beta + 1)$ to obtain

$$I_E = \frac{V_{Th} - V_{BE}}{R_E + \dfrac{R_B}{\beta + 1}} \tag{7–7}$$

But because $I_C$ is very close in value to $I_E$, we can approximate both with the same formula, that is,

$$I_E \approx \frac{V_{Th} - V_{BE}}{R_E + \dfrac{R_B}{\beta}} \approx I_C \tag{7–8}$$

Incidentally, equation 7–8 conveniently yields a value that is between the true $I_C$ and $I_E$ values, thus spreading the small error between the two.

Let us now focus on the design procedure. Let

$\beta_{min}$ = minimum expected value of $\beta$

$\beta_{max}$ = maximum expected value of $\beta$

$I_{Cmin}$ = collector current due to $\beta_{min}$

$I_{Cmax}$ = collector current due to $\beta_{max}$

The extreme values for the collector current according to the extreme values of $\beta$ are

$$I_{Cmax} = \frac{V_{Th} - V_{BE}}{R_E + \dfrac{R_B}{\beta_{max}}} \tag{7–9}$$

and

$$I_{Cmin} = \frac{V_{Th} - V_{BE}}{R_E + \dfrac{R_B}{\beta_{min}}} \tag{7–10}$$

If we solve simultaneously these two equations by equating the $V_{Th} - V_{BE}$ terms, we obtain the expression

$$\frac{R_B}{R_E} = \frac{I_{Cmax} - I_{Cmin}}{I_{Cmin}/\beta_{min} - I_{Cmax}/\beta_{max}} \tag{7–11}$$

which can be used for determining the required $R_B/R_E$ ratio according to the desired allowable variation for $I_C$. Once $R_E$ and $R_B$ are obtained, $V_{Th}$, $R_1$, and $R_2$ will follow.

The following steps summarize the design procedure for the voltage-divider biasing circuit.

1. Given a nominal value for $I_{CQ}$ and a maximum acceptable variation, determine $I_{Cmax}$ and $I_{Cmin}$.
2. With the expected extreme values of $\beta$, determine the required $R_B/R_E$ ratio.
3. Determine $R_E$ using the nominal collector current. A good rule of thumb is to establish a voltage drop across $R_E$ equal to 10% of $V_{CC}$.

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4. Determine $R_B$ from the previously calculated $R_B/R_E$ ratio.
5. Calculate the required $V_{Th}$ using either expression for $I_{Cmin}$ or $I_{Cmax}$.
6. Solve simultaneously the expressions for $V_{Th}$ and $R_B$, that is,

$$V_{Th} = \frac{R_2}{R_1 + R_2} V_{CC} \quad \text{and} \quad R_B = \frac{R_1 R_2}{R_1 + R_2}$$

to obtain

$$R_1 = \frac{V_{CC}}{V_{Th}} R_B \tag{7–12}$$

and then $R_2$ from

$$\frac{1}{R_2} = \frac{1}{R_B} - \frac{1}{R_1}$$

7. Adjust $R_1$ and $R_2$ to the nearest commercial value and calculate the collector current for the two extreme values of β to make sure the design satisfies the requirements.

**EXAMPLE 7–1**

Design a voltage-divider biasing circuit with $V_{CC} = 18$ V, $I_{CQ} = 2$ mA ± 3%, and $V_{CEQ} = 7$ V. Expected β range is 80 to 200. Specify commercial values for resistors.

**Solution**

Using a voltage drop across $R_E$ of 10% of $V_{CC}$, $R_E = 1.8$ V/2 mA = 900 Ω. The closest commercial value is 910 Ω.

The collector resistor is $R_C = V_{R_C}/I_{CQ}$, where $V_{R_C} = V_{CC} - V_{CE} - V_{R_E}$ according to KVL. Then $V_{R_C} = 18 - 7 - 1.8 = 9.2$ V and $R_C = 9.2$ V/2 mA = 4.6 kΩ. We will use 4.7 kΩ.

With the ±3% allowable collector current variation, we obtain $I_{Cmax}$ = 2.06 mA and $I_{Cmin}$ = 1.94 mA. The ratio $R_B/R_E$ can now be calculated using equation 7–11:

$$\frac{R_B}{R_E} = \frac{2.06 - 1.94}{1.94/80 - 2.06/200} = 8.6$$

from which we obtain $R_B = 8.6(910\ \Omega) = 7.83$ kΩ. Solving for $V_{Th}$ from the expression for $I_{Cmax}$, we obtain $V_{Th} = I_{Cmax}(R_E + R_B/\beta_{max}) + V_{BE} = 2.06(0.910 + 7.83/200) + 0.7 = 2.66$ V. (Note that the numbers were entered in mA and kΩ, consistent with volts.) You can also verify that the same result is obtained by using the expression for $I_{Cmin}$. Using equation 7–12, we obtain $R_1 = (V_{CC}/V_{Th})R_B = (18/2.66)7.83$ kΩ = 53 kΩ, from which it follows $R_2 = (1/7.83\text{ k} - 1/53\text{ k})^{-1} = 9.2$ kΩ. The closest commercial values are $R_1 = 51$ kΩ and $R_2 = 9.1$ kΩ.

To verify our design, we calculate $I_{Cmax}$ and $I_{Cmin}$ using the commercial values for resistance we have specified. First, $V_{Th} = (9.1/60.1)18 = 2.73$ V, and $R_B = 51 \| 9.1 = 7.72$ kΩ. Then,

$$I_{Cmin} = \frac{2.73 - 0.7}{0.91 + 7.72/80} = 2.02 \text{ mA} \quad \text{and} \quad I_{Cmax} = \frac{2.73 - 0.7}{0.91 + 7.72/200} = 2.14 \text{ mA}$$

You can see that even though the resulting currents are slightly off due to using commercial resistor values, the total variation in collector current is 0.12 mA, as specified.

In order to use the bias-stabilized circuit as a common-emitter amplifier, besides the input and output coupling capacitors, there may be a need

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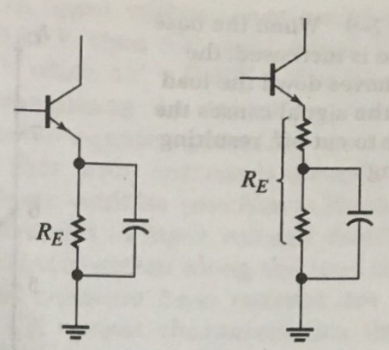
FIGURE 7–8 Using a bypass capacitor for the emitter




(a) Fully bypassed emitter resistor (b) Partly bypassed emitter resistor

for using a bypass capacitor across the emitter resistor in order to place the emitter at *zero ac potential* or *ac ground*, as shown in Figure 7–8(a). It is also possible to partially bypass the emitter resistor as shown in Figure 7–8(b) in order to have control on the gain, as we will see shortly, and also for reducing distortion. The circuit could be used with no bypass capacitor at all, but at the cost of substantially reduced gain.

We will examine in full detail this amplifying configuration along with other configurations later in the chapter using *small-signal models*. However, a few issues regarding the relationship between dc biasing and ac performance need to be addressed beforehand.

## The Effect of Q-Point Location on ac Operation

Let us consider now how the location of the Q-point affects the ac operation of the amplifier. Suppose the value of the base resistor $R_B$ in Figure 7–4 is increased. The quiescent value of the base current will then become smaller. Figure 7–9 shows that the Q-point in this case is shifted down the load line to the point where it intersects the $I_{BQ}$ curve. When the base current increases beyond the Q-point to $I_{Bmax}$, it can be seen in Figure 7–9 that the collector current increases to $I_{Cmax}$ and $V_{CE}$ decreases to $V_{CEmin}$. However, when the base current decreases below the Q-point, the transistor enters its cutoff region. Clearly $I_C$ cannot be less than 0 and $V_{CE}$ cannot be greater than $V_{CC}$. As shown in the figure, the output current prematurely becomes 0 in the sine-wave cycle, and clipping results. At the same time, $V_{CE}$ reaches its limit of $V_{CC}$, and the output waveform shows positive clipping. With the Q-point in its new location, the output voltage change cannot exceed $V_{CC} - V_Q$ without positive clipping occurring. Thus, the maximum peak-to-peak output voltage is $2(V_{CC} - V_Q)$, and it represents the *maximum output swing*. This reduced swing limits the usefulness of the amplifier and illustrates the importance of locating the bias point somewhere near the center of the load line.

If the Q-point is located too far *up* the load line, the output swing will be limited by the onset of saturation. This fact is illustrated in Figure 7–10(a). In this case, a substantial increase in base current beyond its quiescent value causes the transistor to saturate. The collector current cannot exceed its saturation value and $V_{CE}$ cannot be less than 0. Consequently, the output voltage is a negatively clipped waveform, as shown in the figure.

Even if the Q-point is located at the center of the load line, positive and negative clipping can occur if the input signal is too large. Figure 7–10(b) shows what happens when the total change in base current is so great that the transistor is driven into saturation at one end and cutoff at the other. We see that both positive and negative clipping occur due to the amplifier being *overdriven*.

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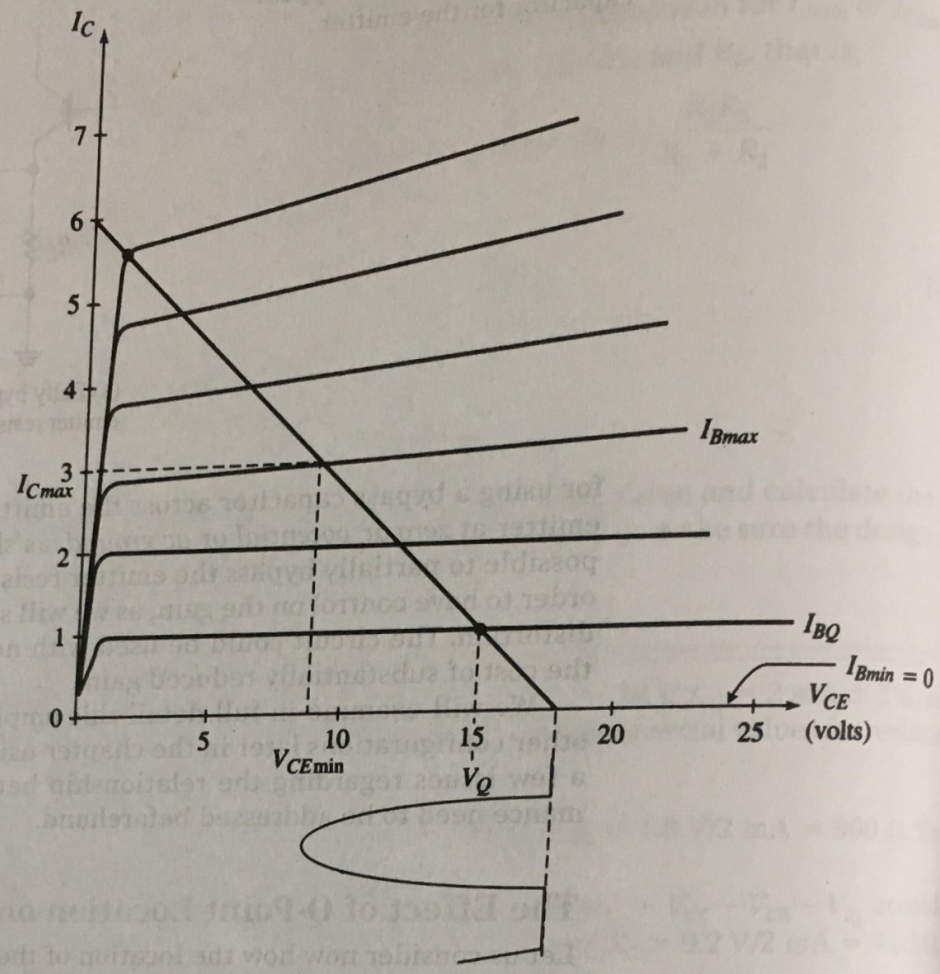
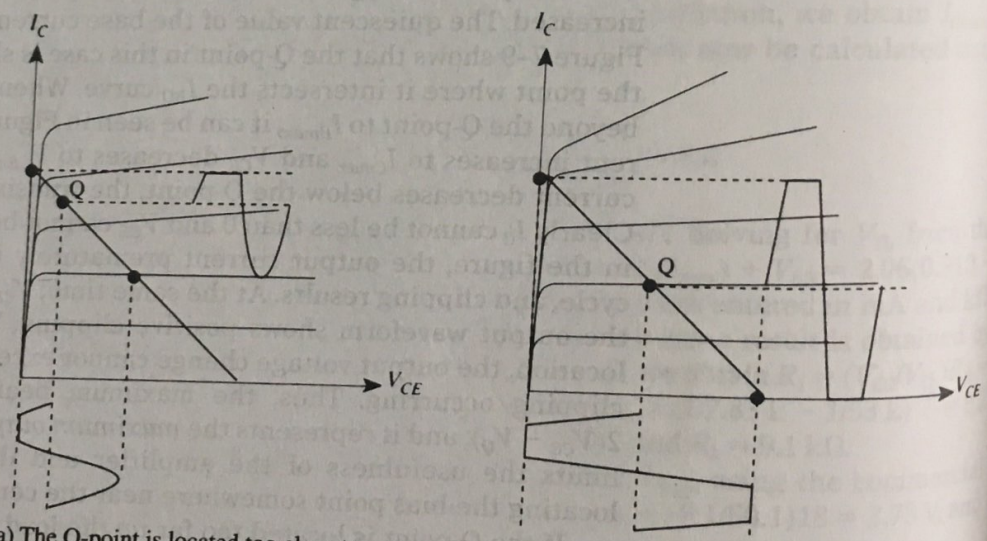



**FIGURE 7–9** When the base resistance is increased, the Q-point moves down the load line and the signal causes the amplifier to cut off, resulting in clipping

**FIGURE 7–10**




(a) The Q-point is located too close to saturation and the output voltage shows negative clipping.

(b) Too large an input signal causes both positive and negative clipping.

## Linearity and Distortion

To be useful, an amplifier's output waveform must be a faithful replica of the input waveform (or a phase-inverted replica of the input). That clearly is not the case when clipping occurs. Apart from clipping, the degree to which the output waveform has the same shape as the input depends upon the amplifier's *linearity*. To be linear, any change in output voltage must be

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*directly proportional* to the change in input voltage that created it. For example, if $\Delta V_o = 1$ V when $\Delta V_i = 0.01$ V, then $\Delta V_o$ must equal 2 V when $\Delta V_i = 0.02$ V, and $\Delta V_o$ must equal 0.5 V when $\Delta V_i = 0.005$ V. The linearity of a transistor can be determined by examining the extent to which equal increments of base current correspond to equally spaced curves on the CE output characteristics. If we assume that input current is directly proportional to input voltage (i.e., that the base–emitter junction is linear, in the sense discussed in Chapter 3), then changes in input voltage should cause the output voltage to vary to a proportional extent along the load line. This will be the case only if the curves of constant base current are equally spaced. Figure 7–11 shows a set of CE output characteristics that have been intentionally distorted to exaggerate nonuniform spacing. Notice that the distance between the curves increases for larger values of base current.

The active region of a transistor's output characteristics is the region where the base current curves are generally found to have equal or nearly equal spacing. For this reason, the active region is often called the *linear* region. Of course, the characteristics shown in Figure 7–11 are decidedly nonlinear. In this example, the nonlinearity is due to the fact that device parameters (such as β) change significantly over the region of operation.

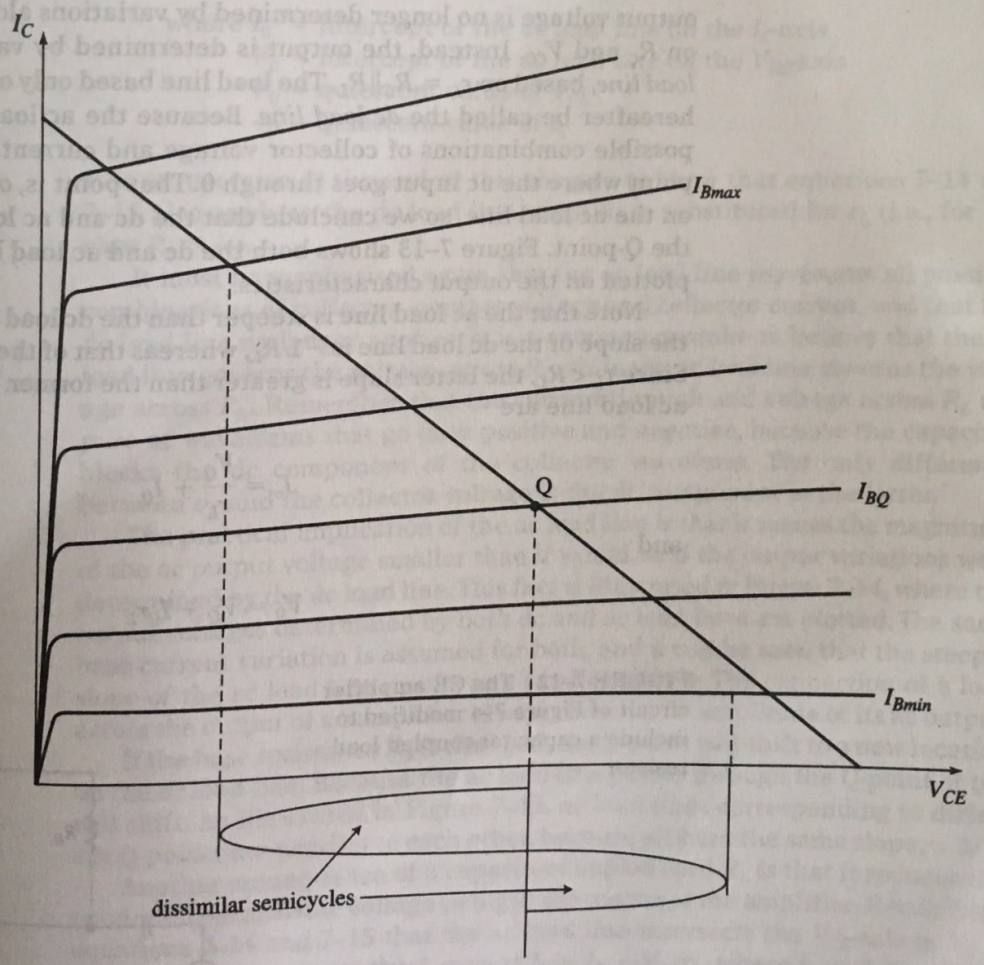


**FIGURE 7–11** Unequal spacing between equal intervals of base current represents a nonlinear characteristic that causes a distorted output

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Small-signal analysis of this device would thus be restricted to a very small range of operation along the load line.

## The Effect of Load Resistance on ac Operation

Let us now consider the effect of connecting a load resistor $R_L$ across the output of the CE amplifier, as shown in Figure 7–12. It is important to realize that *as far as ac performance is concerned, $R_L$ is in parallel with $R_C$. A dc source is a short circuit to ac signals*, so resistor $R_C$ in Figure 7–12 is effectively grounded through $V_{CC}$, and the ac voltage at the collector "sees" $R_C$ in parallel with $R_L$. Another way of viewing this is from the standpoint of analysis by superposition: If we are interested in the output voltage due only to the ac source, $v_S$, we replace all other voltage sources by short circuits.

The ac load resistance, designated $r_L$, is the parallel combination of $R_C$ and $R_L$:

$$r_L = R_C \| R_L = \frac{R_C R_L}{R_C + R_L} \tag{7–13}$$

The dc load resistance is, of course, still equal to $R_C$ because the coupling capacitor blocks the flow of dc current into the load resistor.

The existence of an ac load that differs from the dc load means that the output voltage is no longer determined by variations along a load line based on $R_C$ and $V_{CC}$. Instead, the output is determined by variations along an *ac load line*, based on $r_L = R_C \| R_L$. The load line based only on the value of $R_C$ will hereafter be called the *dc load line*. Because the ac load line represents all possible combinations of collector voltage and current, it must include the point where the ac input goes through 0. That point is, of course, the Q-point on the dc load line, so we conclude that the dc and ac load lines intersect at the Q-point. Figure 7–13 shows both the dc and ac load lines of this example plotted on the output characteristics.

Note that the ac load line is steeper than the dc load line. Remember that the slope of the dc load line is $-1/R_L$, whereas that of the ac load line is $-1/r_L$. Since $r_L < R_L$, the latter slope is greater than the former. The intercepts of the ac load line are

$$I_o = \frac{V_Q}{r_L} + I_Q \tag{7–14}$$

and

$$V_0 = V_Q + I_Q r_L \tag{7–15}$$

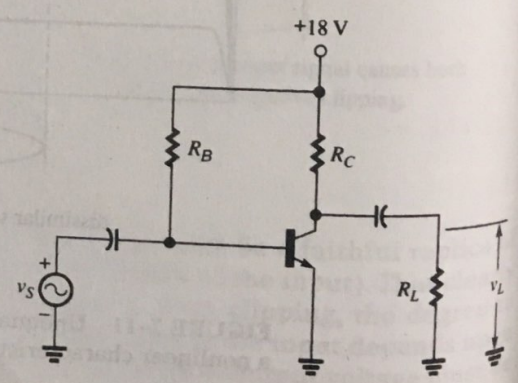


**FIGURE 7–12** The CE amplifier circuit of Figure 7–4 modified to include a capacitor-coupled load resistor

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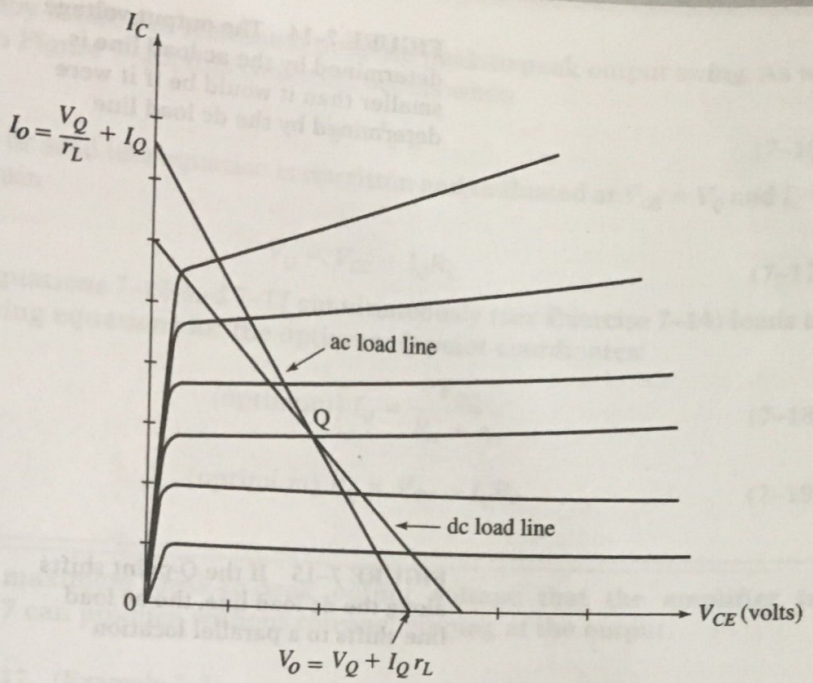
FIGURE 7–13 dc and ac load lines




where $I_0$ = intercept of the ac load line on the $I_C$-axis
$V_0$ = intercept of the ac load line on the $V_{CE}$-axis
$V_Q$ = quiescent value of $V_{CE}$
$I_Q$ = quiescent value of $I_C$

It is an exercise at the end of this chapter to show that equations 7–14 and 7–15 also apply to the dc load line when $R_C$ is substituted for $r_L$ (i.e., for the case $R_L = \infty$).

It must be emphasized again that the ac load line represents all possible combinations of collector–emitter voltage and collector current, and that the dc load line no longer applies. It is a common mistake to believe that the dc load line governs the voltage across $R_C$ while the ac load line governs the voltage across $R_L$. Remember that the current through and voltage across $R_L$ are pure ac waveforms that go both positive and negative, because the capacitor blocks the dc component of the collector waveform. The only difference between $v_L$ and the collector voltage is the dc component in the latter.

The practical implication of the ac load line is that it makes the magnitude of the ac output voltage smaller than it would be if the output variations were determined by the dc load line. This fact is illustrated in Figure 7–14, where the output voltages determined by both dc and ac load lines are plotted. The same base-current variation is assumed for both, and it can be seen that the steeper slope of the ac load line results in a smaller output. The connection of a load across the output of an amplifier always reduces the amplitude of its ac output.

If the base resistance $R_B$ is changed, the Q-point will shift to a new location on the *dc* load line. Because the ac load line passes through the Q-point, it too will shift. As illustrated in Figure 7–15, ac load lines corresponding to different Q-points are parallel to each other, because all have the same slope, $-1/r_L$.

Another consequence of a capacitor-coupled load $R_L$ is that it reduces the maximum permissible voltage swing at the output of the amplifier. Recall from equations 7–14 and 7–15 that the ac load line intersects the $V_{CE}$-axis at $V_0 = V_Q + I_Q r_L$ and intersects the $I_C$-axis at $I_0 = I_Q + V_Q/r_L$, where $I_Q$ and $V_Q$ are the Q-point coordinates. It is therefore clear that the positive-going output voltage cannot exceed the bias voltage by more than $I_Q r_L$ volts. This fact is illustrated

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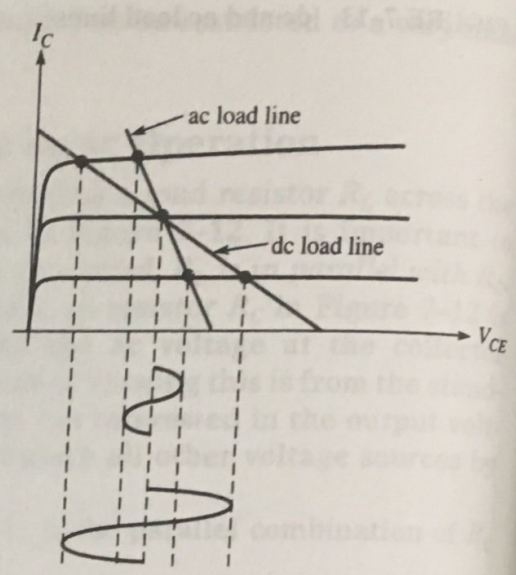


**FIGURE 7–14** The output voltage determined by the ac load line is smaller than it would be if it were determined by the dc load line

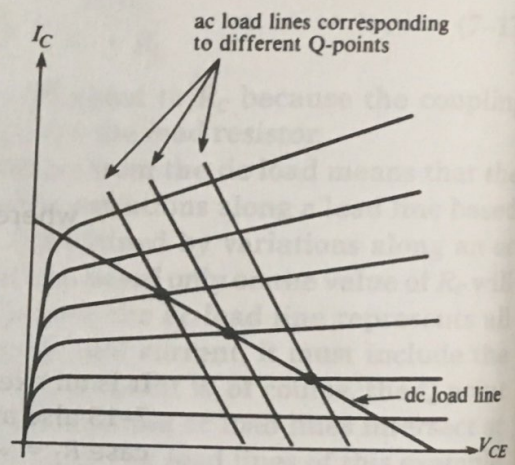


**FIGURE 7–15** If the Q-point shifts along the dc load line, the ac load line shifts to a parallel location

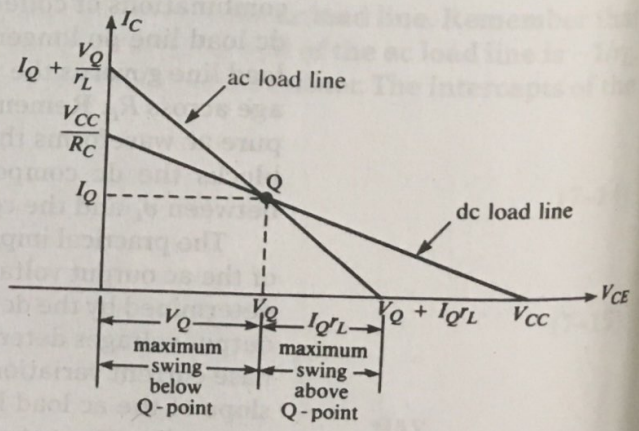


**FIGURE 7–16** The ac load line limits the output voltage swing to the minimum of $V_Q$ and $I_Q r_L$

in Figure 7–16. The output voltage can swing $I_Q r_L$ volts above the Q-point and $V_Q$ volts below the Q-point. Thus the maximum peak output voltage is the *minimum* of the two values $V_Q$ and $I_Q r_L$. If the output attempts to exceed $V_Q$ by more than $I_Q r_L$ volts, its positive peak will be clipped; if it attempts to swing more than $V_Q$ volts below $V_Q$, its negative peak will be clipped.

Figure 7–15 in our discussion of graphical amplifier analysis shows that the ac load line shifts with changes in the Q-point. It is obvious that shifting the ac load line causes it to have different intercepts on the horizontal and vertical axes. It should therefore be possible to locate the Q-point in such a way that the maximum positive swing equals the maximum negative swing,

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and thereby attain the maximum possible peak-to-peak output swing. As we can see in Figure 7–16, this condition occurs when

$$V_Q = I_Q r_L \tag{7–16}$$

When the dc load line equation is rewritten and evaluated at $V_{CE} = V_Q$ and $I_C = I_Q$, we obtain

$$V_Q = V_{CC} - I_Q R_C \tag{7–17}$$

Solving equations 7–16 and 7–17 simultaneously (see Exercise 7–14) leads to the following equations for the optimum Q-point coordinates:

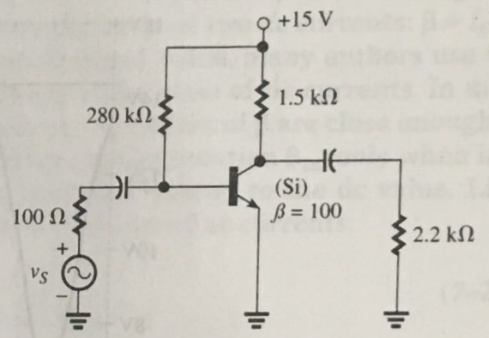
$$\text{(optimum) } I_Q = \frac{V_{CC}}{R_C + r_L} \tag{7–18}$$

$$\text{(optimum) } V_Q = V_{CC} - I_Q R_C \tag{7–19}$$

**EXAMPLE 7–2**

Find the maximum peak-to-peak output voltage that the amplifier in Figure 7–17 can produce without causing clipping at the output.

**FIGURE 7–17** (Example 7–2)




**Solution**

Solving first for the quiescent values, we have

$$I_B = \frac{(15 - 0.7)\text{V}}{280 \times 10^3\ \Omega} = 51.1\ \mu\text{A}$$

$$I_C = I_Q = \beta I_B = 100(51.1\ \mu\text{A}) = 5.11\ \text{mA}$$

$$V_Q = V_{CC} - I_Q R_C = 15\ \text{V} - (5.11\ \text{mA})(1.5\ \text{k}\Omega) = 7.34\ \text{V}$$

$$r_L = R_C \| R_L = (1.5\ \text{k}\Omega) \| (2.2\ \text{k}\Omega) = 892\ \Omega$$

Therefore, the maximum output swing *above* $V_Q = 7.34$ V is $I_Q r_L = (5.11\ \text{mA})(892\ \Omega) = 4.56$ V. Because $V_Q = 7.34$ V, the maximum output variation from the Q-point is the minimum of 4.56 V and 7.34 V, or 4.56 V. Thus, the maximum peak-to-peak ac output is (2)(4.56) = 9.12 V p–p.

**EXAMPLE 7–3**

**PSPICE**

Use PSpice to obtain a plot of $v_{ce}$ versus time in the circuit shown on the next page. The plot should cover two full cycles of output. Also find the quiescent values of $V_{CE}$ and $I_C$.

**Solution**

To obtain a plot of $v_{ce}$ versus time, we must use a SIN source and perform a .TRAN analysis (see Appendix Sections A–4 and A–5). In order for the plot to

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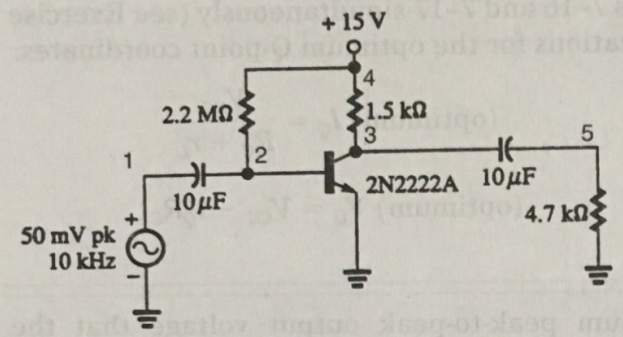
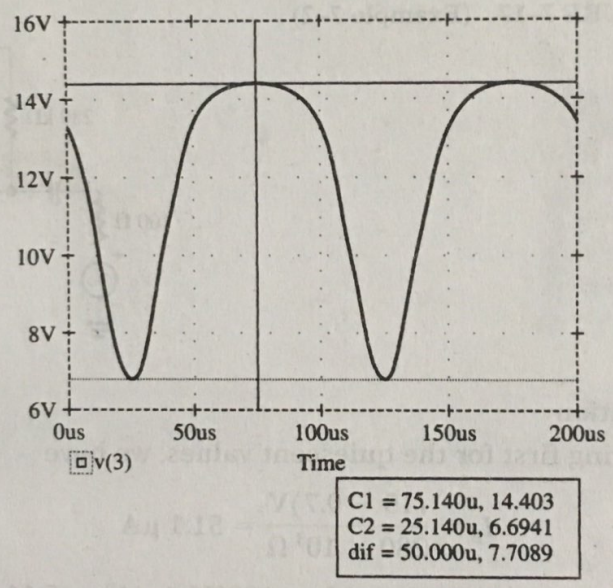
cover two full cycles, we set *TSTOP* in the .TRAN statement to two times the period of the sine wave: 2(1/10 kHz) = 0.2 ms.

Also shown is the PSpice input circuit file. Note that we use the PSpice library to access the model statement for the 2N2222A transistor (see Appendix Section A–17). Also note that the Q-point can be obtained in a PSpice .PRINT statement by requesting outputs IC(Q1) (the dc collector current of Q1) and VCE(Q1) (the dc collector-to-emitter voltage of Q1).




```
EXAMPLE 7-3
VS 1 0 SIN(0 50MV 10KHZ 0 0)
VCC 4 0 15V
C1 1 2 10UF
C2 3 5 10UF
RB 2 4 2.2MEG
RC 3 4 1.5K
RL 5 0 4.7K
Q1 3 2 0 Q2N2222
.LIB EVAL.LIB
.TRAN 500NS 0.2MS 0 500NS
.PROBE
.END
```

(EVAL.LIB for Evaluation version of PSpice only)




Execution of the program reveals that IC(Q1) = 1.125 mA and VCE(Q1) = 13.31 V. Since $V_{CC}$ = 15 V, this quiescent point is close to the cutoff region of the transistor. We might therefore expect positive clipping to occur if the input to the amplifier is sufficiently large (see Figure 7–9). The plot produced by the PSpice Probe option (Section A–16) is shown, and we see that clipping does indeed occur. The Probe cursors are set at the minimum and maximum values of $v_{ce}$, C1 = 14.403 V and C2 = 6.6941 V. Thus, positive clipping occurs at $v_{ce}$ = 14.403 V.

## 7–3 AMPLIFIER ANALYSIS USING SMALL-SIGNAL MODELS

### Small-Signal Parameters

Because transistor circuits are usually analyzed using algebraic rather than graphical methods, it is convenient to have an equivalent circuit that can be substituted for the transistor wherever it appears. Many different kinds of equivalent circuits have been developed for transistors, each of which has

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special features that make it more useful or more accurate than others for a particular kind of analysis. The form that an equivalent circuit takes depends on the transistor *parameters* that are chosen as the basis for the circuit. A transistor parameter is simply a transistor characteristic or property that can be given a numerical value. For example, α and β are transistor parameters. The latter are examples of *derived* parameters: They are computed from a numerical relationship between two quantities (the ratio of two currents, in this case). Transistor parameters can also specify inherent physical characteristics, such as the resistance of the base region or the width of the collector–base depletion region.

Small-signal parameters are parameters whose values are determined under small-signal (ac) operating conditions and at the operating bias point. For example, the small-signal value of β is defined to be

$$\beta = \left.\frac{i_c}{i_b}\right|_{V_{CEQ}} \tag{7–20}$$

Equation 7–20 states that small-signal β is the ratio of ac collector current to ac base current at the quiescent value of $V_{CE}$. Small-signal β can be determined from a set of collector characteristics by constructing a vertical line at $V_{CEQ}$ and finding $\Delta I_C/\Delta I_B$ along that line. Up to now, we have computed the (approximate) value of β by taking the ratio of two *dc* currents: $\beta \approx I_C/I_B$. To distinguish this value from the small-signal value, many authors use the notation $\beta_{DC}$ ("dc beta") when referring to the ratio of dc currents. In most practical applications, the small-signal and dc values of β are close enough to be assumed equal, and we will hereafter use the notation $\beta_{DC}$ only when it is necessary to emphasize that we are referring strictly to the dc value. Like small-signal β, small-signal α is defined in terms of ac currents:

$$\alpha = \left.\frac{i_c}{i_e}\right|_{V_{CBQ}} \tag{7–21}$$

An important physical parameter of a transistor is its small-signal resistance from emitter to base, called the *dynamic emitter resistance* and designated $r'_e$. This resistance is the same as the small-signal input resistance of the transistor in its common-base configuration. It is defined as

$$r'_e = \left.\frac{v_{eb}}{i_e}\right|_{V_{CEQ}} \tag{7–22}$$

Because the emitter–base junction can be regarded as a forward-biased diode, an approximate value for $r'_e$ can be found in the same way in which we found the dynamic resistance of a diode (Chapter 3). Recall that $r_D \approx V_T/I \approx 0.026/I$ at room temperature, where $I$ is the dc current in the diode. Similarly,

$$r'_e \approx \frac{26\text{ mV}}{I_{EQ}} \tag{7–23}$$

where $I_{EQ}$ is the Q-point emitter current.

The small-signal collector resistance $r_c$ is the ac resistance from collector to base. It is the same as the output resistance of a transistor in its common-base configuration and typically has a value of several megohms, because it is across a reverse-biased junction.

$$r_c = \left.\frac{v_{cb}}{i_c}\right|_{I_{EQ}} \tag{7–24}$$

It is important to emphasize that small-signal parameters, in general, depend directly on the dc biasing conditions of the circuit.

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## Small-Signal CB Amplifier Model

An equivalent circuit for an electronic device is called a *model*. Using just the parameters we have discussed so far, we can construct a simple but reasonably accurate small-signal model for a transistor. Figure 7–18 shows a transistor in the common-base configuration and its approximate small-signal model. Remember that all voltages and currents are ac quantities, so all polarities periodically alternate. The polarities shown in the figure should be interpreted as reference directions for instantaneous values. For example, Figure 7–18(a) shows that an increase of current into the emitter terminal is accompanied by an increase of current out of the collector terminal. Models are the same for *npn* and *pnp* devices.

Notice that the model in Figure 7–18 includes a *controlled* ac current source that produces a current equal to $\alpha i_e$. (Notice also the standard symbol for such a controlled source.) Thus, the collector current $i_c$ is approximately equal to $\alpha i_e$, so the model accurately reflects the relationship between $i_e$ and $i_c$. The model does *not* show the feedback effect we discussed in Chapter 4; that is, it does not reflect the fact that the value of $i_e$ depends on the value of $V_{CB}$. For most practical design and analysis problems, the feedback effect is insignificant and can be ignored.

It is clear that the transistor input resistance equals $r'_e$ in our approximate CB model. This is a relatively small value, usually less than 50 Ω.

$$r_i = r'_e \quad \text{(common base)} \tag{7–25}$$

The transistor output resistance, on the other hand, can be seen to equal the large collector-base resistance $r_c$:

$$r_o = r_c \quad \text{(common base)} \tag{7–26}$$

The dynamic resistance $r_c$ can also be described as

$$r_c = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_{EQ}} \quad \text{(at the operating emitter current)} \tag{7–27}$$

and can be seen graphically on the characteristic CB output curves as the reciprocal of the slope of the curve corresponding to $I_{EQ}$ in the active region.

To illustrate how the small-signal model can be used to analyze a practical amplifier, we will incorporate it into the CB amplifier circuit shown in Figure 7–19(a). Figure 7–19(b) shows the ac equivalent of just that part of (a) that is external to the transistor. Note that all dc sources are treated as ac short circuits to ground, in accordance with our previous discussion. Also, the coupling capacitor is assumed to have negligible impedance and is replaced by a short in the ac equivalent circuit. Finally, Figure 7–19(c) shows the complete ac equivalent when the transistor is replaced by its small-signal model.

In Figure 7–19(c), we see that $R_E$ is in parallel with $r'_e$ and that $r_c$ is in parallel with $R_C$. In practical circuits, $R_E$ is usually much greater than $r'_e$ ($R_E \gg r'_e$), so

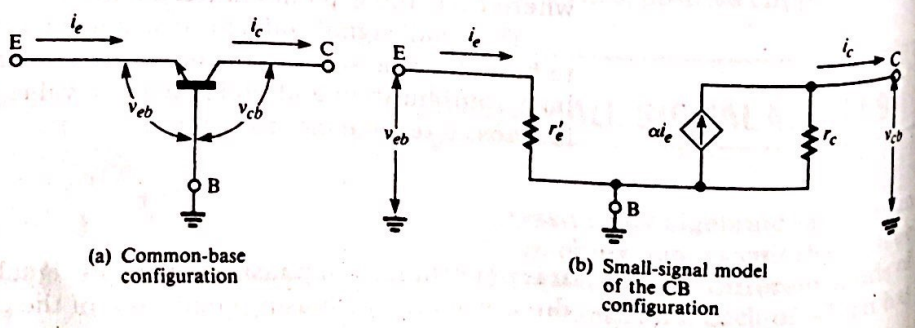


**FIGURE 7–18** A CB transistor and its small-signal model

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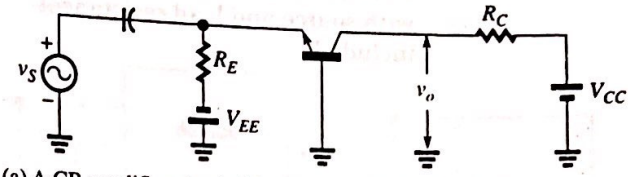
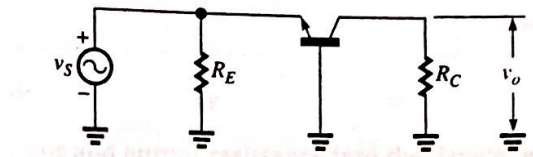
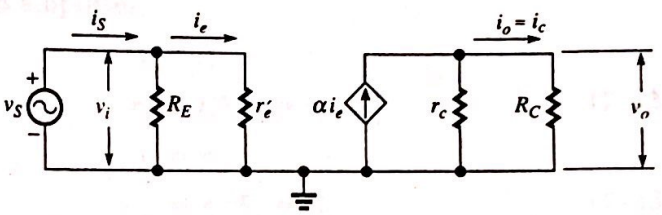
**FIGURE 7–19** Evolution of an ac equivalent circuit for a common-base amplifier




(a) A CB amplifier circuit driven by a small-signal voltage source, $v_S$

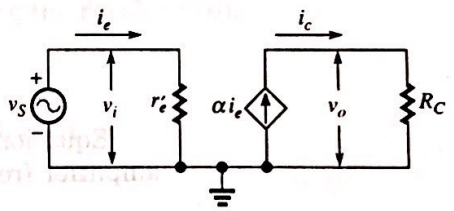



(b) The CB amplifier of (a) when the circuit external to the transistor is replaced by its ac equivalent




(c) The complete, small-signal CB equivalent circuit, when the transistor in (b) is replaced by its model

**FIGURE 7–20** A practical CB equivalent circuit that incorporates the (usual) condition that $r'_e \| R_E \approx r'_e$ and $R_C \| r_c \approx R_C$




the parallel combination $R_E \parallel r'_e$ essentially equals $r'_e$. Also, $r_c \gg R_C$ in practical circuits, so $r_c \parallel R_C$ essentially equals $R_C$. Thus, Figure 7–19(c) can be replaced by the practical equivalent shown in Figure 7–20.

In Figure 7–20, it is clear that

$$v_S = v_i = i_e r'_e \quad \text{and} \quad v_o = i_c R_C = \alpha\, i_e R_C$$

or, since $\alpha \approx 1$, $v_o \approx i_e R_C$. Therefore, the voltage gain is

$$A_v = \frac{v_o}{v_i} \approx \frac{i_e R_C}{i_e r'_e} = \frac{R_C}{r'_e} \tag{7–28}$$

The current gain in Figure 7–20 is

$$A_i = \frac{i_o}{i_i} = \frac{i_c}{i_e} = \alpha \tag{7–29}$$

Thus, the current gain of a CB amplifier is always less than 1.

Figure 7–21(a) shows a CB amplifier that is driven by a source having internal resistance $r_S$. The amplifier load is the resistor $R_L$. Figure 7–21(b) shows the ac equivalent circuit that results when the assumptions $R_E \| r'_e \approx r'_e$ and $r_c \| R_C \approx R_C$ are once again imposed. Figure 7–21(c) shows the amplifier circuit when the transistor is replaced by a single block having the parameters described previously. Note that the voltage source in Figure 7–21(c) is the (Thévenin) equivalent of the current source in Figure 7–20.

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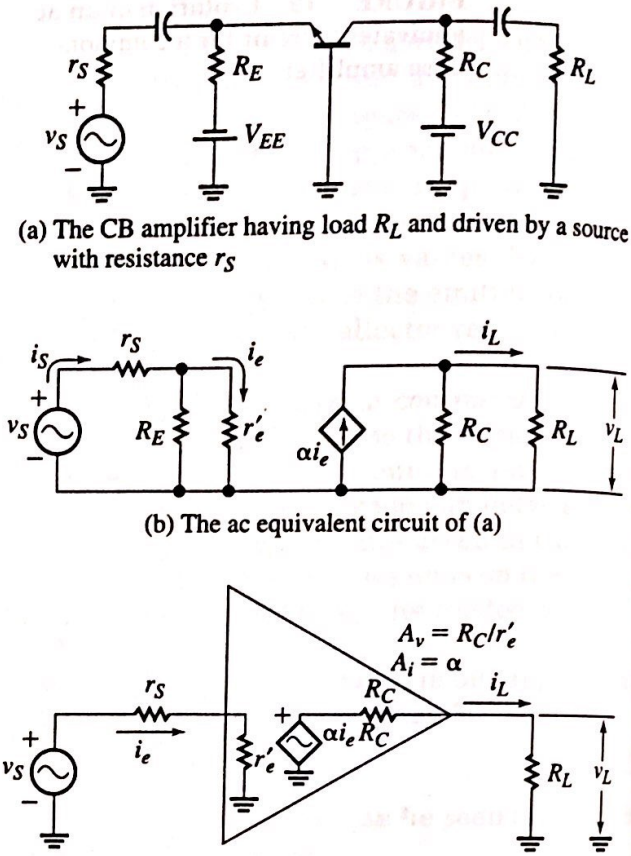
**FIGURE 7–21** The CB amplifier with source and load resistances included




(a) The CB amplifier having load $R_L$ and driven by a source with resistance $r_S$

(b) The ac equivalent circuit of (a)

(c) The circuit of (b) when the transistor is replaced by a single amplifier block

Equation 6–17 in Section 6–2 gives the overall voltage gain of an ac amplifier, from source to load. Applying the equation to Figure 7–21(c), we have

$$A_{vs} = \frac{v_L}{v_S} = \frac{R_C}{r'_e}\left(\frac{r'_e}{r_S + r'_e}\right)\left(\frac{R_L}{R_C + R_L}\right) \tag{7–30}$$

which reduces to

$$A_{vs} = \frac{R_C \| R_L}{r'_e + r_S} = \frac{r_L}{r'_e + r_S} \tag{7–31}$$

The ac output voltage from a CB amplifier is *in phase* with the ac input voltage since the gain is positive. We can also deduce this fact by the following: An increase in emitter-to-base (input) voltage reduces the forward bias on the emitter-base junction and thus reduces the emitter current. But a decrease in emitter current causes a decrease in collector current, since $I_C = \alpha I_E$. Decreasing $I_C$ causes the voltage drop $I_C R_C$ to decrease and therefore causes $V_{CB}$ to increase. Recapitulating, an increase in emitter (input) voltage causes an increase in collector (output) voltage, and we conclude that input and output are in phase.

When a transistor is connected in a circuit to produce gain, the transistor and all the associated external components it needs to operate properly (such as bias resistors) are referred to collectively as an amplifier *stage*. It is important to distinguish between the input and output resistances of the transistor alone and those of the stage of which it is a part. Hereafter, we will use the subscripts *in* and *out* when we wish to emphasize that it refers to a stage characteristic. Figure 7–22 illustrates these distinctions in a general amplifier stage.

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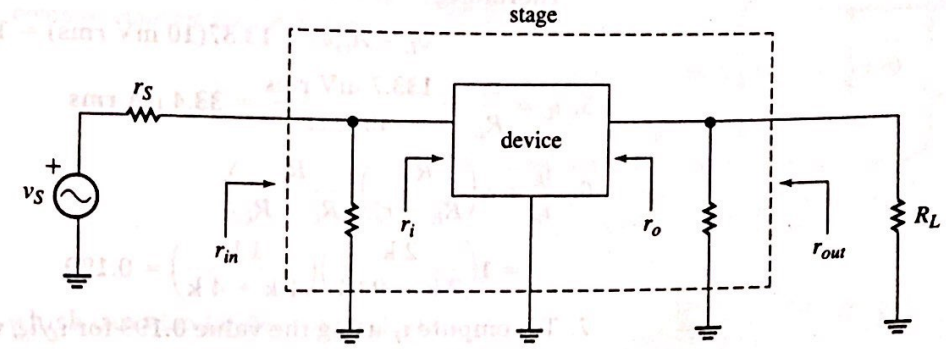



**FIGURE 7–22** $r_i$ and $r_o$ are input and output resistance into the device, whereas $r_{in}$ and $r_{out}$ refer to input and output resistances of the amplifier stage

We note that for a CB amplifier,

$$r_i = r'_e$$

$$r_{in} = r'_e \| R_E \approx r'_e \tag{7–32}$$

$$r_o = r_c$$

$$r_{out} = r_c \| R_C \approx R_C \tag{7–33}$$

**EXAMPLE 7–4**

For the circuit in Figure 7–23, find (1) $r_i$, (2) $r_{in}$, (3) $A_v$, (4) $v_L$, (5) $i_L$, (6) $i_L/i_S$ (assume that $\alpha = 1$), and (7) $i_L$, using the result of (6).

**Solution**

1. $I_E = \dfrac{|V_{EE}| - |V_{EB}|}{R_E} = \dfrac{6 - 0.7}{2\text{ k}\Omega} = 2.65\text{ mA}$

Therefore,

$$r_i = r'_e = \frac{26\text{ mV}}{2.65\text{ mA}} = 9.81\ \Omega$$

2. $r_{in} = r'_e \| R_E = \dfrac{(9.81)(2000)}{2009.81} = 9.76\ \Omega$

This result confirms equation 7–32, because for all practical purposes,

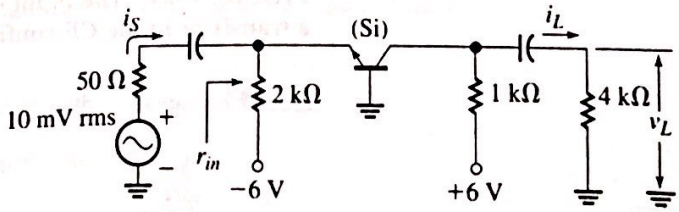
$$r_{in} = r'_e = 9.81\ \Omega$$

3. $A_v = R_C/r'_e = 1000/9.81 = 101.9$

4. $A_{vS} = 101.9\left(\dfrac{r'_e}{r_S + r'_e}\right)\left(\dfrac{R_L}{R_L + R_C}\right)$

$$= 101.9\left(\frac{9.81}{50 + 9.81}\right)\left(\frac{4\text{ k}}{1\text{ k} + 4\text{ k}}\right) = 13.37$$

**FIGURE 7–23** (Example 7–4)

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Therefore,

$$v_L = A_{vs}v_S = 13.37(10 \text{ mV rms}) = 133.7 \text{ mV rms}$$

5. $i_L = \dfrac{v_L}{R_L} = \dfrac{133.7 \text{ mV rms}}{4000\ \Omega} = 33.4\ \mu\text{A rms}$

6. $\dfrac{i_L}{i_S} = \alpha\left(\dfrac{R_E}{R_E + r'_e}\right)\left(\dfrac{R_C}{R_C + R_L}\right)$

$$= 1\left(\frac{2\text{ k}}{2\text{ k} + 9.81}\right)\left(\frac{1\text{ k}}{1\text{ k} + 4\text{ k}}\right) = 0.199$$

7. To compute $i_L$ using the value 0.199 for $i_L/i_S$, we must first find the source current $i_S$.

$$i_S = \frac{10 \text{ mV}}{50\ \Omega + 9.81\ \Omega} = 167\ \mu\text{A}$$

Then, $i_L = 0.199\ (167\ \mu\text{A}) = 33.2\ \mu\text{A}$, which agrees with the value previously found.

## Small-Signal CE Amplifier Model

To develop a model for the transistor in its common-emitter configuration, we will first investigate the input resistance in that configuration. Figure 7–24 shows the CE input circuit with $r'_e$ drawn inside the emitter terminal, to emphasize that it is an internal transistor parameter. The ac input resistance is $r_i = v_{be}/i_b$. Recalling that $i_e = (\beta + 1)i_b$, we have

$$r_i = \frac{v_{be}}{i_e/(\beta + 1)} = (\beta + 1)\frac{v_{be}}{i_e}$$

But $v_{be}/i_e = r'_e$, so

$$r_i = (\beta + 1)r'_e \approx \beta r'_e \quad \text{(common emitter)} \tag{7–34}$$

Equation 7–34 shows that the input resistance in the CE configuration is approximately β times greater than that in the CB configuration. The quantity $(\beta + 1)r'_e$ is often designated as $r_\pi$ in texts and data sheets. It can also be shown that the output resistance of a transistor in its CE configuration is approximately β times *smaller* than it is in the CB configuration: $r_o \approx r_c/\beta$. Because the CE input resistance is β times greater and the output resistance is β times smaller than the corresponding values in the CB configuration, the common-emitter amplifier is inherently better suited for voltage amplification than its CB counterpart.

In a manner analogous to the CB model, the CE output resistance $r_o = r_c/\beta$ is the reciprocal of the slope of the curve for $I_{BQ}$ in the active region of the CE output characteristic, that is,

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_{BQ}}$$

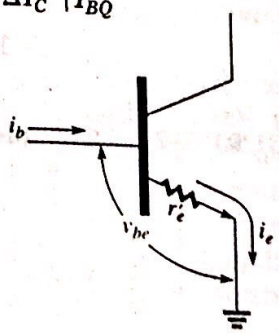


**FIGURE 7–24** The input circuit for a transistor in the CE configuration

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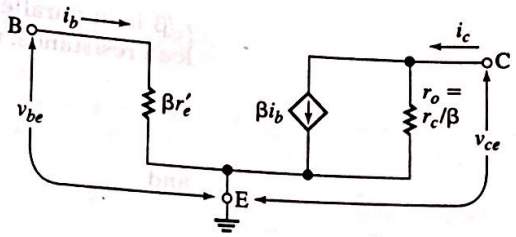



**FIGURE 7–25** Approximate small-signal model for a transistor in the common-emitter configuration

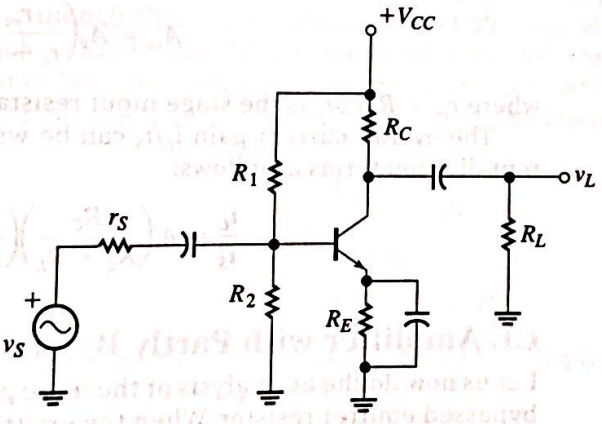
which can also be determined from

$$r_o = \frac{V_A + V_{CEQ}}{I_{CQ}} \tag{7–35}$$

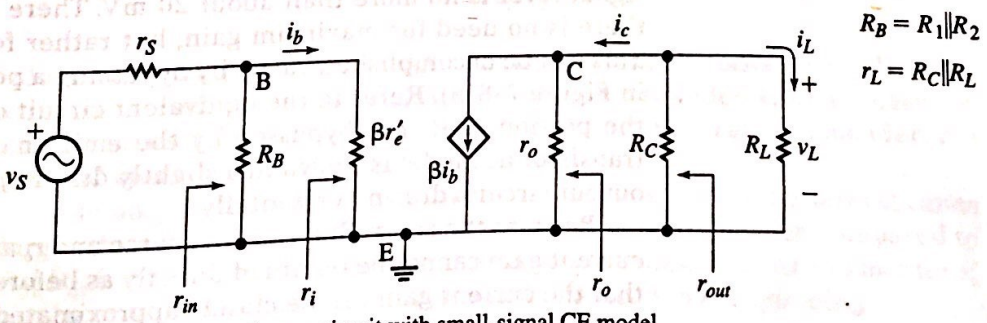
where $V_A$ is the transistor's Early voltage. For example, if $V_A = 80\,\text{V}$, $V_{CEQ} = 8\,\text{V}$, and $I_{CQ} = 2\,\text{mA}$, which can be fairly typical values, the resulting $r_o$ is 44 kΩ.

Figure 7–25 shows an approximate model for the common-emitter transistor. Note that the controlled current source has value $\beta i_b$, reflecting the fact that $i_c = \beta i_b$. Once again, we neglect the feedback effect, whereby the value of $i_b$ depends somewhat on $V_{CE}$.

Figure 7–26 shows a common-emitter amplifier stage with voltage-divider bias and its ac equivalent circuit. Note that the dc supply voltages are treated as ac short circuits, as before. In Figure 7–26(b), it can be seen that




(a) Complete CE amplifier




$R_B = R_1 \| R_2$

$r_L = R_C \| R_L$

(b) Equivalent ac circuit with small-signal CE model

**FIGURE 7–26** A common-emitter amplifier

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$r_c/\beta$ is in parallel with $R_C$, which implies that $r_{out} = r_o \| R_C$. Note also the ac load resistance, $r_L = R_C \| R_L$, defined in the figure. It is clear that

$$i_c = \frac{r_o}{r_o + r_L}(\beta i_b) \quad \text{(current division)}$$

and

$$A_i = \frac{i_c}{i_b} = \beta\left(\frac{r_o}{r_o + r_L}\right) \tag{7–36}$$

The input resistance in this case is clearly

$$r_i = \beta r'_e \tag{7–37}$$

Invoking the general form for the voltage gain in terms of $A_i$, namely $A_v = -A_i(R_L/r_i)$, we can write

$$A_v = -\beta\left(\frac{r_o}{r_o + r_L}\right)\frac{r_L}{\beta r'_e} \quad (r_L = R_C \| R_L \text{ is the total ac load resistance})$$

which can further be reduced to

$$A_v = \frac{-(r_L \| r_o)}{r'_e} \tag{7–38}$$

Note that if $r_o \gg r_L$, the current gain becomes $A_i \approx \beta$, and $A_v$ reduces to

$$A_v \approx \frac{-r_L}{r'_e} \qquad (r_o \gg r_L) \tag{7–39}$$

The overall gain, $A_{vs} = v_L/v_S$, can be written as

$$A_{vs} = A_v\left(\frac{r_{in}}{r_s + r_{in}}\right) \tag{7–40}$$

where $r_{in} = R_B \| \beta r'_e$ is the stage input resistance.

The overall current gain $i_L/i_S$ can be written in terms of $A_i$ and the current-division terms as follows:

$$\frac{i_L}{i_S} = A_i\left(\frac{R_C}{R_C + R_L}\right)\left(\frac{R_B}{r_{in} + R_B}\right) \tag{7–41}$$

## CE Amplifier with Partly Bypassed Emitter Resistance

Let us now do the ac analysis of the more general CE amplifier with a partly bypassed emitter resistor. When the emitter resistor is fully bypassed, maximum gain is obtained but at the cost of high distortion, unless the input signal level is no more than about 20 mV. There are also instances where there is no need for maximum gain, but rather for having a specific gain. This can be accomplished easily by bypassing a portion of $R_E$, as was shown in Figure 7–8(b). Refer to the equivalent circuit of Figure 7–27 where $R_f$ is the portion of $R_E$ not bypassed by the emitter capacitor. Notice that the transistor ac model is shown in a slightly different way with both input and output circuits drawn horizontally.

Because the controlled current source and $r_o$ are no longer grounded, the current gain cannot be obtained directly as before; however, it can be shown that the current gain can be closely approximated by the same expression:

$$A_i \approx \beta\left(\frac{r_o}{r_o + r_L}\right) \tag{7–42}$$

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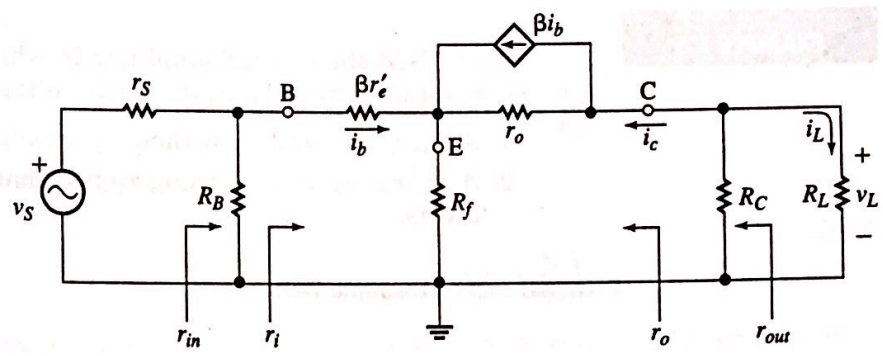


**FIGURE 7–27** Equivalent ac circuit of the CE amplifier with emitter resistance $R_f$

To obtain the input resistance looking into the base, we first write the equation of the input voltage at the base terminal as follows:

$$v_b = i_b\beta r'_e + (i_b + A_i i_b)R_f = i_b[\beta r'_e + (1 + A_i)R_f]$$

then solve for $v_b/i_b$, which is the input resistance $r_i$:

$$r_i = \beta r'_e + (1 + A_i)R_f \tag{7–43}$$

The voltage gain can now be expressed by means of the general form $-A_i(R_L/r_i)$ but using the total ac resistance $r_L$:

$$A_v = -A_i\frac{r_L}{r_i} \tag{7–44}$$

where $A_i$ and $r_i$ are given by equations 7–42 and 7–43. Notice, however, that the expression for $r_i$ contains also $A_i$, which in turn contains the term $r_o/(r_o + r_L)$. So even though these terms do not cancel algebraically, their effect on the expression closely cancel due to the fact that the $\beta r'_e$ term would be the smaller term in $r_i$. Therefore, with $A_i \gg 1$, it can easily be shown that the voltage gain, current gain, and input resistance can be approximated by the following:

$$A_v \approx \frac{-r_L}{r'_e + R_f} \tag{7–45}$$

$$A_i \approx \beta \tag{7–46}$$

$$r_i \approx \beta\,(r'_e + R_f) \tag{7–47}$$

The overall gain $A_{vs} = v_L/v_S$ is obtained by multiplying $A_v$ by the voltage-division fraction of the input circuit:

$$A_{vs} = \frac{-r_L}{r'_e + R_f}\left(\frac{r_{in}}{r_{in} + r_s}\right) \tag{7–48}$$

where $r_{in} = R_B \| \beta(r'_e + R_f)$ = stage input resistance. Notice that all these equations reduce to those derived for the grounded-emitter case by simply making $R_f = 0$. This is why this configuration can be considered a general case.

The output resistance ($r'_o$ in this case) can be shown to be several times larger than that for grounded emitter and can be ignored when compared to $R_C \| R_L$, further justifying the preceding approximations. An expression for $r'_o$ can be obtained by the methods described in Section 6–2, yielding

$$r'_o \approx r_o\left(1 + \frac{\beta R_f}{R_f + \beta r'_e + r_s \| R_B}\right) \tag{7–49}$$

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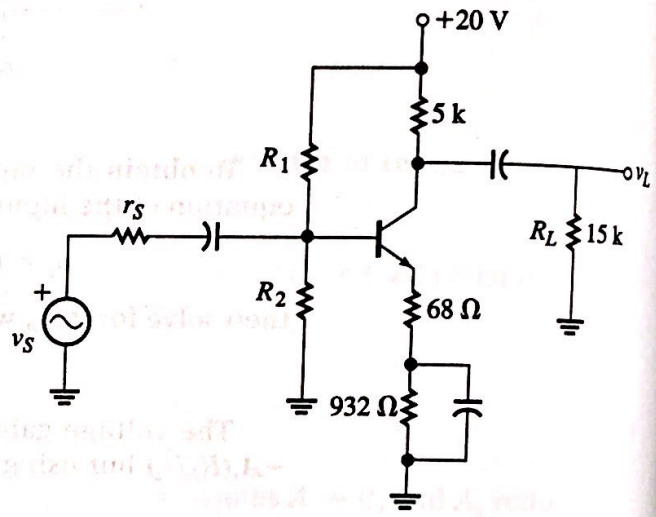
**EXAMPLE 7–5**

Figure 7–28 shows a CE amplifier in which $R_1 \| R_2 = 8\ \text{k}\Omega$. If the quiescent collector current is 2 mA, the Early voltage is 72 V, and $\beta = 150$, find

1. $A_i$, $r_i$, $r_{in}$, $A_v$, and $A_{vs}$ without approximations.
2. $A_i$, $r_i$, $r_{in}$, $A_v$, and $A_{vs}$ using approximate expressions. Determine percent errors.

**FIGURE 7–28** (Example 7–5)




**Solution**

Use equations 7–42 through 7–49.

1. The ac emitter resistance is $r'_e = 26\ \text{mV}/2\ \text{mA} = 13\ \Omega$.
   The quiescent C-E voltage is $V_{CEQ} = 20 - (2\ \text{mA})(5\ \text{k} + 1\ \text{k}) = 8\ \text{V}$ (KVL).
   The ac output resistance is $r_o = (72 + 8)/2\ \text{mA} = 40\ \text{k}\Omega$ (equation 7–35).
   The total ac load resistance is $r_L = 5\ \text{k} \| 15\ \text{k} = 3.75\ \text{k}\Omega$.
   Current gain is $A_i = 150(40\ \text{k}/43.75\ \text{k}) = 137.1$.
   Input resistance is $r_i = 150(13) + 138.1(68) = 11.34\ \text{k}\Omega$.
   Stage input resistance is $r_{in} = 11.34\ \text{k} \| 8\ \text{k} = 4.69\ \text{k}$.
   Voltage gain is $A_v = -137.1(3.75\ \text{k}/11.34\ \text{k}) = -45.34$.
   Overall voltage gain is $A_{vs} = -45.34(4.69\ \text{k}/5.69\ \text{k}) = -37.4$.
2. $A_i \approx \beta = 150$ (error = 9.4%)
   $r_i = 150(13 + 68) = 12.2\ \text{k}\Omega$ (error = 7.1%)
   $r_{in} = 8\ \text{k} \| 12.2\ \text{k} = 4.83\ \text{k}$ (error = 3%)
   $A_v = -(3.75\ \text{k})/(13 + 68) = -46.3$ (error = 2.1%)
   $A_{vs} = -46.3(4.83\ \text{k}/5.83\ \text{k}) = -38.4$ (error = 2.7%)

Notice that the most significant errors were those for $A_i$ and $r_i$ because they are moderately influenced by the output resistance $r_o$. The other errors are not significant from a practical standpoint.

In order to obtain a particular overall gain from a CE amplifier, we must determine a value for $R_f$ that will satisfy the requirement. Note that equation 7–48 includes $r_{in}$ in addition to $R_f$. But $r_{in}$ depends also on $R_f$. So in order to solve for $R_f$ relatively easily, we must derive an expression for the overall gain $A_{vs}$ in a more closed form. If we expand $r_{in} = R_B \| \beta(r'_e + R_f)$ as "product over sum" and substitute it into the term $r_{in}/(r_s + r_{in})$, we can obtain

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$$\frac{r_{in}}{r_s + r_{in}} = \frac{r'_e + R_f}{\frac{r_s}{\beta} + (r'_e + R_f)\left(1 + \frac{r_s}{R_B}\right)}$$

which after substituted into (7–48) yields

$$A_{vs} = \frac{-r_L}{\frac{r_s}{\beta} + (r'_e + R_f)\left(1 + \frac{r_s}{R_B}\right)} \tag{7–50}$$

As a verification, observe that the preceding expression reduces to $A_v$ if we make $r_s = 0$. Also notice that while not totally independent of β, as is the case for $A_v$, the overall gain, $A_{vs}$, is slightly influenced by β.

**EXAMPLE 7–6**

Change both $R_f$ and the bypassed emitter resistance in the previous example to establish an overall gain of −50 while maintaining the same dc bias conditions.

**Solution**

Solve for $R_f$ from equation 7–50:

$$R_f = \left(\frac{r_L}{|A_{vs}|} - \frac{r_s}{\beta}\right)\left(\frac{R_B}{r_s + R_B}\right) - r'_e$$

Substitute values to obtain $R_f = 47.7\ \Omega$ (47 Ω is a commercial value). In order to maintain the original $R_E$, the bypassed emitter resistance needs to be changed to 953 Ω.

*Helpful hint:* Try solving for $R_f$ by substituting the values directly into equation 7–50 and then using the calculator to extract the value of $R_f$ by "undoing" the equation's arithmetic. Do this without taking down any partial results. You will notice that with practice and confidence the answer can be obtained very quickly, with fewer chances of making "Math 101" errors. This is not to discourage you from practicing good math (a must in engineering), but just to illustrate another powerful use of your calculator.

We now turn again to the issue of obtaining maximum unclipped output voltage through proper location of the Q-point on the load line. Equation 7–18 is used for determining the optimum value of the collector current when the emitter is connected directly to ground. This equation can be modified for the general CE amplifier with fully or partly bypassed emitter resistance by an emitter capacitor. Basically, there are two resistive components in equation 7–18: The dc component, $R_C$, and the ac component, $r_L$. In the general CE amplifier circuit, however, there are two additional components: The emitter resistance, $R_E$, and the unbypassed ac resistance, $R_f$. A general expression for $I_{CQ}$ (optimum) can then be written as

$$I_{CQ}(\text{optimum}) = \frac{V_{CC}}{R_C + R_E + R_f + r_L} \tag{7–51}$$

Again, we say that this is a general expression because it can be used in all other instances: Emitter directly grounded ($R_E = 0, R_f = 0$), emitter resistor totally bypassed ($R_f = 0$), and emitter resistor without bypass capacitor ($R_f = R_E$). Note that the dc emitter resistor $R_E$ is the sum of $R_f$ and the bypassed resistor. An example illustrating these issues follows.

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**EXAMPLE 7–7**

Design a CE amplifier for a load resistance of 10 kΩ using $V_{CC}$ = 20 V and $R_C$ = 3.3 kΩ. Determine the optimum collector current for obtaining maximum output swing. The input source resistance is 600 ohms and the required overall gain is $A_{vs}$ = −45. Specify $R_E$, $R_1$, and $R_2$ so that the Q-point collector current will not change more than ±4% over a β range of 70 to 180.

**Solution**

In order to determine the optimum collector current, we need to know $R_E$ and $R_f$. $R_E$ is normally determined based on a voltage drop of about 10% of $V_{CC}$. But since $I_C$ is not known yet, we can assume that the drop across $R_C$ will be about 50% of $V_{CC}$. This would leave 40% of $V_{CC}$ for $V_{CE}$, which is consistent with the fact that the Q-point should be above the middle point of the dc load line (higher $I_C$, lower $V_{CE}$) for maximum output voltage swing. Therefore, $R_E$ needs to be about one-fifth of $R_C$, or 660 ohms. Note that with 10 volts across $R_C$, the collector current will be about 3 mA, according to Ohm's law.

We also need to estimate the value of $R_f$ based on the gain of −45. Here again we are faced with another unknown: $R_B = R_1 \| R_2$. However, since the magnitude of the gain from base to collector is approximately $r_L/(r'_e + R_f)$, we can calculate $R_f$ based on a magnitude of about 50, since the specified overall gain is −45. With $r_L$ = 3.3 k‖10 k = 2.5 k Ω and $r'_e$ about 8 ohms, we have $R_f$ = 2500/50 − 8 = 42 Ω. The optimum collector current according to equation 7–51 is then

$$I_{CQ}(\text{optimum}) = 20/(3.3\text{ k} + 660 + 2.5\text{ k} + 42) \approx 3.1\text{ mA}$$

With the ±4% allowed variation of collector current we establish $I_{Cmax}$ = 3.22 mA and $I_{Cmin}$ = 2.98 mA. Using equation 7–10, we determine

$$R_B/R_E = (3.22 - 2.98)/(2.98/70 - 3.22/180) = 9.7$$

and $R_B$ = 9.7 $R_E$ = 6.4 kΩ

From equation 7–9, $V_{Th} = I_C(R_E + R_B/\beta) + V_{BE}$ = 3.22(660+6.4 k/180) + 0.7 = 2.94 V.

From equation 7–12, $R_1$ = (20/2.94)6.4 k = 43.5 kΩ, from which $R_2$ = 7.5 kΩ follows.

Commercial values for $R_1$ and $R_2$ are 43 kΩ and 7.5 kΩ, respectively.

A more exact value for $R_f$ can now be calculated with equation 7–50 using a mid β-value of 120.

$$45 = \frac{2500}{\dfrac{600}{120} + (8 + R_f)\left(1 + \dfrac{600}{6400}\right)} \longrightarrow R_f = 38.2\ \Omega \ \ (39\ \Omega \text{ commercial}).$$

You can verify that by using the extreme values of β, the resulting value for $R_f$ does not change much. Now, because the sum of $R_f$ and the bypassed emitter resistance equals $R_E$, or 660 Ω, then the bypassed emitter resistance must be 621 Ω, or 620 Ω commercial. Exercise 7–15 at the end of the chapter verifies this design thoroughly.

## Small-Signal CC Amplifier Model

Figure 7–29(a) shows a common-collector amplifier and Figure 7–29(b) shows the corresponding small-signal equivalent circuit. Note that the collector in Figure 7–29(b) is shown grounded, since $V_{CC}$ in Figure 7–29(a) is connected directly to the collector and dc sources are once again treated as ac short circuits. Notice again that the transistor model was drawn slightly differently, with the three terminals clearly identified. Some authors refer to the CC transistor as a "grounded collector" configuration, which is correct in the ac sense.

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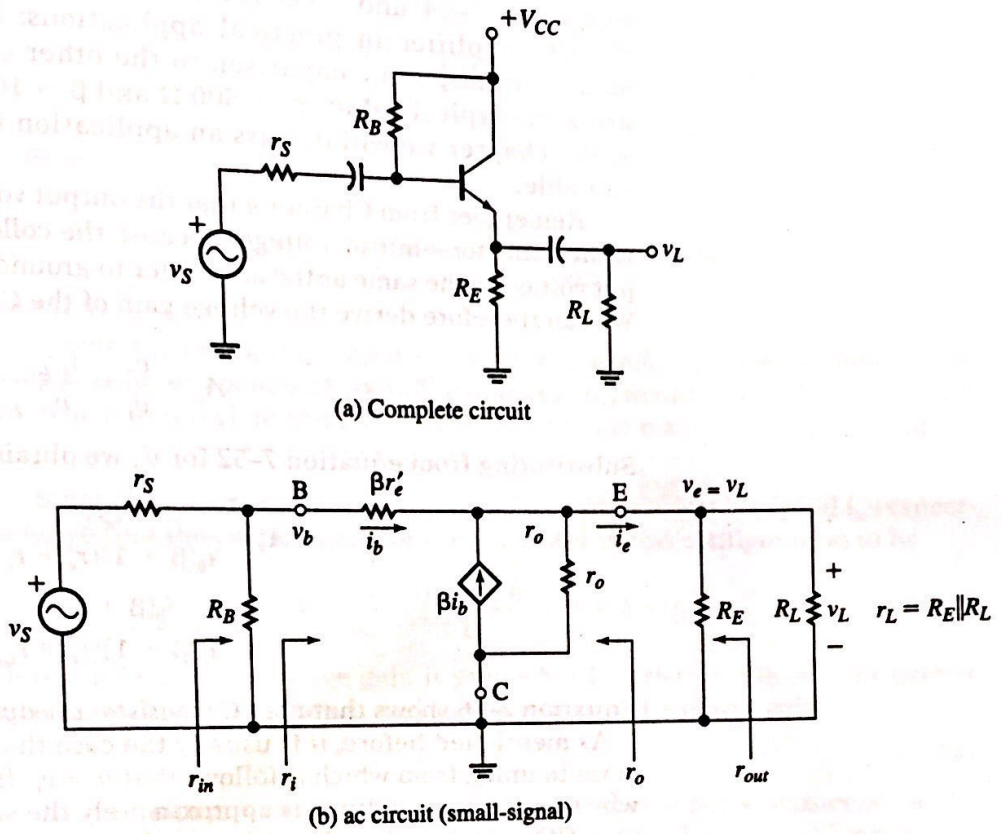


**FIGURE 7–29** A common-collector amplifier and its small-signal equivalent circuit

As in the CE model, the resistance between base and emitter is seen to be $\beta r'_e$, which is again an acceptable approximation for $r_\pi = (\beta + 1)r'_e$. The total input resistance at the base of the transistor (between base and ground) is derived as follows:

$$r_i = \frac{v_i}{i_i} = \frac{v_i}{i_b}$$

Remember that in a CC circuit $v_i$ *is the ac base-to-collector voltage, which the figure clearly shows is the same as the ac base-to-ground voltage.* The input current $i_i$ is the same as the base current $i_b$.

For purposes of this derivation, let us temporarily replace $\beta r'_e$ in Figure 7–29(b) by the more accurate value $(\beta + 1)r'_e$. Then, writing Kirchhoff's voltage law from B to ground in Figure 7–29(b), we obtain

$$\begin{aligned} v_i = v_b &= i_b(\beta + 1)r'_e + i_e r_L \\ &= i_b(\beta + 1)r'_e + i_b(\beta + 1)r_L \\ &\doteq i_b(\beta + 1)(r'_e + r_L) \end{aligned} \tag{7–52}$$

Solving for $v_b/i_b$ from (7–52), we obtain

$$\frac{v_b}{i_b} = r_i = (\beta + 1)(r'_e + r_L) \tag{7–53}$$

Again invoking the approximation $\beta + 1 \approx \beta$, we have

$$r_i \approx \beta(r'_e + r_L) \tag{7–54}$$

It is apparent from Figure 7–29(b) that

$$r_{in} = R_B \| r_i \tag{7–55}$$

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Equations 7–54 and 7–55 reveal the single most important feature of the CC amplifier in practical applications: Its input resistance can be made very large in comparison to the other configurations. For example, using the typical values $r_L = 500\ \Omega$ and $\beta = 100$, we have $r_i \approx 50\ \text{k}\Omega$. Later in the chapter we will discuss an application in which this feature is very valuable.

Remember from Chapter 4 that the output voltage in the CC configuration is the collector–emitter voltage. Because the collector is grounded, the ac output voltage is the same as the ac emitter-to-ground voltage (see Figure 7–29(b)). We can therefore derive the voltage gain of the CC transistor as follows:

$$A_v = \frac{v_o}{v_i} = \frac{i_e r_L}{v_i}$$

Substituting from equation 7–52 for $v_i$, we obtain

$$A_v = \frac{i_e r_L}{i_b(\beta + 1)(r'_e + r_L)}$$

$$= \frac{i_b(\beta + 1)r_L}{i_b(\beta + 1)(r'_e + r_L)} = \frac{r_L}{r'_e + r_L} \qquad (7\text{–}56)$$

Equation 7–56 shows that *the CC transistor always has a voltage gain less than 1.* As mentioned before, it is usually the case that $r_L \gg r'_e$, so the gain is very close to unity, from which it follows that $v_o \approx v_i$. It is not difficult to visualize why the ac output voltage is approximately the same as the ac input voltage in a CC configuration: The input and output are "separated" only by the small ac resistance of the forward-biased base–emitter junction. Note that there is no phase inversion between input and output. As the base-to-ground voltage increases, so does the emitter-to-ground voltage. Because the output voltage is essentially the same as the input voltage, in magnitude and phase, the emitter is said to *follow* the base. In that context, a transistor in the CC configuration is often called an *emitter follower* (more often, in fact, than it is called a *common-collector* circuit).

**EXAMPLE 7–8**

The common-collector amplifier in Figure 7–29(a) has $V_{CC} = 15\ \text{V}$, $R_B = 75\ \text{k}\Omega$, and $R_E = 910\ \Omega$. The $\beta$ of the silicon transistor is 100 and the load resistor is $600\ \Omega$. Find

1. $r_{in}$,
2. $A_v$.

**Solution**

1. From equations 4–28,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{15\ \text{V} - 0.7\ \text{V}}{75\ \text{k}\Omega + 101(910\ \Omega)} = 85.7\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(85.7\ \mu\text{A}) = 8.57\ \text{mA}$$

Then,

$$r'_e = \frac{0.026\ \text{V}}{I_E} = \frac{0.026\ \text{V}}{8.57\ \text{mA}} = 3.03\ \Omega$$

$$r_L = 910 \| 600 = 362\ \Omega$$

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From equation 7–56,

$$r_i = (\beta + 1)(r_e + r_L) = 101(3.03\ \Omega + 362\ \Omega) = 36.9\ \text{k}\Omega$$

$$r_{in} = R_B \| r_i = 36.9\ \text{k} \| 75\ \text{k} = 24.7\ \text{k}\Omega$$

2. From equation 7–56,

$$A_v = \frac{r_L}{r'_e + r_L} = \frac{362\ \Omega}{3.03\ \Omega + 362\ \Omega} = 0.992$$

Note that $A_v \approx 1$.

A note regarding the output swing: In this example, the maximum output swing is $2I_{EQ}r_L$ or about 6.2 V(p-p). The optimum $I_{EQ}$ would be $V_{CC}/(R_E + r_L) = 11.8$ mA, which would yield about 8.5 V(p-p) of available maximum output swing.

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Since the common-collector input and output currents are $i_b$ and $i_e$, respectively, we find the current gain for the transistor in this configuration to be

$$A_i = \frac{i_e}{i_b} = \frac{(\beta + 1)i_b}{i_b} = \beta + 1 \approx \beta \tag{7–57}$$

Thus, while the CC voltage gain is somewhat less than 1, the current gain is substantially greater than 1, and so, therefore, is the power gain:

$$A_p \approx A_v A_i \approx A_i \tag{7–58}$$

Rather than present a lengthy derivation for the output resistance of the CC transistor, let us make an intuitive observation, from which we can formulate a general rule for determining output resistance of CC amplifiers. We have already seen how the relationship $i_e = (\beta + 1)i_b$ leads to the result that the resistance looking into the base is $(\beta + 1)$ times greater than the total resistance from emitter to ground (equation 7–54). Conversely, that same relationship implies that resistance looking into the emitter is $(\beta + 1)$ times *smaller* than the resistance from the base back to the signal source. Now, the output resistance of the CC stage in Figure 7–29, $r_{out}$, is the resistance looking into the emitter in parallel with $R_E$. Therefore, applying the foregoing rule, we find

$$r_{out} = R_E \left\| \left( r'_e + \frac{R'_B}{\beta + 1} \right) \right. \tag{7–59}$$

where $R'_B$ is the resistance looking from the base toward the signal source. Figure 7–30 shows how $R'_B$ is defined in the ac equivalent of the base circuit. $R'_B$ is computed by shorting the signal source to ground, so

$$R'_B = R_B \| r_S \tag{7–60}$$

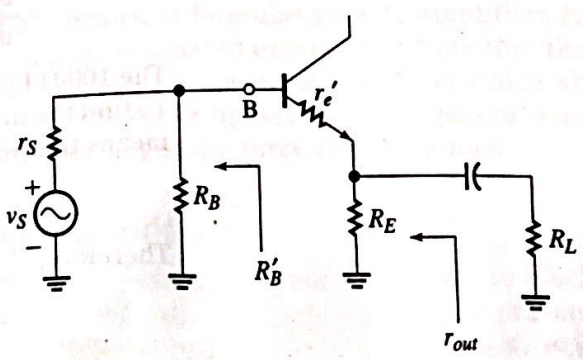


**FIGURE 7–30** $R'_B$ is the (Thévenin) equivalent resistance looking from the base toward the source. $R'_B = R_B \| r_s$

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and with $\beta + 1 \approx \beta$,

$$r_{out} \approx R_E \left\| \left( r'_e + \frac{R_B \| r_S}{\beta} \right) \right. \tag{7–61}$$

Equation 7–61 shows that the output resistance of an emitter follower can be quite small. For example, for the typical values $R_E = 1\ \text{k}\Omega$, $r'_e = 5\ \Omega$, $R_B = 100\ \text{k}\Omega$, $r_S = 50\ \Omega$, and $\beta = 100$, we find

$$r_{out} \approx 1\ \text{k} \left\| \left( 5 + \frac{100\ \text{k} \| 50}{100} \right) \right. \approx 5.5\ \Omega$$

When $r_S = 0$, notice that $R_B \| r_S = 0$ and the equation becomes

$$r_{out} \approx R_E \| r'_e \approx r'_e \quad (r_S = 0) \tag{7–62}$$

The overall voltage gain of the emitter-follower stage, taking source resistance into account, can be determined as follows:

$$A_{vs} = \frac{v_L}{v_S} = \frac{r_L}{r'_e + r_L} \left( \frac{r_{in}}{r_S + r_{in}} \right) \tag{7–63}$$

where $r_L = R_E \| R_L$. For small $r_S$, equation 7–63 is approximately equivalent to equation 7–56.

Although the emitter follower by itself has a voltage gain less than 1, it can be used to improve the voltage gain of a larger amplifier system. Because of its large input resistance, it does not "load" the output of another amplifier. In other words, the load presented by an emitter follower to another amplifier does not appreciably reduce the voltage gain of that amplifier. Also, because it has a small output resistance, the emitter follower can drive a "heavy" load (small resistance) whose presence would otherwise reduce voltage gain. For these reasons, an emitter follower is valuable as an intermediate stage between an amplifier and a load. When an emitter follower is used this way, it is called a *buffer* amplifier, or an *isolation* amplifier, because it effectively isolates another amplifier from the loading effect of $R_L$. This use is illustrated in the next example.

**EXAMPLE 7–9**

An amplifier having an output resistance of 1 kΩ is to drive a 100-Ω load, as shown in Figure 7–31(a). Assuming that the amplifier has a voltage gain of $A_v = 140$ (with no load connected), find

1. the voltage gain with the load connected, and
2. the voltage gain when an emitter follower is inserted between the amplifier and the load, as shown in Figure 7–31(b).

**Solution**

1. The voltage gain with the 100-Ω load connected is

$$\frac{v_L}{v_S} = A_v \left( \frac{R_L}{r_o + R_L} \right) = 140 \left( \frac{100}{1000 + 100} \right) = 12.7$$

The 100-Ω load severely reduces the voltage gain.

2. To find the input resistance of the emitter follower, we must find $r'_e$, which means that we must first find the dc bias current $I_E$:

$$I_E \approx \frac{V_{CC} - 0.7}{R_E + R_B/\beta} = 92\ \text{mA}$$

Therefore,

$$r'_e = \frac{26\ \text{mV}}{92\ \text{mA}} = 0.28\ \Omega$$

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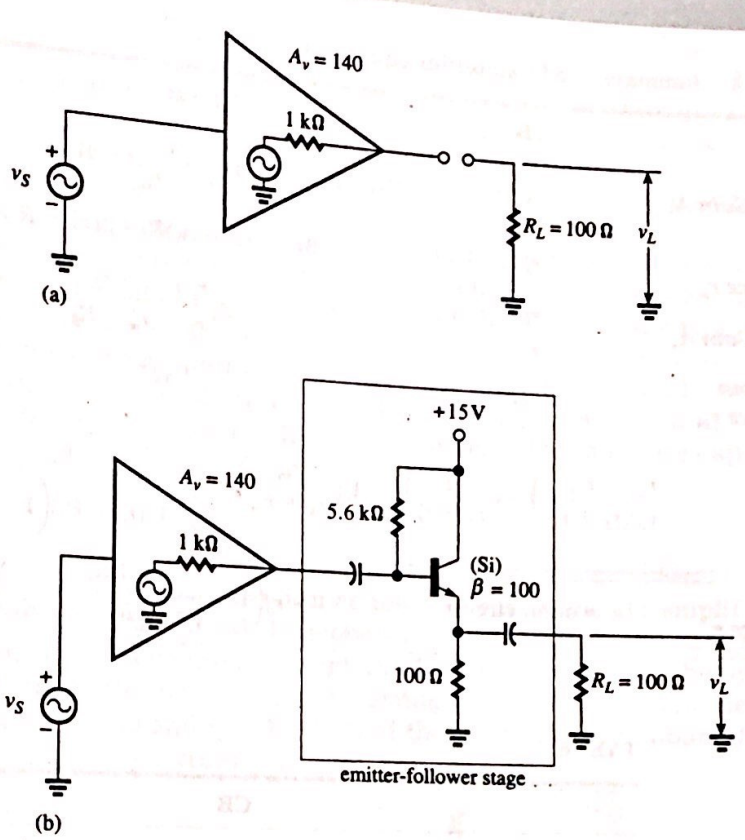
FIGURE 7–31 (Example 7–9)




The ac load resistance for the emitter follower is

$$r_L = R_E \| R_L = (100\ \Omega) \| (100\ \Omega) = 50\ \Omega$$

From equation 7–56,

$$r_{in} = 5.6\ \text{k} \| 100(0.28 + 50) = 2.65\ \text{k}\Omega$$

As far as the emitter follower is concerned, the source resistance is the output resistance (1 kΩ) of the amplifier driving it. Therefore, from equation 7–63, the overall gain of the emitter follower is

$$A_{vs} = \frac{50}{0.28 + 50}\left(\frac{2.65\ \text{k}}{1\ \text{k} + 2.65\ \text{k}}\right) = 0.726$$

The system gain from amplifier to load is then (0.726)(140) = 102. We see that insertion of the emitter follower improved the voltage gain from 12.7 to 102, an increase of 700%.

Table 7–1 is a summary of all important formulas for BJT amplifiers in the three configurations, including approximated expressions. Note that the common-emitter configuration is given as the general case from which all particular cases can be obtained. Table 7–2 compares, in a very general way, the important small-signal characteristics of the three configurations.

## Capacitively Coupled BJT Amplifiers

Recall that the primary reason for employing capacitor coupling is to block the flow of dc current. We have observed that it is often necessary to prevent the flow of dc current between the input of an amplifier and its signal source,

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**TABLE 7–1** Summary of BJT amplifier equations

| | CB | CE (general) | CC |
|---|---|---|---|
| ***Current Gain*** $A_i$ | $\alpha$ | $\beta\left(\frac{r_o}{r_o + r_L}\right) \approx \beta$ | $(\beta + 1)\frac{r_o}{r_o + r_L} \approx \beta$ |
| ***Input Resistance*** $r_i$ | $r'_e$ | $\beta r'_e + (1 + A_i)R_f \approx \beta(r'_e + R_f)$ | $\beta r'_e + (1 + A_i)r_L \approx \beta(r'_e + r_L)$ |
| ***Voltage Gain*** $A_v$ | $\frac{r_L}{r'_e}$ | $-A_i\frac{r_L}{r_i} \approx \frac{-r_L}{r'_e + R_f}$ | $\frac{r_L}{r'_e + r_L} \approx 1$ |
| ***Stage Input Resistance*** $r_{in}$ | $R_E \parallel r_i$ | $R_B \parallel r_i$ | $R_B \parallel r_i$ |
| ***Overall Voltage Gain*** $A_{vs}$ | $\frac{r_L}{r'_e}\left(\frac{r_{in}}{r_S + r_{in}}\right) \approx \left(\frac{r'_L}{r_S + r'_e}\right)$ | $A_v\left(\frac{r_{in}}{r_S + r_{in}}\right) \approx \frac{-r_L}{\frac{r_S}{\beta} + (r'_e + R_f)\left(1 + \frac{r_s}{R_B}\right)}$ | $A_v\left(\frac{r_{in}}{r_S + r_{in}}\right) \approx \frac{r_{in}}{r_S + r_{in}}$ |
| ***Output Resistance*** $r_o$ | $r_c \approx$ open circuit | $\approx r_o\left(1 + \frac{\beta R_f}{\beta r'_e + R_f + r_S \parallel R_B}\right)$ | $r'_e + \frac{r_S \parallel R_B}{\beta + 1} \approx r'_e + \frac{r_S \parallel R_B}{\beta}$ |

**TABLE 7–2**

| | CB | CE | CC |
|---|---|---|---|
| ***Voltage Gain*** | Large (noninverting) | Large (inverting) | ≈ 1 (noninverting) |
| ***Current Gain*** | ≈ 1 | Large | Large |
| ***Power Gain*** | Moderate | Large | Small |
| ***Input Resistance*** | Low | Moderate | High |
| ***Output Resistance*** | High | Moderate | Low |

as well as between the amplifier's output and its load. Similarly, capacitor coupling is used to prevent dc current from flowing between the output of one amplifier stage and the input of the next stage. The capacitor connected in the path between amplifier stages makes it possible to have a dc bias voltage at the output of one stage that is different from the dc bias voltage at the input to the next stage. This idea is illustrated in Figure 7–32, which shows the output of a BJT amplifier stage connected through a coupling capacitor

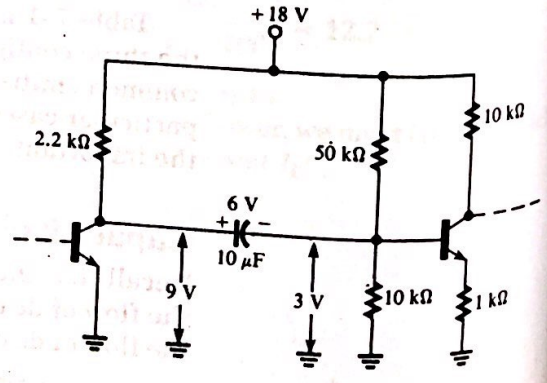


**FIGURE 7–32** The capacitor used in the capacitor coupling method makes it possible to have different bias voltages on the amplifier stages. Note that the (electrolytic) capacitor has 6 V dc across it and has its positive lead connected to the more positive bias (9 V).

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to the input of another BJT amplifier stage. Notice that the collector of the first stage is at +9 V and that the base of the second stage is at +3 V. The dc voltage across the capacitor is therefore 9 − 3 = 6 V, so the capacitor should have a dc-working-voltage (DCWV) rating somewhat greater than 6 V. If the 10-μF coupling capacitor is of the electrolytic type, it *must* be connected with its positive terminal to the more positive bias voltage: the 9-V collector voltage in this example.

Of course, a coupling capacitor permits the flow of *ac* signal current between stages, provided the frequency is high enough to keep the capacitive reactance small. The disadvantage of the RC coupling method is that it affects the low-frequency response of the amplifier; we must sometimes choose between an impractically large capacitor value and an unreasonably large lower cutoff frequency. RC coupling is not used in integrated circuits because it is difficult and uneconomical to fabricate capacitors on a chip.

**EXAMPLE 7–10**

Figure 7–33 shows two capacitor-coupled, common-emitter amplifier stages. Notice that the ac signal developed at the output of the first stage (the collector of $Q_1$) is coupled through the 0.85-μF capacitor to the input of the second stage (the base of $Q_2$). Assuming that the transistors are identical and have $\beta = 100$ and $r_c = 1\ \text{M}\Omega$, find the small signal, midband (1) voltage gain $v_L/v_S$ and (2) current gain $i_L/i_S$.

**Solution**

We will use the common-emitter, small-signal relations that are summarized in Table 7–1.

1. The collector current for $Q_1$ is $I_{C1} = \beta\left(\dfrac{V_{CC} - V_{BE}}{R_B}\right) = 1.82\ \text{mA}$ and $r'_{e1} = \dfrac{26\ \text{mV}}{1.82\ \text{mA}} = 14.3\ \Omega$. The collector current for $Q_2$ is found using Thévenin's theorem: $V_{Th} = 12(10/78) = 1.54\ \text{V}$, $R_B = 10 \| 68 = 8.72\ \text{k}\Omega$, and $I_C = (1.54 - 0.7)/(220 + 8.72\ \text{k}/100) = 2.73\ \text{mA}$, yielding $r'_{e2} = 9.5\ \Omega$.

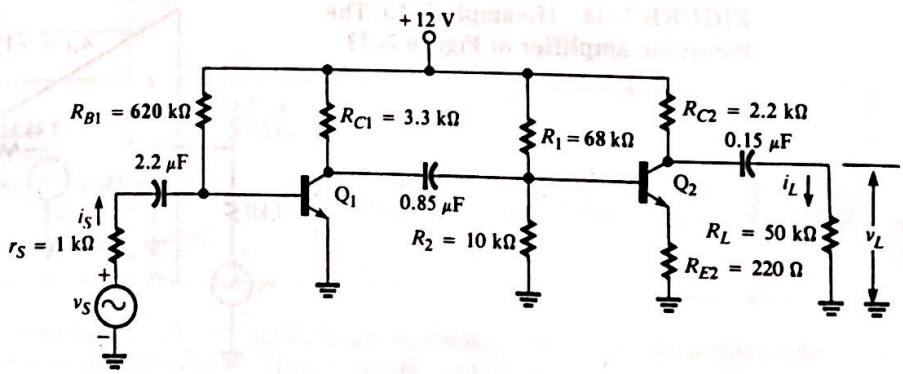
The input resistance to the first stage is

$$r_{in1} = R_{B1} \| \beta r'_e = (620\ \text{k}\Omega) \| (1.43\ \text{k}\Omega) \approx 1.43\ \text{k}\Omega$$

The output resistance of stage 1 (at the collector of $Q_1$) is

$$r_{out1} = R_{C1} \| (r_c/\beta) = (3.3\ \text{k}\Omega) \| [(1\ \text{M}\Omega)/100] = 2.48\ \text{k}\Omega$$

FIGURE 7–33 (Example 7–10)

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The *unloaded* voltage gain of stage 1 is, therefore,

$$A_{v1} = \frac{-r_{out1}}{r'_e} = \frac{-2.48\ \text{k}\Omega}{14.3\ \Omega} = -173.4$$

The input resistance to the second stage is

$$\begin{aligned} r_{in2} &= R_1 \| R_2 \| \beta(r'_e + R_{E2}) \\ &= (68\ \text{k}\Omega) \| (10\ \text{k}\Omega) \| 100[(9.5\ \Omega) + (220\ \Omega)] \\ &= (8.72\ \text{k}\Omega) \| (23\ \text{k}\Omega) = 6.32\ \text{k}\Omega \end{aligned}$$

The output resistance of stage 2 is

$$r_{out2} = R_{C2} \| (r_c/\beta) = (2.2\ \text{k}\Omega) \| (1\ \text{M}\Omega/100) = 1.8\ \text{k}\Omega$$

The *unloaded* voltage gain of stage 2 is, therefore,

$$A_{v2} = \frac{-r_{out2}}{R_{E2} + r'_e} = \frac{-1.8\ \text{k}\Omega}{(220\ \Omega) + (9.5\ \Omega)} = -7.84$$

The two-stage amplifier can now be represented as shown in Figure 7–34. No capacitors are shown in this figure because we are assuming operation in the midband frequency range. Using (the two-stage form of) equation 7–61, we find

$$\frac{v_L}{v_S} = \left[\frac{1.43\ \text{k}\Omega}{(1\ \text{k}\Omega) + (1.43\ \text{k}\Omega)}\right](-173.4)\left[\frac{6.32\ \text{k}\Omega}{(2.48\ \text{k}\Omega) + (6.32\ \text{k}\Omega)}\right](-7.84) \times \left[\frac{50\ \text{k}\Omega}{(1.8\ \text{k}\Omega) + (50\ \text{k}\Omega)}\right] = 554$$

The positive result shows that $v_L$ is in phase with $v_S$.

Notice that an alternative approach to finding the overall voltage gain is to find the voltage gains $A_1$ and $A_2$ *with loads connected.* Taking this approach, we compute the ac load resistance $r_L$ of each stage:

$$r_{L1} = r_{out1} \| r_{in2} = (2.48\ \text{k}\Omega) \| (6.32\ \text{k}\Omega) = 1.78\ \text{k}\Omega$$

$$r_{L2} = r_{out2} \| R_L = (1.8\ \text{k}\Omega) \| (50\ \text{k}\Omega) = 1.74\ \text{k}\Omega$$

The voltage gains with these loads connected are then

$$A_1 \approx \frac{-r_{L1}}{r'_{e1}} = \frac{-1.78\ \text{k}\Omega}{14.3\ \Omega} = -124.5$$

$$A_2 \approx \frac{-r_{L2}}{r'_{e2} + R_{E2}} = \frac{-1.74\ \text{k}\Omega}{(9.5\ \Omega) + (220\ \Omega)} = -7.58$$

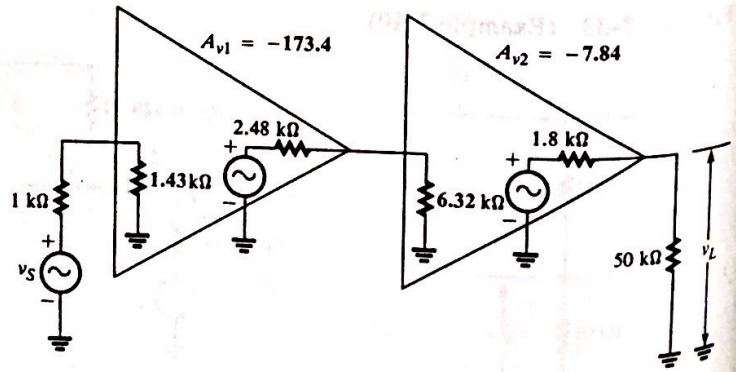


**FIGURE 7–34** (Example 7–10) The two-stage amplifier of Figure 7–33

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The overall voltage gain is then

$$\frac{v_L}{v_S} = \left[\frac{r_{in1}}{r_{in1} + r_S}\right] A_1 A_2 = \left[\frac{1.43\ \text{k}\Omega}{(1.43\ \text{k}\Omega) + (1\ \text{k}\Omega)}\right](-124.5)(-7.58) = 555$$

Except for a small rounding error, this approach produces the same result as before.

2. To determine the overall current gain, it is helpful to draw the small-signal equivalent circuit of each stage and then trace the flow of ac current through the amplifier. We will use the current-divider rule at each node to determine the portion of signal current that continues to flow toward the load. Figure 7–35 shows the small-signal equivalent of the first stage. Applying the current-divider rule to the input side of stage 1 in Figure 7–35, we obtain

$$i_{b1} = \left[\frac{620\ \text{k}\Omega}{1.43\ \text{k}\Omega + 620\ \text{k}\Omega}\right] i_S = 0.9977 i_S$$

This result shows that essentially all of the source current enters the base of $Q_1$ (0.0023 $i_S$ is shunted to ground through $R_B$). At the output side of stage 1, we have

$$i_{c1} = \beta i_{b1} = 100 i_{b1} = 100(0.9977 i_S) = 99.77 i_S$$

To find the portion of $\beta i_{b1}$ that flows into the base of $Q_2$, we must consider all the parallel paths to ground in the interstage circuitry between $Q_1$ and $Q_2$. Figure 7–36 shows the equivalent circuit of the second stage and the output side of the first stage. Note that $r_{out1}$ is the parallel combination of $r_c/\beta$ and $R_{C1}$, and this combination is in parallel with the bias resistors $R_1$ and $R_2$ at the input to the second stage. The total equivalent resistance $r_{SH}$ shunting the input (base) of $Q_2$ is, therefore,

$$r_{SH} = r_{out1} \| R_1 \| R_2 = (2.48\ \text{k}\Omega) \| (68\ \text{k}\Omega) \| (10\ \text{k}\Omega) = 1.93\ \text{k}\Omega$$

The current $i_{b2}$ into the base of $Q_2$ is then found by the current-divider rule:

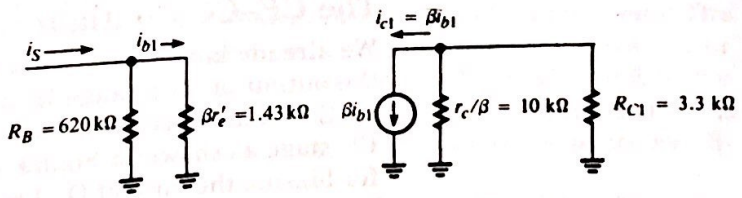


**FIGURE 7–35** (Example 7–10) The small-signal equivalent circuit for the first stage of the amplifier in Figure 7–33. This circuit is used to compute the current $i_{b1}$ in terms of $i_S$.

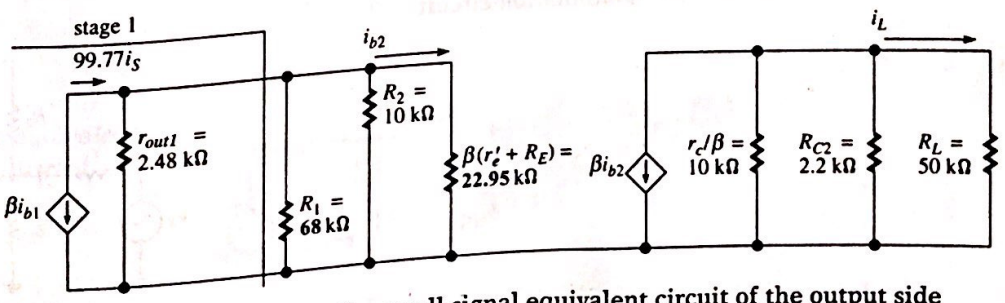


**FIGURE 7–36** (Example 7–10) The small-signal equivalent circuit of the output side of stage 1 joined to amplifier stage 2. This circuit is used to find $i_L$ in terms of $i_S$.

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$$i_{b2} = -99.77 i_S \left[ \frac{r_{SH}}{r_{SH} + \beta(r_e' + R_E)} \right]$$
$$= -99.77 i_S \left[ \frac{1.93\ \text{k}\Omega}{(1.93\ \text{k}\Omega) + (22.95\ \text{k}\Omega)} \right] = -7.74 i_S$$

Notice that a significant portion of signal current is lost in the interstage circuitry due to the shunt paths to ground: Less than $\frac{1}{10}$ of $i_{c1}$ reaches the base of $Q_2$. Now,

$$i_{c2} = \beta i_{b2} = 100(-7.74 i_S) = -774 i_S$$

The parallel combination of $r_c/\beta$ and $R_{C2}$ shunts $R_L$, so one more application of the current-divider rule gives

$$i_L = -\left[ \frac{(r_c/\beta) \parallel R_{C2}}{R_L + (r_c/\beta) \parallel R_{C2}} \right] \beta i_{b2} = -\left[ \frac{(10\ \text{k}\Omega) \parallel (2.2\ \text{k}\Omega)}{(50\ \text{k}\Omega) + (10\ \text{k}\Omega) \parallel (2.2\ \text{k}\Omega)} \right] (-774 i_S)$$
$$= 26.94 i_S$$

Therefore, the current gain from source to load is

$$\frac{i_L}{i_S} = 26.94$$

## 7–4 DIRECT COUPLING

We now examine *direct coupling,* the coupling method in which the output of one stage is electrically connected directly to the input of the next stage. In other words, both the dc and ac voltages at the output of one stage are identical to those at the input of the next stage. The method is often referred to as *dc,* which, in the context of signal coupling, means both direct coupling and direct current. Clearly, any change in the dc voltage at the output of one stage produces an identical change in dc voltage at the input to the next stage, so a direct-coupled amplifier behaves like a direct-current amplifier. Direct coupling is used in differential and operational amplifiers, which we will study extensively in Chapter 17, and in integrated circuits. Two practical configurations that employ direct coupling are introduced next.

### The CE–CC Configuration

We already know that a CC stage is used for driving low-resistance loads. If the output of a CE stage is to be used with a relatively low load resistance, a CC should be used as a buffer. The CC stage can be directly coupled to the CE stage as shown in Figure 7–37. The collector resistance of $Q_1$ also serves for biasing the base of $Q_2$. Let us perform a dc analysis of the circuit.

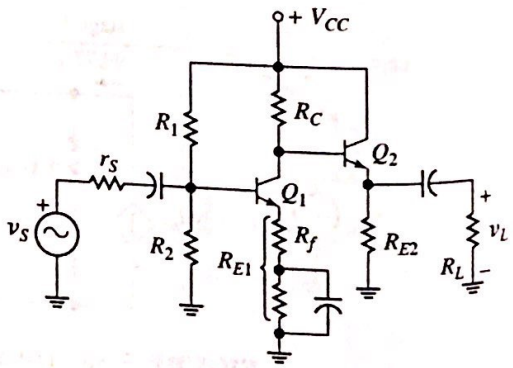


**FIGURE 7–37** The CE–CC combination circuit

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As we know, the collector current of $Q_1$ is

$$I_{C1} \approx \frac{V_{Th} - V_{BE}}{R_{E1} + R_B/\beta_1}$$

where $V_{Th} = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right)$ and $R_B = R_1 \| R_2$

The emitter current of $Q_2$ is

$$I_{E2} = \frac{V_{B2} - V_{BE}}{R_{E2}} = \frac{V_{CC} - (I_{C1} + I_{B2})R_C - V_{BE}}{R_{E2}}$$

Substituting $I_{B2} = \frac{I_{E2}}{\beta_2 + 1}$ and reducing we obtain

$$I_{E2} \approx \frac{V_{CC} - V_{BE} - I_{C1}R_C}{R_{E2} + R_C/\beta_2} \tag{7–64}$$

To analyze the circuit in ac, we first draw the corresponding ac-equivalent circuit as shown in Figure 7–38. The overall gain $v_L/v_S$ can be expressed as the product of the in-circuit gains of both stages, that is, considering the input resistance of the CC stage as part of the load resistance of the CE stage. Using the equations from Table 7–1 we can write

$$\frac{v_L}{v_S} = \frac{-r_{L1}}{\frac{r_S}{\beta_1} + (r'_{e1} + R_f)\left(1 + \frac{r_S}{R_B}\right)}\left(\frac{r_{L2}}{r'_{e2} + r_{L2}}\right) \tag{7–65}$$

where

$$r_{L1} = R_C \| [\beta_2(r'_{e2} + r_{L2})]$$

and

$$r_{L2} = R_{E2} \| R_L$$

## The Darlington Pair

When the collectors of two BJTs are tied together and the emitter of one is direct-coupled to the base of the other, as shown in Figure 7–39, we obtain an important and highly useful configuration called a *Darlington pair.* The combination is used in amplifier circuits as if it were a single transistor having the base, collector, and emitter terminals labeled B, C, and E in the figure. We will analyze the Darlington pair to discover the effective beta ($\beta_{DP}$) of the single transistor it represents, as well as some of its small-signal characteristics.

Let $\beta_1$ and $\beta_2$ be the dc β-values of $Q_1$ and $Q_2$, respectively. Then, by definition,

$$I_{C1} = \beta_1 I_{B1} \quad \text{and} \quad I_{E1} = (\beta_1 + 1)I_{B1}$$

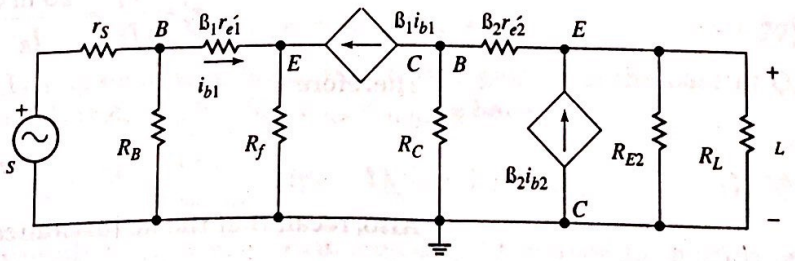


FIGURE 7–38 The ac-equivalent circuit of a CE-CC amplifier

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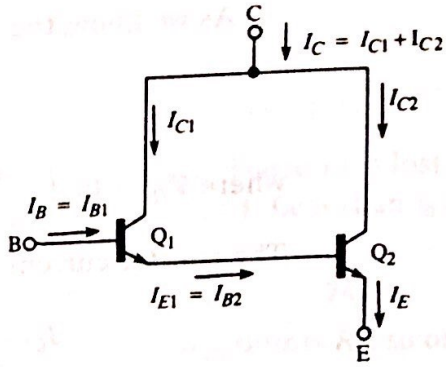


**FIGURE 7–39** The Darlington pair is used as a single transistor having the collector, base, and emitter terminals labeled C, B, and E

But $I_{E1} = I_{B2}$, so

$$I_{C2} = \beta_2 I_{B2} = \beta_2(\beta_1 + 1)I_{B1}$$

Now,

$$I_C = I_{C1} + I_{C2} = \beta_1 I_{B1} + \beta_2(\beta_1 + 1)I_{B1} = [\beta_1\beta_2 + (\beta_1 + \beta_2)]I_{B1}$$

Since $I_{B1} = I_B$, we have $I_C = [\beta_1\beta_2 + (\beta_1 + \beta_2)]I_B$, or

$$\beta_{DP} = I_C/I_B = \beta_1\beta_2 + \beta_1 + \beta_2 \tag{7–66}$$

Equation 7–66 shows that the effective β of the Darlington pair is the product plus the sum of the βs of the individual transistors. It is usually true that $\beta_1\beta_2 \gg \beta_1 + \beta_2$, so

$$\beta_{DP} = \beta_1\beta_2 + \beta_1 + \beta_2 \approx \beta_1\beta_2 \tag{7–67}$$

Darlington pairs are often fabricated on a single chip to achieve matched $Q_1$ and $Q_2$ characteristics. When $\beta_1 = \beta_2 = \beta$, we have an effective β of

$$\beta_{DP} = \beta^2 + 2\beta \approx \beta^2 \tag{7–68}$$

For example, if $\beta_1 = \beta_2 = 100$, then $\beta_{DP} = 10{,}000 + 200 \approx 10{,}000$. We see that the Darlington pair can be regarded as a "super-β" transistor, and therefore enjoys all the advantages that high-β transistors have.

While the foregoing analysis was performed for dc currents and the dc β-values, an identical small-signal analysis shows that the small-signal value of $\beta_{DP}$ is the product plus the sum of the small-signal values of $\beta_1$ and $\beta_2$. Hereafter we will make the usual assumption that the dc and small-signal values of β are approximately equal and will not distinguish between the two.

We wish now to determine the effective small-signal input resistance from B to E, $r_{i(DP)}$, and the emitter resistance $r'_{e(DP)}$, of the composite transistor. Recall the general relationship (equation 7–22):

$$r'_e \approx \frac{V_T}{I_E} \approx \frac{26\text{ mV}}{I_E} \quad \text{(at room temperature)}$$

Therefore

$$r'_{e2} = \frac{26\text{ mV}}{I_{E2}} \tag{7–69}$$

Also, recall that the ac resistance looking into the base of $Q_2$, $r_{i2}$, is

$$r_{i2} \approx \beta_2 r'_{e2} \tag{7–70}$$

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Now

$$r'_{e1} \approx \frac{26\text{ mV}}{I_{E1}} \tag{7–71}$$

Since $I_{E2} \approx \beta_2 I_{B2} = \beta_2 I_{E1}$, we have

$$I_{E1} \approx \frac{I_{E2}}{\beta_2} \tag{7–72}$$

Substituting (7–72) into (7–71) gives

$$r'_{e1} \approx \beta_2\left(\frac{26\text{ mV}}{I_{E2}}\right) = \beta_2 r'_{e2} \tag{7–73}$$

The total effective resistance looking into the base of $Q_1$ (across the composite B–E terminals), i.e., the effective small-signal input resistance of the Darlington pair, is

$$r_{i(DP)} = \beta_1(r'_{e1} + r_{i2}) \approx \beta_1(r'_{e1} + \beta_2 r'_{e2}) \tag{7–74}$$

Substituting from equation 7–73, we have

$$r_{i(DP)} \approx \beta_1(\beta_2 r'_{e2} + \beta_2 r'_{e2}) = 2\beta_1\beta_2 r'_{e2} \tag{7–75}$$

Since $\beta_{DP} \approx \beta_1\beta_2$, the effective emitter resistance $r'_{e(DP)}$, is

$$r'_{e(DP)} \approx \frac{r_{in(DP)}}{\beta_{DP}} = \frac{2\beta_1\beta_2 r'_{e2}}{\beta_1\beta_2} = 2r'_{e2} \tag{7–76}$$

**EXAMPLE 7–11**

A Darlington pair is biased so that the total collector current is 2 mA. If $\beta_1 = 110$ and $\beta_2 = 100$, find the room-temperature values of (1) $\beta_{DP}$, (2) $r_{i(DP)}$, and (3) $r'_{e(DP)}$.

**Solution**

1. $\beta_{DP} = \beta_1\beta_2 + \beta_1 + \beta_2 = (110)(100) + 110 + 100 = 11{,}210$
2. From equation 7–69,

$$r'_{e2} \approx \frac{0.026}{2 \times 10^{-3}} = 13\ \Omega$$

From equation 7–75, $r_{i(DP)} \approx 2(110)(100)13 = 286\text{ k}\Omega$.

3. From equation 7–76, $r'_{e(DP)} \approx 2(13) = 26\ \Omega$.

This example shows that the Darlington pair can be used to obtain a significant increase in base-to-emitter input resistance compared to that obtainable from a conventional BJT: 286 kΩ versus 1.3 kΩ.

The Darlington pair is most often used in an emitter-follower configuration because of the excellent buffering it provides between a high-impedance source and a low-impedance load. With an ac load resistance $r_L$ connected to the emitter, the total input resistance to the follower is

$$r_i = r_{i(DP)} + \beta_{DP} r_L = \beta_{DP}(r'_{e(DP)} + r_L) \tag{7–77}$$

When operated as an emitter follower, the current gain from the base of $Q_1$ to the emitter of $Q_2$ is $A_i = i_{e2}/i_{b1}$. Since $i_{e1} = i_{b2}$, we have

$$A_i = \frac{i_{e2}}{i_{b1}} = \left(\frac{i_{e2}}{i_{b2}}\right)\frac{i_{e1}}{i_{b1}} = (\beta_1 + 1)(\beta_2 + 1) \approx \beta_1\beta_2 \tag{7–78}$$

The next example illustrates an extreme case of the need for buffering, where the source resistance is 5 kΩ and the load resistance is 100 Ω.

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**EXAMPLE 7–12**

Figure 7–40 shows a common-emitter stage driving a Darlington pair connected as an emitter follower. The β-values for the silicon transistors are $\beta_1 = 200$, $\beta_2 = 100$, and $\beta_3 = 100$.

1. Find $v_L/v_S$.
2. Find $v_L/v_S$ if the Darlington pair is removed and the 100-Ω load is capacitor-coupled to the collector of $Q_1$.

**Solution**

1. $$V_{Th} \approx \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} = \left[\frac{10\text{ k}\Omega}{(47\text{ k}\Omega) + (10\text{ k}\Omega)}\right](15\text{ V}) = 2.6\text{ V}$$

$$R_B = 10\text{ k} \| 47\text{ k} = 8.25\text{ k}$$

$$I_{C1} \approx I_{E1} \approx \frac{2.6 - 0.7}{978 + \dfrac{8.25\text{ k}}{200}} \approx 1.9\text{ mA}$$

$$r'_{e1} \approx \frac{26\text{ mV}}{I_{E1}} = \frac{26\text{ mV}}{1.9\text{ mA}} = 13.7\ \Omega$$

$$r_{in} = R_B \| \beta_1(r'_{e1} + R_f) = (8.25\text{ k}\Omega) \| 200(13.7 + 68) = 5.48\text{ k}\Omega$$

Notice that the collector of $Q_1$ is direct-coupled to the base of $Q_2$ in the Darlington pair, so

$$V_{B2} = V_{C1} \approx V_{CC} - I_{C1}R_{C1} = 15\text{ V} - (1.9\text{ mA})(3.3\text{ k}\Omega) = 8.7\text{ V}$$

The dc emitter voltage of $Q_3$ is about 1.4 V less than the base voltage of $Q_2$, since there are *two* forward-biased base-emitter junctions between those two points:

$$V_{E3} = V_{B2} - 1.4 = 8.7 - 1.4 = 7.3\text{ V}$$

$$I_{E3} = \frac{V_{E3}}{R_{E3}} = \frac{7.3\text{ V}}{47\ \Omega} = 155\text{ mA}$$

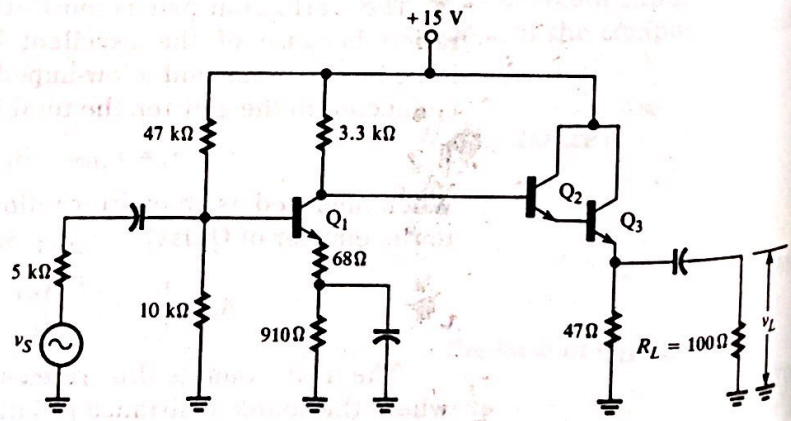
Noting that $Q_1$ and $Q_2$ in our previous analysis of the Darlington pair are now designated $Q_2$ and $Q_3$, we have, from equation 7–69,

$$r'_{e3} = \frac{26\text{ mV}}{.155\text{ mA}} = 0.17\ \Omega$$

From equation 7–76,

$$r'_{e(DP)} \approx 2(0.17\ \Omega) = 0.34\ \Omega$$

**FIGURE 7–40** (Example 7–12)

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From equation 7–68,

$$\beta_{DP} = (100)^2 + 200 = 10{,}200$$

From equation 7–77, the total resistance looking into the Darlington pair, with load connected, is

$$r_i = 10{,}200(0.34 + 47 \| 100) = 330\ \text{k}\Omega$$

This value of input resistance is so large in comparison to the 3.3-kΩ collector resistance of $Q_1$ that virtually no loading occurs. Thus,

$$A_{v1} \approx \frac{-R_{C1}}{r'_{e1} + R_f} = \frac{-3.3\ \text{k}\Omega}{81.7\ \Omega} = -40.4$$

The voltage gain of the emitter-follower stage is (from equation 7–56)

$$A_{v(DP)} \approx \frac{r_L}{r'_{e(DP)} + r_L} = \frac{32}{0.34 + 32} \approx 0.99$$

Taking into account the gain drop caused by $r_S$, the overall voltage gain is

$$\frac{v_L}{v_S} = \left[\frac{r_{in}}{r_S + r_{in}}\right] A_{v1}A_{v(DP)}$$

$$= \left[\frac{5.48\ \text{k}\Omega}{(5\ \text{k}\Omega) + (5.48\ \text{k}\Omega)}\right](-40.4)(0.99) = -20.9$$

2. With the 100-Ω load connected to the collector of $Q_1$, the ac load on $Q_1$ is $r_{L1} = (3.3\ \text{k}\Omega) \| (100\ \Omega) \approx 97\ \Omega$. Therefore,

$$A_{v1} \approx \frac{-r_{L1}}{r'_{e1} + R_f} = \frac{-97}{81.7} = -1.2$$

The overall gain is then

$$\frac{v_L}{v_S} = \left[\frac{5.48\ \text{k}\Omega}{(5\ \text{k}\Omega) + (5.48\ \text{k}\Omega)}\right](-1.2) = -0.63$$

Without the buffering provided by the Darlington pair, the overall voltage gain turns out to be much less than the original value, not to mention the severe reduction of available output swing.

## 7–5 OTHER SMALL-SIGNAL MODELS

### Transconductance

We have seen that one of the important parameters used in the transistor models of the last section, the ac emitter resistance $r'_e$, depends on the dc bias current by way of the relation

$$r'_e = \frac{V_T}{I_E} \approx \frac{26\ \text{mV}}{I_{EQ}} \quad \text{(at room temperature)}$$

In fact, all small-signal parameters depend on dc operating conditions, some to a greater extent than others. Our goal now is to develop a transistor model that reflects that dependency better than the models of the previous section. One of the advantages of the model is that it permits us to perform (approximate) small-signal analysis based entirely on a knowledge of the dc

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characteristics of a transistor. We begin with a discussion of a new small-signal parameter, *transconductance*, whose approximate value can be found using only dc quantities.

Transconductance is another *derived* parameter that is widely used in the analysis of electronic devices of all kinds. It is designated $g_m$ and is defined as the ratio of a small-signal *output* current to a small-signal *input* voltage, with dc output voltage held constant:

$$g_m = \left.\frac{i_o}{v_i}\right|_{V_o = \text{constant}} \tag{7–79}$$

Because $g_m$ is the ratio of a current to a voltage, its units are those of conductance, that is, siemens. It is called *trans*conductance because it relates input and output quantities (*across* the device).

For a BJT, transconductance is defined in terms of the common-emitter configuration; that is, input voltage is $v_{be}$ and output current is $i_c$:

$$g_m = \left.\frac{i_c}{v_{be}}\right|_{V_{CEQ}} \tag{7–80}$$

For $v_{be}$ less than about 10 mV, it can be shown that the value of $g_m$ is closely approximated by the following:

$$g_m \approx \frac{I_C}{V_T} \approx \frac{I_C}{26\text{ mV}} \quad \text{(at room temperature)} \tag{7–81}$$

where $I_C$ is the dc collector current and $V_T$ is the thermal voltage $kT/q$. Because $I_E \approx I_C$, we see that $g_m \approx I_E/0.026 = 1/r'_e$ (from equation 7–23).

## Output Resistance

The output resistance of a CE transistor can also be determined using dc bias values. Recall that

$$r_o = \left.\frac{v_{ce}}{i_c}\right|_{I_{BQ}} \tag{7–82}$$

Equation 7–82 states that the output resistance is the reciprocal of the slope of the Q-point base current on a set of CE output characteristics. See Figure 7–41.

From Figure 7–41, it is apparent that

$$r_o = \frac{V_A + V_{CEQ}}{I_{CQ}} \tag{7–83}$$

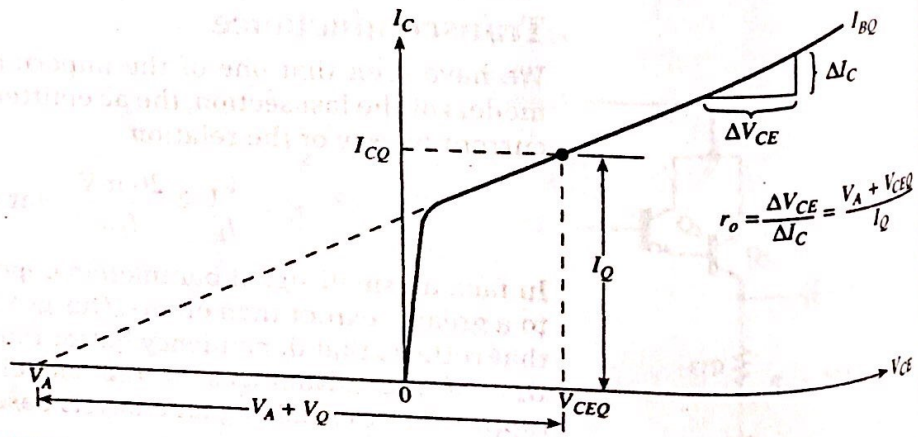


**FIGURE 7–41** Common-emitter output resistance is the reciprocal of the slope of a line of constant base current on the CE output characteristics

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where $V_A$ = Early voltage
$V_{CEQ}$ = quiescent collector-emitter voltage
$I_{CQ}$ = quiescent collector current

Instead of output resistance, the output *conductance* $g_o$ is used in some transistor models:

$$g_o = \frac{1}{r_o} \tag{7–84}$$

## The Hybrid-π Model

Figure 7–42 shows a CE transistor model based on the parameters we have discussed in this section called the hybrid-π model. Note that the current source representing collector current is now labeled $g_m v_{be}$. From equation 7–80, we have $i_c = g_m v_{be}$, so the current source is correctly labeled. Because the hybrid-π model utilizes $g_m$, it is often called a *transconductance model.*

Analysis of a CE amplifier using the hybrid-π model is very similar to our previous analysis because the two structures are identical. Refer to the basic CE amplifier whose ac equivalent circuit is shown in Figure 7–43. The input resistance is clearly $r_\pi$; whereas the current gain, which is the ratio of collector current to base current, can be obtained using the current-division rule as

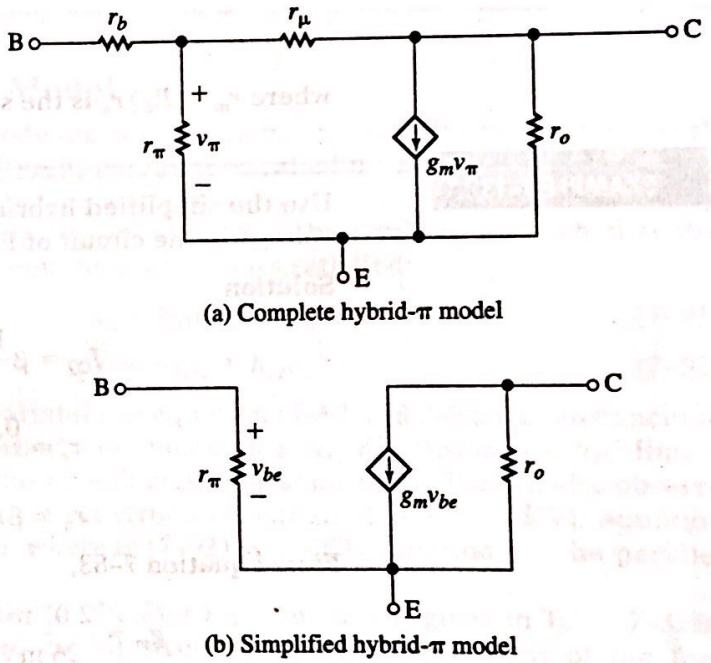


**FIGURE 7–42** The common-emitter hybrid-π model for mid-band frequencies

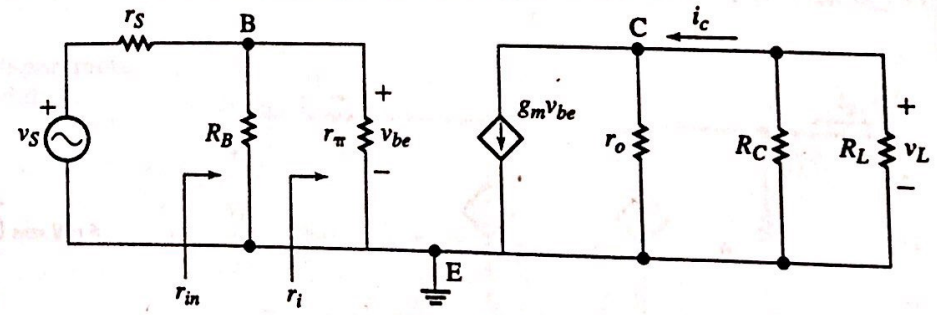


**FIGURE 7–43** A basic CE amplifier with the hybrid-π model

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$$A_i = g_m r_\pi \left(\frac{r_o}{r_o + r_L}\right) \tag{7–85}$$

Compare this expression to the one previously derived, namely, $A_i = \beta[r_o/(r_o + r_L)]$. It is clear that the two models are then related by the following expressions:

$$r_\pi = \beta r'_e \tag{7–86}$$

and

$$\beta = g_m r_\pi \tag{7–87}$$

The voltage gain, which is the ratio of the load voltage to the base-emitter voltage can be written as

$$A_v = \frac{v_L}{v_{be}} = \frac{-g_m v_{be}(r_o \| r_L)}{v_{be}} = -g_m(r_o \| r_L) \tag{7–88}$$

which, when $r_o \gg r_L$, reduces to

$$A_v = -g_m r_L \quad (r_L \gg r_o) \tag{7–89}$$

The reader can verify that the same results can be obtained by invoking the general voltage gain expression $A_v = -A_i(r_L/r_i)$.

The overall gain $A_{vs}$, which takes into account the source resistance $r_s$, is written as

$$A_{vs} = -g_m(r_L \| r_o)\left(\frac{r_{in}}{r_s + r_{in}}\right) \tag{7–90}$$

where $r_{in} = R_B \| r_\pi$ is the stage input resistance.

**EXAMPLE 7–13**

Use the simplified hybrid-$\pi$ model of Figure 7–42(b) to determine the load voltage in the circuit of Figure 7–44. Assume that $\beta = 80$ and $V_A = 140$ V.

**Solution**

$$I_{CQ} = \beta\frac{V_{CC} - 0.7}{R_B} = (80)\frac{9.3\text{ V}}{360\text{ k}} = 2.07\text{ mA}$$

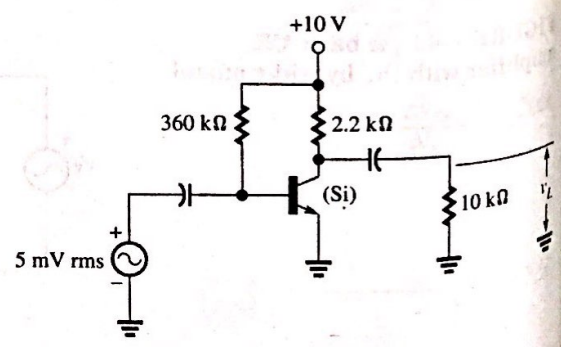
$$r'_e = \frac{0.026\text{ V}}{I_E} = \frac{0.026}{2.07\text{ mA}} = 12.56\ \Omega$$

$$r_\pi \approx \beta r'_e = (80)(12.56\ \Omega) \approx 1\text{ k}\Omega$$

From equation 7–83,

$$g_m = \frac{2.07\text{ mA}}{26\text{ mV}} = 79.6\text{ mS}$$

**FIGURE 7–44** (Example 7–13)

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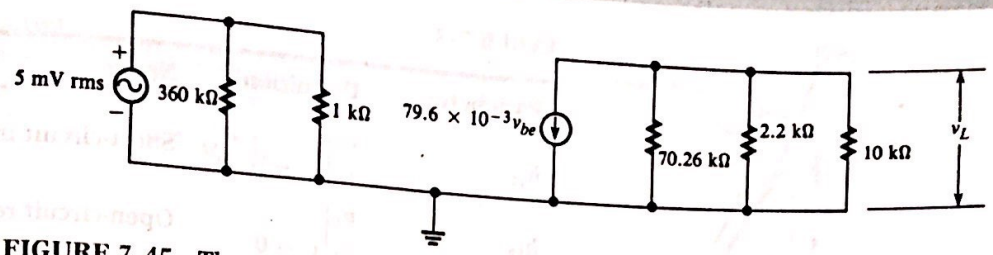


**FIGURE 7–45** The ac equivalent circuit of Figure 7–44 (Example 7–13)

$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 10\text{ V} - (2.07\text{ mA})(2.2\text{ k}\Omega) = 5.45\text{ V}$$

From equation 7–92,

$$r_o = \frac{V_A + V_{CEQ}}{I_Q} = \frac{(140 + 5.45)\text{ V}}{2.07 \times 10^{-3}\text{ A}} = 70.26\text{ k}\Omega$$

Figure 7–45 shows the ac equivalent circuit of the amplifier with the transconductance model incorporated. The total equivalent resistance across the output is $(70.26\text{ k}\Omega)\|(2.2\text{ k}\Omega)\|(10\text{ k}\Omega) \approx 1.8\text{ k}\Omega$. Therefore, the voltage gain, using equation 7–89, is

$$A_v = -(79.6\text{ mS})(1.8\text{ k}) = -143$$

The magnitude of the load voltage is therefore (5 mV)(143) = 715 mV.

## The *h* Parameter Model

Another scheme of modeling transistors makes use of a two-port network structure with four different parameters, called *hybrid* or *h parameters*. The *h*-parameter circuit structure is shown in Figure 7–46, where we can identify the four parameters: $h_{11}$, $h_{12}$, $h_{21}$, and $h_{22}$. Their values are such that the following two network equations are always satisfied:

$$v_1 = h_{11}i_1 + h_{12}v_2 \tag{7–91}$$

$$i_2 = h_{21}i_1 + h_{22}v_2 \tag{7–92}$$

By observing the variables in equations 7–91 and 7–92, we can conclude that $h_{11}$ must be resistance or impedance, $h_{12}$ dimensionless, $h_{21}$ dimensionless, and $h_{22}$ must be a conductance or admittance. We can also observe that, according to the circuit structure, equation 7–91 is a KVL equation around the input loop, whereas (7–92) is a KCL equation for the parallel output circuit.

The formal definition of the four *h* parameters is given in Table 7–3. By observing carefully the circuit structure and the definitions of the four parameters, and by analogy with the previous CE models, we can identify $h_{11}$ as being $\beta r'_e$ or $r_\pi$. Similarly, the parameter $h_{21}$ is equivalent to β, and $h_{22}$ is

**FIGURE 7–46** The *h*-parameter two-port network model

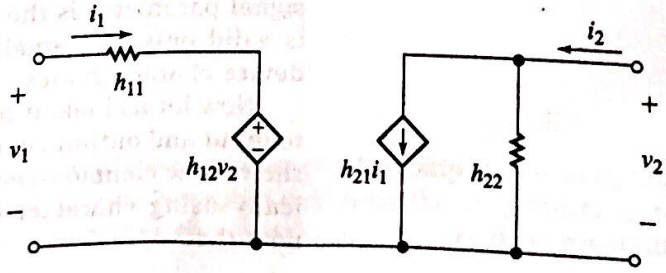


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TABLE 7–3

| Parameter | Definition | Name |
|---|---|---|
| $h_{11}$ | $\left.\frac{v_1}{i_1}\right\|_{v_2 = 0}$ | Short-circuit input impedance |
| $h_{12}$ | $\left.\frac{v_1}{v_2}\right\|_{i_1 = 0}$ | Open-circuit reverse voltage ratio |
| $h_{21}$ | $\left.\frac{i_2}{i_1}\right\|_{v_2 = 0}$ | Short-circuit forward current ratio |
| $h_{22}$ | $\left.\frac{i_2}{v_2}\right\|_{i_1 = 0}$ | Open-circuit output admittance |

simply the reciprocal of $r_o$. Up to now, we had not used a parameter equivalent to $h_{12}$. This parameter is useful for modeling the small effect that the output voltage has on the input behavior, an effect that was mentioned at the beginning of the chapter but was considered negligible.

Even though these parameters can be used for describing any two-port network, we will concentrate on their use for characterizing BJTs as small-signal amplifiers. In this application, $h$ parameters are used with two-letter subscripts that not only identify the specific parameter but also the particular configuration: CB, CE, or CC. The equivalencies for the first subscript are as follows:

$h_{11} = h_i$ (from input)
$h_{12} = h_r$ (from reverse)
$h_{21} = h_f$ (from forward)
$h_{22} = h_o$ (from output)

The second subscript is simply $b$, $e$, or $c$ to indicate CB, CE, or CC, respectively. For example, the parameter $h_{ie}$ is the input resistance in CE configuration, that is, $\beta r'_e$ or $r_\pi$; $h_{fb}$ is the forward current transfer ratio in CB configuration, which would be equivalent to $\alpha$ (actually $-\alpha$ because of the direction of the collector current in the CB configuration). Thus, the 12 $h$ parameters for a bipolar transistor are designated

$h_{ie}, h_{fe}, h_{re}, h_{oe}$: common-emitter $h$ parameters
$h_{ic}, h_{fc}, h_{rc}, h_{oc}$: common-collector $h$ parameters
$h_{ib}, h_{fb}, h_{rb}, h_{ob}$: common-base $h$ parameters

If all of the $h$-parameter values in one configuration are known, then the values corresponding to any other configuration can be determined. The common-emitter values are the ones most often given in data sheets.

The values specified for transistor $h$ parameters are almost always small-signal quantities. Occasionally, a dc value will be given, in which case it is common practice to use capital-letter subscripts, as, for example, $h_{FE}$. It is important to remember that all small-signal BJT parameter values are affected by dc (quiescent) current, as discussed previously. Each small-signal parameter is the ratio of certain ac voltages and currents, and each is valid only in a small region over which there is negligible change in device characteristics.

Now let us look at how the basic definitions of the $h$ parameters relate to input and output characteristics of a BJT in the CE modality. Figure 7–47 shows how common-emitter $h$-parameter values can be determined graphically using characteristic curves. In the common-emitter configuration, note that

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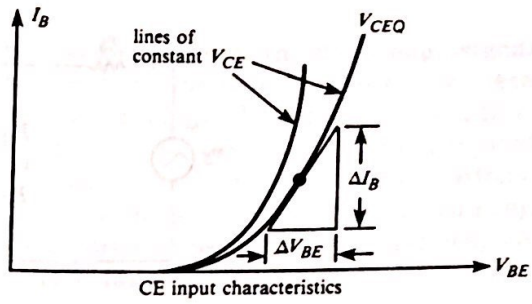
**FIGURE 7–47** Graphical determination of common-emitter $h$ parameters. Notice that the ac quantities $v_{ce}$ and $i_b$ are 0 when the dc quantities $V_{CE}$ and $I_B$ are held constant

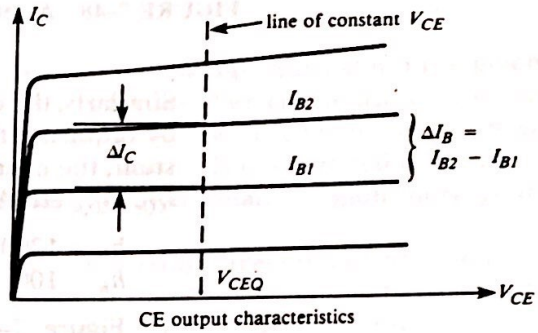
$$h_{11} = \left.\frac{v_1}{i_1}\right|_{v_2 = 0}$$

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$



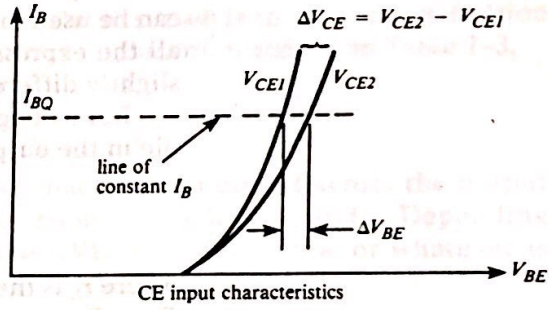

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2 = 0}$$

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}} = \beta$$



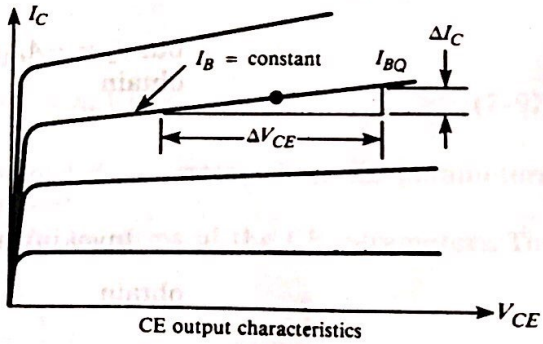

$$h_{12} = \left.\frac{v_1}{v_2}\right|_{i_1 = 0}$$

$$h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right|_{I_B = \text{constant}}$$




$$h_{22} = \left.\frac{i_2}{v_2}\right|_{i_1 = 0}$$

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B = \text{constant}}$$




$$v_1 = v_{be} \qquad i_1 = i_b$$

and

$$v_2 = v_{ce} \qquad i_2 = i_c$$

Therefore, from the definitions of the $h$ parameters, the computation of $h_{ie}$ and $h_{fe}$ must be performed with $v_{ce} = 0$. Note that requiring the *ac* quantity $v_{ce}$ to be 0 is the same as requiring that the *dc* quantity $V_{CE}$ be held constant.

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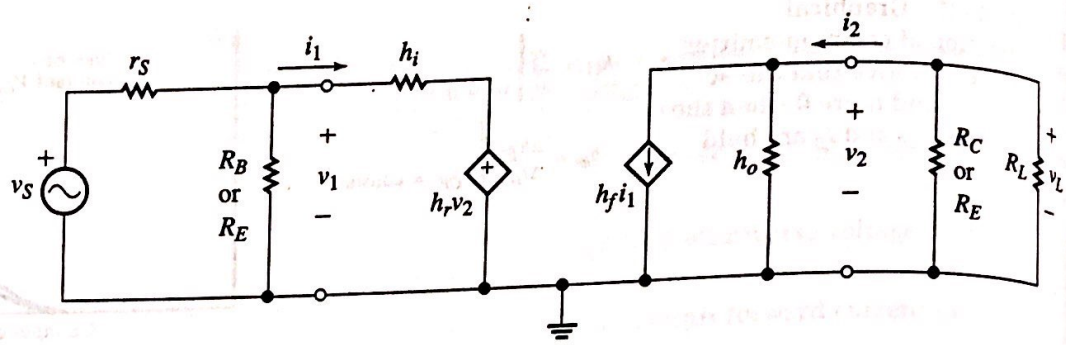


FIGURE 7–48 A general amplifier using the h-parameter small-signal model

Similarly, the computation of $h_{re}$ and $h_{oe}$ requires that $i_b = 0$, which is satisfied by requiring that $I_B$ remain constant. Furthermore, besides being held constant, the conditional variables should be set at their Q-point values, such as $I_{CQ}$, $V_{CEQ}$, etc. A typical set of $h$-parameter values for a silicon *npn* transistor is

$$h_{ie} = 1200\ \Omega \qquad h_{re} = 2 \times 10^{-4}$$
$$h_{fe} = 100 \qquad h_{oe} = 20 \times 10^{-6}\ \text{S}$$

Figure 7–48 shows a general amplifier modeled with $h$ parameters. Notice that the parameters are shown with the first subscript only because the analysis is identical for the three configurations. The resulting equations can be used for any particular case by simply adding the second subscript to all the expressions. The presence of the $h$ parameter $h_r$ makes the analysis slightly different but it remains straightforward.

Let us begin with the current gain $A_i$. Using the current-division principle in the output circuit, we can solve for the ratio $i_2/i_1$ and obtain

$$\frac{i_2}{i_1} = A_i = \frac{h_f}{1 + h_o r_L} \tag{7–93}$$

where $r_L$ is the total ac load resistance, including any biasing resistor such as $R_C$ or $R_E$.

To obtain the input resistance, we write the KVL equation

$$v_1 = h_i i_1 + h_r v_2$$

but $v_2 = -A_i i_1 r_L$. Therefore, substituting $v_2$ and solving for the ratio $v_1/i_1$, we obtain

$$\frac{v_1}{i_1} = r_i = h_i - A_i h_r r_L = h_i - \frac{h_r h_f r_L}{1 + h_o r_L} \tag{7–94}$$

Invoking again the general form for the voltage gain $A_v = -A_i \dfrac{r_L}{r_i}$, we can obtain

$$A_v = \frac{v_2}{v_1} = \frac{-h_f r_L}{h_i(1 + h_o r_L) - h_r h_f r_L} \tag{7–95}$$

Overall gain, $A_{vs}$, is again expressed as $A_v$ times the voltage-division fraction of the input circuit; that is,

$$A_{vs} = A_v \left( \frac{r_{in}}{r_S + r_{in}} \right) \tag{7–96}$$

where $r_{in}$ is the stage input resistance given by $r_{in} = R_B \| r_i$ for CE, or $r_{in} = R_E \| r_i$ for CB.

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As you can see, there are more similarities between the three small-signal models we have so far analyzed than there are differences. To better use these models, we should concentrate on understanding the definitions of the different parameters and what they represent, try to memorize at least their typical values, understand the differences between the amplifying configurations, and avoid looking at these models as sets of magic formulas for substituting numbers. Of course, it is important to memorize a few important equations, but understanding where they came from is by far more important.

## Conversion Formulas

If we have the $h$-parameter values for a particular transistor in a given configuration, the full set of parameters for another configuration can be obtained through conversion formulas. Let us derive the conversion formulas for two cases to illustrate the process. The reader is encouraged to derive a few more formulas because this is an excellent means to gain more good skills in amplifier analysis.

Consider deriving the formulas for converting parameters from common emitter to common collector. Although it is not strictly necessary, rearranging the original circuit can help in making the derivation less difficult. Figure 7–49 shows the CE $h$-parameter model with the base as input, the emitter as output, and the collector grounded.

Let us derive the formula for $h_{fc}$. The first step is to write the definition of the parameter we want to obtain. Using the definitions from Table 7–3,

$$h_{fc} = \left.\frac{i_e}{i_b}\right|_{v_{ec}=0}$$

To satisfy the condition $v_{ec} = 0$, we place a short circuit across the output terminals, and then we write an equation that includes $i_e$ and $i_b$. Depending on the circuit structure, we can use KVL, KCL, Ohm's law, or whatever is appropriate.

Using KCL we write

$$i_b + h_{fe}i_b + i_e = 0$$

Solving for $\frac{i_e}{i_b}$ yields

$$\frac{i_e}{i_b} = -(1 + h_{fe}) = h_{fc} \tag{7–97}$$

To obtain the conversion formulas for CB parameters from CE parameters, we use the circuit shown in Figure 7–50.

We will derive the formula for $h_{ob}$ in terms of the CE parameters. The definition is

$$h_{ob} = \left.\frac{i_c}{v_{cb}}\right|_{i_e=0}$$

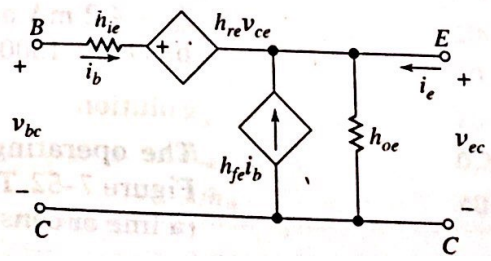


FIGURE 7–49 Circuit for obtaining CC parameters from CE parameters

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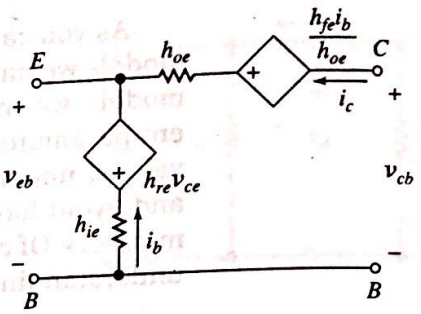


**FIGURE 7–50** Circuit for obtaining CB parameters from CE parameters. Note the source transformation

Leaving the input port open to satisfy the condition $i_e = 0$, we write an expression that relates $v_{cb}$ and $i_c$ as follows:

$$i_c = \frac{v_{cb} + h_{fe}i_b/h_{oe} + h_{re}v_{ce}}{h_{ie} + 1/h_{oe}}$$

Noting that $i_b = -i_c$ and $v_{ce} = \frac{i_c}{h_{oe}} + \frac{h_{fe}i_c}{h_{oe}}$,

$$i_c\left(h_{ie} + \frac{1}{h_{oe}} + \frac{h_{fe}}{h_{oe}} - \frac{h_{re}}{h_{oe}} - \frac{h_{re}h_{fe}}{h_{oe}}\right) = v_{cb}$$

Solving for $i_c/v_{cb}$ yields

$$\frac{i_c}{v_{cb}} = \frac{h_{oe}}{h_{ie}h_{oe} + (1 + h_{fe})(1 - h_{re})} = h_{ob} \tag{7–98}$$

Table 7–4 shows the conversion formulas between the three BJT configurations along with typical values for the four parameters in each configuration. Note that these conversion formulas can be simplified substantially by neglecting terms that are very small compared to other terms in the expression. For example, $h_{re}$ and $h_{rb}$ are very small and therefore $(1 - h_{re})$ and $(1 - h_{rb})$ become simply 1. Other instances are the products $h_{ie}h_{oe}$ and $h_{ib}h_{ob}$ which are much less than 1, as well as the fact that $h_{rc} \approx 1$. It is left to the reader to develop a set of approximate conversion formulas based on these facts.

Figure 7–51 shows the manufacturer's small-signal specifications for the 2N2218A–2N2222A series transistors whose dc specifications were given in Chapter 4. The graphs showing how the $h$ parameters vary with collector current clearly demonstrate the dependence of parameter values on dc conditions. Note also that a significant variation is possible among devices of the same type. Each graph shows the $h$-parameter variation for a typical "high-gain" unit (labeled 1) and for a typical "low-gain" unit (labeled 2). Table 7–5 shows approximate parameter equivalents and conversions.

**EXAMPLE 7–14**

Using Table 7–4 and the common-emitter output characteristics shown in Figure 7–52, find approximate values for $h_{fe}$, $h_{oe}$, $h_{fb}$, $h_{ob}$, $h_{fc}$, and $h_{oc}$ when $I_C = 4.2$ mA and $V_{CE} = 15$ V. The transistor whose characteristics are shown has $h_{ie} = 1500\ \Omega$ and $h_{re} = 2 \times 10^{-4}$ at the operating point.

**Solution**

The operating point where $I_C = 4.2$ mA and $V_{CE} = 15$ V is labeled Q in Figure 7–52. To find $h_{fe}$, we determine $\Delta I_C$ along the vertical line through Q (a line of constant $V_{CE}$) and the corresponding value of $\Delta I_B$. As shown in the

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TABLE 7–4 *h*-Parameter conversion equations

| | | CE | CB | CC |
|---|---|---|---|---|
| CE | $h_{ie}$ | 1400 Ω | $\dfrac{h_{ib}}{(1+h_{fb})(1-h_{rb})+h_{ib}h_{ob}}$ | $h_{ic}$ |
| | $h_{re}$ | $2\times10^{-4}$ | $\dfrac{h_{ib}h_{ob}-h_{rb}(1+h_{fb})}{(1+h_{fb})(1-h_{rb})+h_{ib}h_{ob}}$ | $1-h_{rc}$ |
| | $h_{fe}$ | 100 | $\dfrac{-h_{fb}(1-h_{rb})-h_{ob}h_{ib}}{(1+h_{fb})(1-h_{rb})+h_{ib}h_{ob}}$ | $-(1+h_{fc})$ |
| | $h_{oe}$ | $2\times10^{-5}$ S | $\dfrac{h_{ob}}{(1+h_{fb})(1-h_{rb})+h_{ib}h_{ob}}$ | $h_{oc}$ |
| CB | $h_{ib}$ | $\dfrac{h_{ie}}{(1+h_{fe})(1-h_{re})+h_{ie}h_{oe}}$ | 14 Ω | $\dfrac{h_{ic}}{h_{ic}h_{oc}-h_{fc}h_{rc}}$ |
| | $h_{rb}$ | $\dfrac{h_{ie}h_{oe}-h_{re}(1+h_{fe})}{(1+h_{fe})(1-h_{re})+h_{ie}h_{oe}}$ | $4\times10^{-5}$ | $\dfrac{h_{fc}(1-h_{rc})+h_{ic}h_{oc}}{h_{ic}h_{oe}-h_{fc}h_{rc}}$ |
| | $h_{fb}$ | $\dfrac{-h_{fe}(1-h_{re})-h_{ie}h_{oe}}{(1+h_{fe})(1-h_{re})+h_{ie}h_{oe}}$ | −0.99 | $\dfrac{h_{rc}(1+h_{fc})-h_{ic}h_{oc}}{h_{ic}h_{oc}-h_{fc}h_{rc}}$ |
| | $h_{ob}$ | $\dfrac{h_{oe}}{(1+h_{fe})(1-h_{re})+h_{ie}h_{oe}}$ | $2\times10^{-7}$ S | $\dfrac{h_{oc}}{h_{ic}h_{oc}-h_{fc}h_{rc}}$ |
| CC | $h_{ic}$ | $h_{ie}$ | $\dfrac{h_{ib}}{(1+h_{fb})(1-h_{rb})+h_{ib}h_{ob}}$ | 1400 Ω |
| | $h_{rc}$ | $1-h_{re}$ | $\dfrac{1+h_{fb}}{(1+h_{fb})(1-h_{rb})+h_{ib}h_{ob}}$ | 1 |
| | $h_{fc}$ | $-(1+h_{fe})$ | $\dfrac{h_{rb}-1}{(1+h_{fb})(1-h_{rb})+h_{ib}h_{ob}}$ | −101 |
| | $h_{oc}$ | $h_{oe}$ | $\dfrac{h_{ob}}{(1+h_{fb})(1-h_{rb})+h_{ib}h_{ob}}$ | $2\times10^{-5}$ S |

figure, $\Delta I_C \approx (5.6\text{ mA}) - (3.1\text{ mA}) = 2.5\text{ mA}$, and $\Delta I_B = (50\ \mu\text{A}) - (30\ \mu\text{A}) = 20\ \mu\text{A}$. Therefore,

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=15\text{ V}} \approx \frac{2.5\text{ mA}}{20\ \mu\text{A}} = 125$$

TABLE 7–5

| Model Parameter | Hybrid-π Model (CE) | Approximate *h*-Parameter Equivalent | Typical Value |
|---|---|---|---|
| $r'_e$ | $1/g_m$ | $h_{ib}$ | 25 Ω |
| α | — | $h_{fb}$ | 0.99 |
| $r_c$ | $(\beta+1)r_o$ | $1/h_{ob}$ | 5 MΩ |
| $(\beta+1)r'_e$ | $r_\pi$ | $h_{ie}$ | 2.5 kΩ |
| β | $g_m r_\pi$ | $h_{fe}$ | 100 |
| $r_c/(\beta+1)$ | $r_o$ | $1/h_{oe}$ | 50 kΩ |
| $(\beta+1)/r_c$ | — | $h_{oe}$ | 20 μS |
| $1/r_c$ | $1/(\beta+1)r_o$ | $h_{ob}$ | 0.2 μS |
| $1/r'_e$ | $g_m$ | $1/h_{ib}$ | 40 mS |

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**FIGURE 7–51** Typical small-signal specifications (Courtesy of Motorola Corporation)

**SMALL-SIGNAL CHARACTERISTICS**

| | | | | | |
|---|---|---|---|---|---|
| Current-Gain — Bandwidth Product(2) ($I_C$ = 20 mAdc, $V_{CE}$ = 20 Vdc, f = 100 MHz) | All Types, Except<br>2N2219A, 2N2222A, 2N5582 | $f_T$ | 250<br>300 | —<br>— | MHz |
| Output Capacitance(3) ($V_{CB}$ = 10 Vdc, $I_E$ = 0, f = 100 kHz) | | $C_{obo}$ | — | 8.0 | pF |
| Input Capacitance(3) ($V_{EB}$ = 0.5 Vdc, $I_C$ = 0, f = 100 kHz) | Non-A Suffix<br>A-Suffix, 2N5581, 2N5582 | $C_{ibo}$ | —<br>— | 30<br>25 | pF |
| Input Impedance ($I_C$ = 1.0 mAdc, $V_{CE}$ = 10 Vdc, f = 1.0 kHz) | 2N2218A, 2N2221A<br>2N2219A, 2N2222A | $h_{ie}$ | 1.0<br>2.0 | 3.5<br>8.0 | kohms |
| ($I_C$ = 10 mAdc, $V_{CE}$ = 10 Vdc, f = 1.0 kHz) | 2N2218A, 2N2221A<br>2N2219A, 2N2222A | | 0.2<br>0.25 | 1.0<br>1.25 | |
| Voltage Feedback Ratio ($I_C$ = 1.0 mAdc, $V_{CE}$ = 10 Vdc, f = 1.0 kHz) | 2N2218A, 2N2221A<br>2N2219A, 2N2222A | $h_{re}$ | —<br>— | 5.0<br>8.0 | X 10⁻⁴ |
| ($I_C$ = 10 mAdc, $V_{CE}$ = 10 Vdc, f = 1.0 kHz) | 2N2218A, 2N2221A<br>2N2219A, 2N2222A | | —<br>— | 2.5<br>4.0 | |
| Small-Signal Current Gain ($I_C$ = 1.0 mAdc, $V_{CE}$ = 10 Vdc, f = 1.0 kHz) | 2N2218A, 2N2221A<br>2N2219A, 2N2222A | $h_{fe}$ | 30<br>50 | 150<br>300 | — |
| ($I_C$ = 10 mAdc, $V_{CE}$ = 10 Vdc, f = 1.0 kHz) | 2N2218A, 2N2221A<br>2N2219A, 2N2222A | | 50<br>75 | 300<br>375 | |
| Output Admittance ($I_C$ = 1.0 mAdc, $V_{CE}$ = 10 Vdc, f = 1.0 kHz) | 2N2218A, 2N2221A<br>2N2219A, 2N2222A | $h_{oe}$ | 3.0<br>5.0 | 15<br>35 | μmhos |
| ($I_C$ = 10 mAdc, $V_{CE}$ = 10 Vdc, f = 1.0 kHz) | 2N2218A, 2N2221A<br>2N2219A, 2N2222A | | 10<br>25 | 100<br>200 | |

**h PARAMETERS**

$V_{CE}$ = 10 Vdc, f = 1.0 kHz, $T_A$ = 25°C

This group of graphs illustrates the relationship between $h_{fe}$ and other "h" parameters for the series of transistors. To obtain these curves, a high-gain and a low-gain unit were selected and the same units were used to develop the correspondingly numbered curves on each graph.

FIGURE 5 — INPUT IMPEDANCE

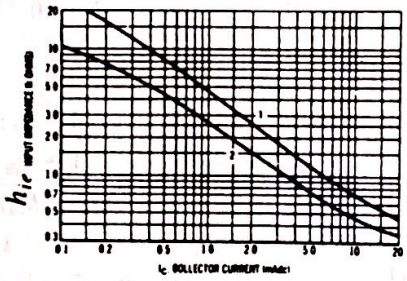



FIGURE 6 — VOLTAGE FEEDBACK RATIO

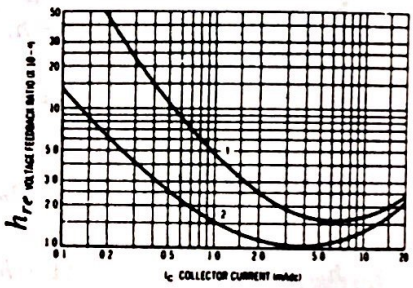



FIGURE 7 — CURRENT GAIN

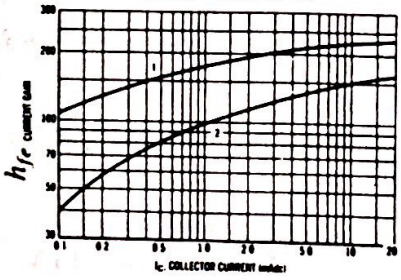
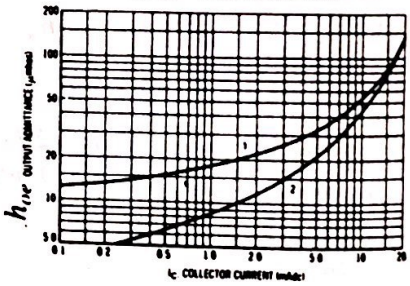



FIGURE 8 — OUTPUT ADMITTANCE




To find $h_{oe}$, we determine the slope of the line corresponding to $I_B = 40\ \mu A$ (a line of constant $I_B$). As shown in the figure, $\Delta I_C \approx (4.4\ \text{mA}) - (4\ \text{mA}) = 0.4\ \text{mA}$, and $\Delta V_{CE} \approx (28\ \text{V}) - (2\ \text{V}) = 26\ \text{V}$. Therefore,

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B = 40\ \mu A} \approx \frac{0.4 \times 10^{-3}}{26} = 15.38\ \mu S$$

From Table 7–4,

$$h_{fb} = \frac{-h_{fe}(1 - h_{re}) - h_{ie}h_{oe}}{(1 + h_{fe})(1 - h_{re}) + h_{ie}h_{oe}}$$

$$= \frac{-125(1 - 2 \times 10^{-4}) - 1500(15.38 \times 10^{-6})}{126(1 - 2 \times 10^{-4}) + 1500(15.38 \times 10^{-6})} = -0.992$$

$$h_{ob} = \frac{h_{oe}}{(1 + h_{fe})(1 - h_{re}) + h_{ie}h_{oe}}$$

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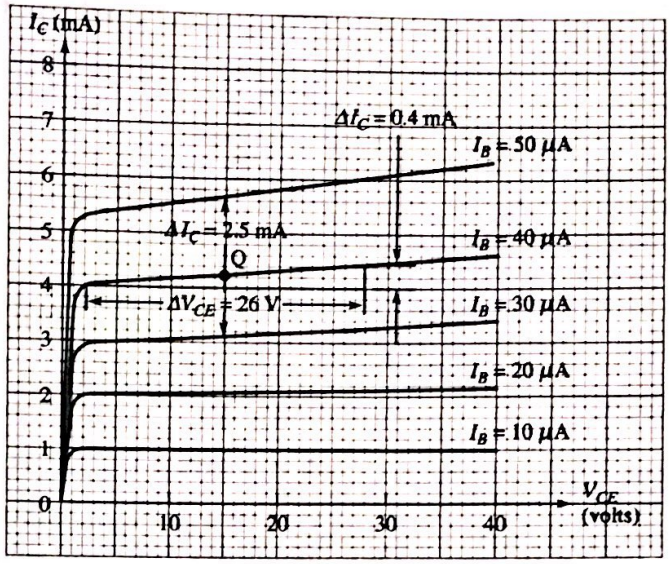
FIGURE 7–52 (Example 7–14)




$$= \frac{15.38 \times 10^{-6}}{126(1 - 2 \times 10^{-4}) + 1500(15.38 \times 10^{-6})} = 1.22 \times 10^{-7}\ \text{S}$$

$$h_{fc} = -(1 + h_{fe}) = -126$$

$$h_{oc} = h_{oe} = 15.38\ \mu\text{S}$$

**EXAMPLE 7–15**

The transistor shown in Figure 7–53 has the following $h$-parameter values: $h_{ie} = 1600\ \Omega$, $h_{fe} = 80$, $h_{re} = 2 \times 10^{-4}$, $h_{oe} = 20\ \mu\text{S}$. Find (1) $A_i$, (2) $r_i$, (3) $r_{in}$, (4) $A_v$, (5) $A_{vs}$, (6) $r_o$, and (7) $r_{out}$.

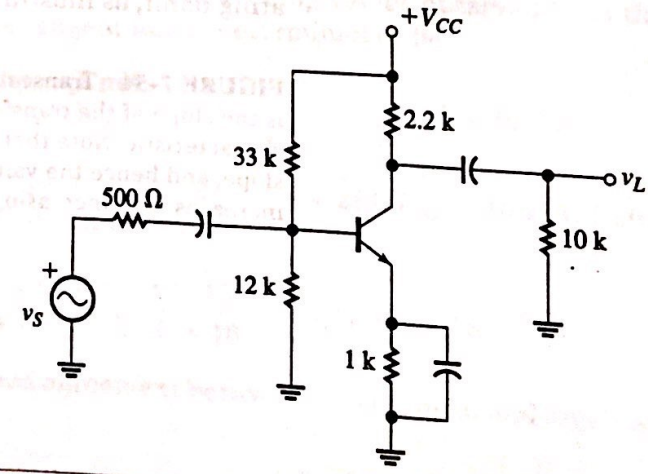
**Solution**

1. $r_L = 2.2\ \text{k} \| 10\ \text{k} = 1.8\ \text{k}$

$$A_i = \frac{h_{fe}}{1 + h_{oe}r_L} = \frac{80}{1 + (20\ \mu\text{S})(1.8\ \text{k})} = 77.2$$

2. $r_i = h_{ie} - A_i h_{re} r_L = 1.6\ \text{k} - 77.2(2 \times 10^{-4})(1.8\ \text{k}) = 1.57\ \text{k}\Omega$
3. $R_B = 33\ \text{k} \| 12\ \text{k} = 8.8\ \text{k}\Omega$

FIGURE 7–53 (Example 7–15)

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$$r_{in} = 1.57\text{ k}\|8.8\text{ k} = 1.33\text{ k}\Omega$$

4. $A_v = -A_i\dfrac{r_L}{r_i} = -77.2\left(\dfrac{1.8\text{ k}}{1.57\text{ k}}\right) = -88.5$

5. $A_{vs} = A_v\left(\dfrac{r_{in}}{r_S + r_{in}}\right) = -88.5\left(\dfrac{1.33\text{ k}}{500 + 1.33\text{ k}}\right) = -64.3$

6. $r_o = \dfrac{1}{h_{oe} - \dfrac{h_{fe}h_{re}}{h_{ie} + r_S\|R_B}} = \dfrac{1}{1.6\text{ k} - \dfrac{80(2\times10^{-4})}{1.6\text{ k} + 500\|8.8\text{ k}}} = 81.4\text{ k}\Omega$

7. $r_{out} = r_o\|R_C = 81.4\text{ k}\|2.2\text{ k} = 2.14\text{ k}\Omega \approx R_C$

## 7–6 THE COMMON-SOURCE JFET AMPLIFIER

Like bipolar transistors, field-effect transistors can be connected as ac amplifiers to achieve voltage, power, and/or current gain. For example, in the most useful JFET configuration, the *common-source* amplifier, a small variation in the gate-to-source (input) voltage creates a large variation in the drain-to-source (output) voltage, when the device is operated in its pinch-off region. We will develop equations that allow us to compute the magnitude of the gain in this and other FET configurations when the input variation is small compared to its total possible range, i.e., under small-signal conditions. We begin with a discussion of the FET small-signal parameters that directly affect gain magnitude computations.

### Small-Signal JFET Parameters

Recall that transconductance is defined to be the ratio of a small-signal output current ($i_o$) to the small-signal input voltage ($v_i$) that produced it. The transconductance of a JFET is defined in the context of a *common-source* configuration, for which the output current is $i_d$ and the input voltage is $v_{gs}$:

$$g_m = \frac{i_d}{v_{gs}} = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\,=\,\text{constant}} \tag{7–99}$$

where $\Delta I_D$ is the *change* in drain current caused by $\Delta V_{GS}$, the *change* in gate-to-source voltage. Note that we resume the use of lowercase letters in keeping with the usual convention for representing small-signal quantities. The value of $g_m$ can be found graphically using a JFET transfer characteristic, since the latter is a plot of drain current versus gate-to-source voltage. Transconductance is thus the *slope* of the transfer characteristic at the operating point, as illustrated in Figure 7–54.

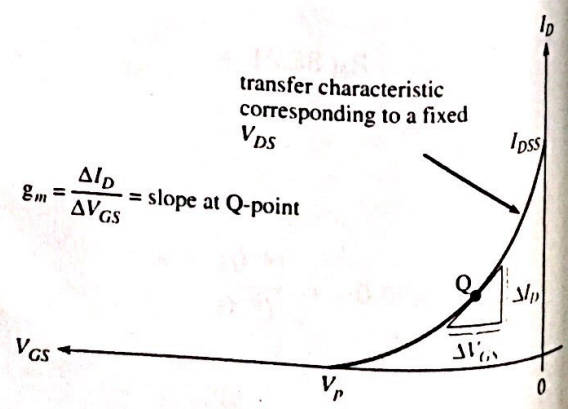


**FIGURE 7–54** Transconductance is the slope of the transfer characteristic. Note that the slope, and hence the value of $g_m$ increases with increasing $I_D$.

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As shown in the figure, $g_m$ is calculated graphically by drawing a line tangent to the characteristic at the quiescent point and then measuring its slope. Note that transconductance increases with increasing values of $I_D$, that is, at Q-points lying farther up the curve toward $I_{DSS}$, because the curve becomes steeper in that direction. Because the current in a JFET amplifier varies above and below the Q-point, and because the transconductance changes at every point along the characteristic, small-signal analysis is valid only if $\Delta I_D$ is small enough to make the change in $g_m$ negligible.

It can be shown that under small-signal conditions the value of $g_m$ is approximately given by

$$g_m = \frac{2I_{DSS}}{|V_p|}\left(1 - \left|\frac{V_{GS}}{V_p}\right|\right) \text{ siemens} \tag{7–100}$$

where $V_{GS}$ is the quiescent value of the gate-to-source voltage. The use of absolute values in equation 7–100 makes it valid for both *n*-channel and *p*-channel devices. Equation 7–100 can be used in conjunction with the equation for the transfer characteristic to express $g_m$ in terms of $I_D$, the quiescent value of the drain current:

$$g_m = \frac{2I_{DSS}}{|V_p|}\sqrt{\frac{I_D}{I_{DSS}}} \text{ siemens} \tag{7–101}$$

Equation 7–101 clearly shows that the value of $g_m$ increases with increasing $I_D$. It is a maximum when $I_D = I_{DSS}$, for which it is given the special symbol $g_{mO}$. From equation 7–101 with $I_D = I_{DSS}$, we have

$$g_{mO} = \frac{2I_{DSS}}{|V_p|} \text{ siemens} \tag{7–102}$$

Although a large value of $g_m$ is desirable, and results in a large voltage gain (as we shall presently see), we would never bias a JFET at $I_D = I_{DSS}$ for small-signal operation. Obviously, no signal variation above that Q-point could occur if that were the case.

**EXAMPLE 7–16**

An *n*-channel JFET has the transfer characteristic shown in Figure 7–55. Determine, both (1) graphically and (2) algebraically, the value of its transconductance when $I_D = 4$ mA. Also determine the value of $g_{mO}$.

**Solution**

1. As shown in Figure 7–55, a line is drawn tangent to the transfer characteristic at the point where $I_D = 4$ mA. Using values obtained from the figure, the slope of the tangent line is determined to be

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{(6 \text{ mA}) - (2 \text{ mA})}{(2.1 \text{ V}) - (0.8 \text{ V})} = \frac{4 \times 10^{-3} \text{ A}}{1.3 \text{ V}} = 3.077 \times 10^{-3} \text{ S}$$

2. From Figure 7–55, it is evident that $V_p = -4$ V and $I_{DSS} = 10$ mA. Using equation 7–101 with $I_D = 4$ mA, we find

$$g_m = \frac{2(10 \times 10^{-3} \text{ A})}{4 \text{ V}}\sqrt{\frac{4 \times 10^{-3}}{10 \times 10^{-3}}} = 3.16 \times 10^{-3} \text{ S}$$

We see that there is good agreement between the graphical and algebraic solutions.

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FIGURE 7–55 (Example 7–16)

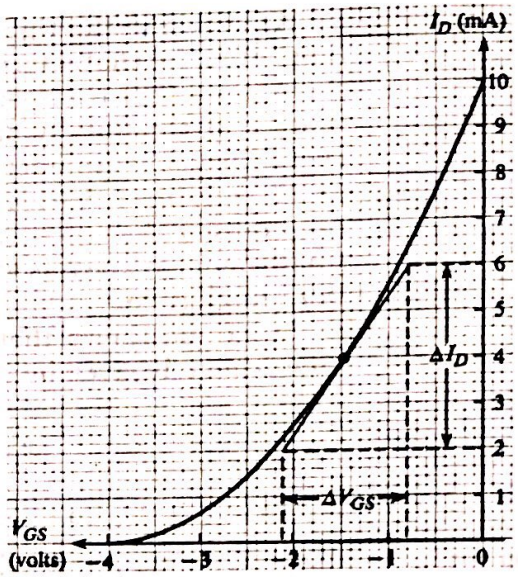
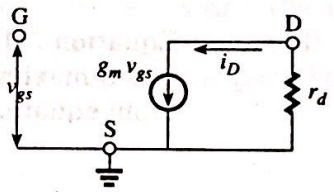



FIGURE 7–56 Small-signal equivalent circuit of a common-source JFET




The value of $g_{mO}$ is computed using equation 7–102:

$$g_{mO} = \frac{2(10 \times 10^{-3}\ \text{A})}{4\ \text{V}} = 5 \times 10^{-3}\ \text{S}$$

The small-signal output resistance of a common-source JFET is defined by

$$r_o = \frac{v_{ds}}{i_d} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} = \text{constant}} \tag{7–103}$$

This parameter is also called the *drain resistance*, $r_d$ or $r_{ds}$. It can be determined graphically from a set of drain characteristics, but the lines are so nearly horizontal in the pinch-off region that it is difficult to obtain accurate values. In any case, the value is generally so large that it has little effect on the computation of voltage gain in practical circuits. Values of $r_d$ range from about 50 kΩ to several hundred kΩ in the pinch-off region.

Figure 7–56 shows the small-signal equivalent circuit of the common-source JFET, incorporating the parameters we have discussed. The current source having value $g_m v_{gs}$ is a voltage-controlled current source because the current it produces depends on the (input) voltage $v_{gs}$. It is apparent in the figure that $i_d = g_m v_{gs}$, in agreement with the definition of $g_m$ (equation 7–99):

$$g_m = \frac{i_d}{v_{gs}} \longrightarrow i_d = g_m v_{gs}$$

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Notice that there is an open circuit shown between the gate and source terminals. Because the gate-to-source junction is reverse biased in normal operation, the extremely large resistance between those terminals can be assumed to be infinite in most practical situations.

## The Common-Source JFET Configuration

Figure 7–57 shows a common-source JFET amplifier with fixed-bias $V_{GG}$. $R_G$ is a large resistance connected in series with $V_{GG}$ to prevent the dc source from shorting the ac signal to ground. (Recall that a dc source is an ac short circuit.) The input resistance of the JFET is so large that there is negligible dc voltage division at the gate; that is, the major part of $V_{GG}$ appears from gate-to-source instead of across $R_G$, so $V_{GS} \approx V_{GG}$. From another viewpoint, the dc gate current is so small that there is negligible drop across $R_G$. The input coupling capacitor serves the same purpose it does in a BJT amplifier, namely, to provide dc isolation between the signal source and the FET. For the moment, we ignore any signal-source resistance ($r_S$) and assume that the output is open ($R_L = \infty$).

The total gate-to-source voltage is the sum of the small-signal source voltage, $v_S$, and the bias voltage $V_{GG}$. For example, if $V_{GG} = -2$ V and $v_S$ is a sine wave having peak value 0.1 V, then $v_{gs} = -2 + 0.1 \sin \omega t$ volts. Thus, $v_{gs}$ varies between the extreme values $-2 - 0.1 = -2.1$ V and $-2 + 0.1 = -1.9$ V. When $v_{gs}$ goes more positive (toward $-1.9$ V), the drain current increases. This increase in $i_d$ causes the output voltage $v_{ds}$ to *decrease,* since

$$V_{DS} = V_{DD} - I_D R_D \tag{7–104}$$

We conclude that an increase in the input signal voltage causes a decrease in the output voltage and that the output is therefore 180° out of phase with the input.

Figure 7–58 shows the equivalent circuit of the common-source amplifier in Figure 7–57, with the JFET replaced by its small-signal equivalent. The coupling capacitor is assumed to have negligible impedance at the signal frequency we are considering (for now), so it is replaced by a short circuit. As usual, all dc sources are treated as ac short circuits to ground. Notice that the arrow in the controlled current source can be shown reversed (from Figure 7–56) with a minus sign attached. Note: If the arrow is reversed, the minus sign *must* be attached (not "can be"). The minus sign denotes the phase inversion between input and output, as we have described.

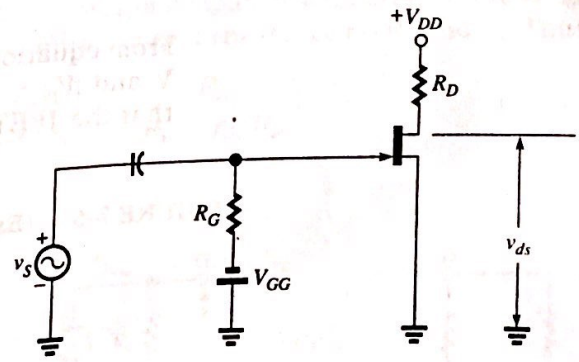


**FIGURE 7–57** A common-source amplifier with fixed bias

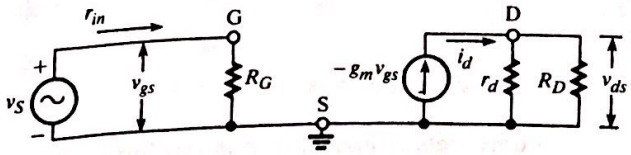


**FIGURE 7–58** The small-signal equivalent circuit of the common-source amplifier shown in Figure 7–57

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It is clear from Figure 7–58 that

$$v_{ds} = i_d(r_d \| R_D) \tag{7–105}$$

Since $i_d = -g_m v_{gs}$, we have

$$v_{ds} = -g_m v_{gs}(r_d \| R_D) \tag{7–106}$$

There is no signal-source resistance, so $v_{gs} = v_S$, and the voltage gain is therefore

$$A_v = \frac{v_{ds}}{v_S} = \frac{v_{ds}}{v_{gs}} = -g_m(r_d \| R_D) \tag{7–107}$$

In most practical amplifier circuits, the value of $r_d$ is much greater than that of $R_D$, so $r_d \| R_D \approx R_D$, and a good approximation for the voltage gain is

$$\frac{v_{ds}}{v_{gs}} \approx -g_m R_D \tag{7–108}$$

It is important to remember that a JFET amplifier is operated in its pinch-off region. Therefore, the bias point and the voltage variations around the bias point must always satisfy $|V_{DS}| \geq |V_p| - |V_{GS}|$.

So long as the signal source does not drive the gate positive with respect to the source, the reverse-biased gate-to-source resistance is very large and the input resistance to the amplifier is essentially $R_G$. The equivalent circuit in Figure 7–58 is based on this assumption, and it can be seen that $r_{in} = R_G$.

**EXAMPLE 7–17**

The JFET in the amplifier circuit shown in Figure 7–59 has $I_{DSS} = 12$ mA, $V_p = -4$ V, and $r_d = 100$ kΩ.

1. Find the quiescent values of $I_D$ and $V_{DS}$.
2. Find $g_m$.
3. Draw the ac equivalent circuit.
4. Find the voltage gain.

**Solution**

1. $I_D$ is found using the equation of the transfer characteristic:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = (12\text{ mA})\left(1 - \frac{-2\text{ V}}{-4\text{ V}}\right)^2 = 3\text{ mA}$$

From equation 7–104, $V_{DS} = 15 - (3\text{ mA})(2.2\text{ k}\Omega) = 8.4$ V. Since $V_{DS} = 8.4$ V and $|V_p| - |V_{GS}| = 4 - 2 = 2$ V, we have $|V_{DS}| > |V_p| - |V_{GS}|$, confirming that the JFET is biased in its pinch-off region.

FIGURE 7–59 (Example 7–17)

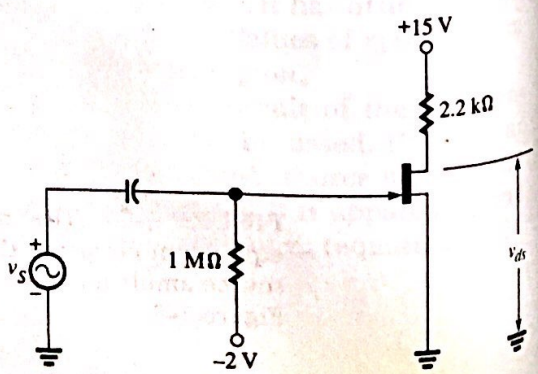


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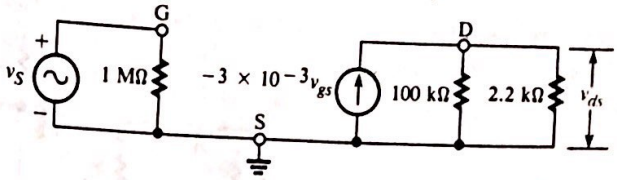
FIGURE 7–60 (Example 7–17)




2. From equation 7–101,

$$g_m = \frac{2(12\text{ mA})}{4\text{ V}}\sqrt{\frac{3\text{ mA}}{12\text{ mA}}} = 3 \times 10^{-3}\text{ S}$$

3. The ac equivalent circuit is shown in Figure 7–60.
4. Since $r_d \| R_D = (100\text{ k}\Omega) \| (2.2\text{ k}\Omega) \approx 2.2\text{ k}\Omega$, we have, from equation 7–108,

$$\frac{v_{ds}}{v_s} = \frac{v_{ds}}{v_{gs}} \approx (-3 \times 10^{-3}\text{ S})(2.2 \times 10^3\ \Omega) = -6.6$$

As the preceding example illustrates, the voltage gain obtainable from a JFET amplifier is much smaller than that which can be obtained from its BJT counterpart. The principal advantage of the JFET amplifier is its very large input resistance.

## The Self-Biased JFET Amplifier

When the JFET amplifier is biased using only the self-biasing resistor, the voltage gain is again computed using $A_v = -g_m(r_d \| R_D)$. A resistor $R_G$ is connected between gate and ground to provide dc continuity for the gate circuit. This resistor can be made very large to maintain a large input resistance to the amplifier. The reverse current through the reverse-biased gate-source junction is very small, so the voltage drop across $R_G$ is negligible. However, if an extremely large resistance is used with a JFET having excessive leakage current, the drop should be taken into account. For example, if $R_G = 10\text{ M}\Omega$ and $I_{DS(reverse)} = 0.1\ \mu\text{A}$, the gate voltage will be increased by $(10\text{ M}\Omega)(0.1\ \mu\text{A}) = 1\text{ V}$ with respect to ground. Figure 7–61 shows the self-biased JFET amplifier and its ac equivalent circuit.

To avoid confusion, we will hereafter refer to resistance associated with the signal source as *signal-source resistance*, which we will designate by $r_S$, and we will continue to refer to resistance in series with the source terminal of the JFET as simply *source resistance*, $R_S$. When signal-source resistance is present, there is the usual voltage division between $r_S$ and the input resistance of the amplifier, $r_i$. When a load resistor $R_L$ is capacitor-coupled to the output, there is also a voltage division between the amplifier output resistance $r_d \| R_D$ and $R_L$. Thus,

$$\frac{v_L}{v_s} = \left(\frac{r_{in}}{r_S + r_{in}}\right) A_v \left(\frac{R_L}{R_L + r_d \| R_D}\right) \tag{7–109}$$

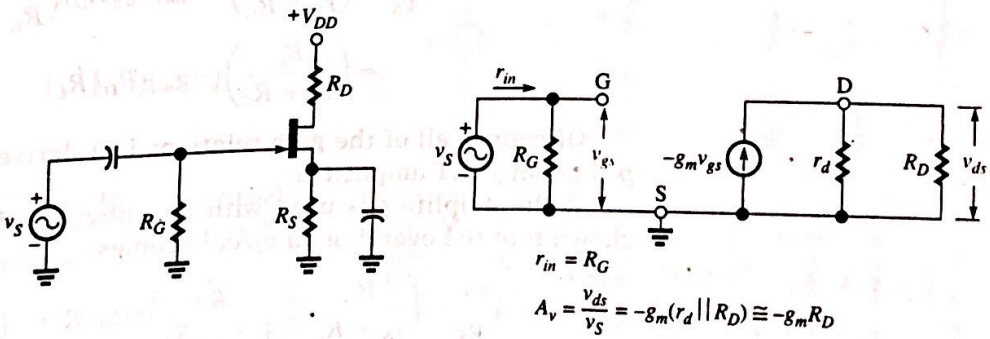



FIGURE 7–61 The self-biased JFET amplifier and its ac equivalent circuit

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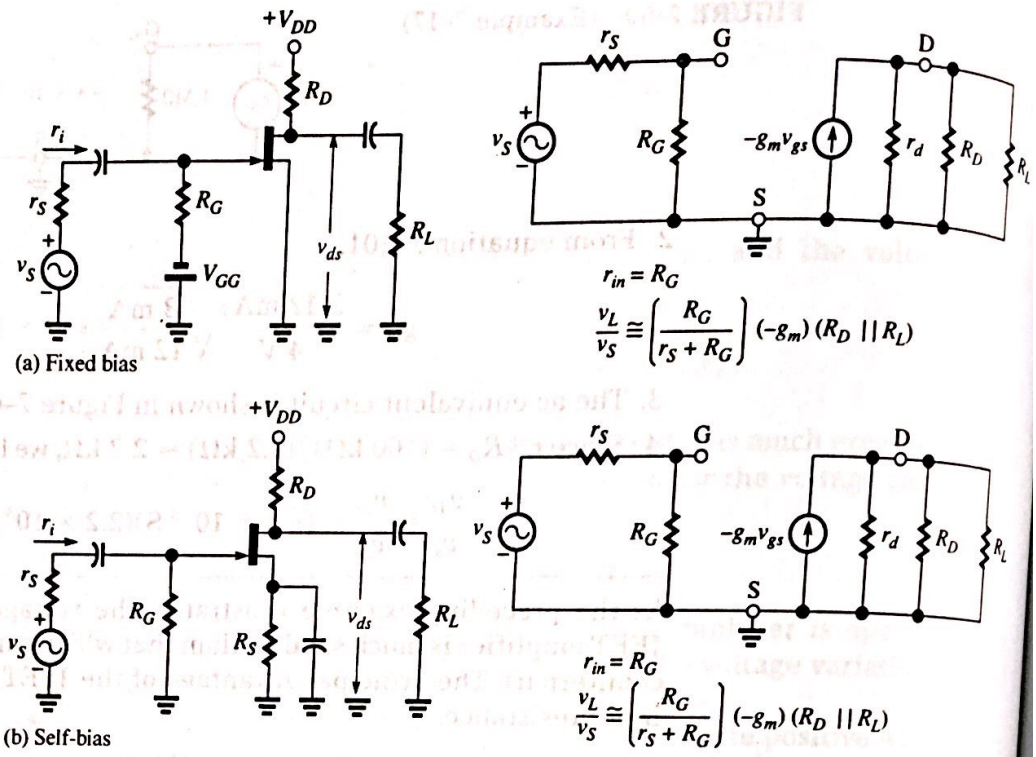


**FIGURE 7–62** Common-source amplifiers with load and signal-source resistances included and their ac equivalent circuits

Figure 7–62 shows the common-source amplifier in a fixed and self-bias arrangement with load and signal-source resistances included. Also shown are the ac equivalent circuits of each. Note in each case that $r_S$ is in series with the amplifier input and $R_L$ is in parallel with the amplifier output.

For the fixed-bias amplifier (Figure 7–62(a)), equation 7–109 becomes

$$\frac{v_L}{v_S} = \left(\frac{R_G}{r_S + R_G}\right)[-g_m(r_d \| R_D)]\left(\frac{R_L}{R_L + r_d \| R_D}\right) \tag{7–110}$$

$$\approx \left(\frac{R_G}{r_S + R_G}\right)(-g_m R_D)\left(\frac{R_L}{R_L + R_D}\right)$$

$$= \left(\frac{R_G}{r_S + R_G}\right)(-g_m)(R_D \| R_L) \tag{7–111}$$

For the self-biased amplifier (Figure 7–62(b)), equation 7–109 becomes

$$\frac{v_L}{v_S} = \left(\frac{R_G}{r_S + R_G}\right)(-g_m)(r_d \| R_D)\left(\frac{R_L}{R_L + r_d \| R_D}\right) \tag{7–112}$$

$$\approx \left(\frac{R_G}{r_S + R_G}\right)(-g_m)(R_D \| R_L) \tag{7–113}$$

Of course, all of the gain relations just derived are exactly the same for *p*-channel JFET amplifiers.

If the amplifier is used with an unbypassed source resistor, it can be shown that the overall gain $v_L/v_S$ becomes

$$\frac{v_L}{v_S} = \left(\frac{R_G}{r_S + R_G}\right)\left(\frac{-g_m}{1 + g_m R_S}\right)(R_D \| R_L) \quad \text{(unbypassed } R_S\text{)} \tag{7–114}$$

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We see that the effect of omitting the bypass capacitor is to reduce gain by the factor $1/(1 + g_m R_S)$. Using the typical values $g_m = 4000\ \mu S$, $R_D = 3\ k\Omega$, and $R_S = 500\ \Omega$, the gain with $R_S$ bypassed is $-g_m R_D = -(4000\ \mu S)(3\ k\Omega) = -12$. This value is reduced in the unbypassed case by the factor $1 + g_m R_S = 1 + (4000\ \mu S)(500\ \Omega) = 3$ to the value $-\frac{12}{3} = -4$.

## 7–7 THE COMMON-DRAIN AND COMMON-GATE JFET AMPLIFIERS

### Common-Drain Amplifier

Figure 7–63 shows a JFET connected as a common-drain amplifier. Note that the drain terminal is connected directly to the supply voltage $V_{DD}$, so the drain is at ac ground. Because the input and output signals are taken with respect to ground, the drain is common to both, which accounts for the name of the configuration. Because the ac output signal is between the source terminal and ground, it is the same signal measured from source to drain as measured across $R_S$. Note that the JFET is biased using the combined self-bias/voltage-divider method, though either of the other two bias methods we studied for the common-source configuration could also be used. As can be seen from the figure,

$$v_i = v_{gs} + v_L \tag{7–115}$$

Therefore, the gate-to-source voltage is

$$v_{gs} = v_i - v_L \tag{7–116}$$

Figure 7–64 shows the ac equivalent circuit of the common-drain amplifier, $v_i$ is related to $v_{gs}$ by equations 7–115 and 7–116. Neglecting the signal-source resistance $r_S$ for the moment, we derive the voltage gain $v_L/v_i$ as follows:

$$v_L = g_m v_{gs}(r_d \| R_S \| R_L) \tag{7–117}$$

Substituting $v_{gs} = v_i - v_L$ (equation 7–116) into (7–117), we obtain

$$v_L = g_m(v_i - v_L)(r_d \| R_S \| R_L)$$

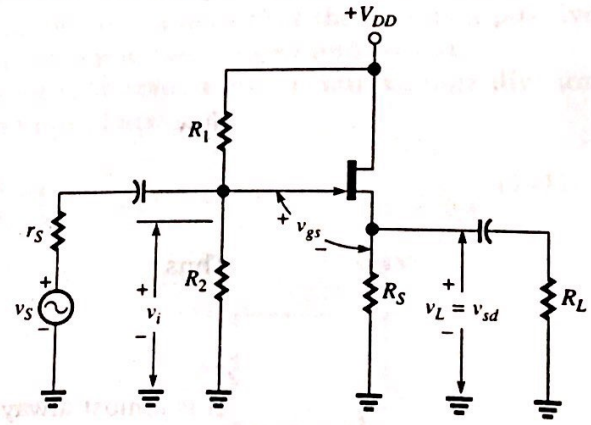


FIGURE 7–63 A common-drain JFET amplifier

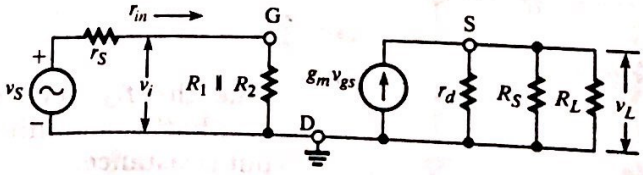


FIGURE 7–64 The small-signal equivalent circuit for the common-drain amplifier

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$$= g_m v_i(r_d \| R_S \| R_L) - g_m v_L(r_d \| R_S \| R_L)$$

$$v_L + g_m v_L(r_d \| R_S \| R_L) = g_m v_i(r_d \| R_S \| R_L)$$

Solving for $v_L/v_i$, we obtain

$$\frac{v_L}{v_i} = \frac{g_m(r_d \| R_S \| R_L)}{1 + g_m(r_d \| R_S \| R_L)} \tag{7–118}$$

It is clear from equation 7–118 that the voltage gain of the common-drain configuration is always less than 1. Note that there is no phase inversion between input and output. When $g_m(r_d \| R_S \| R_L) \gg 1$ (often the case), equation 7–118 shows

$$\frac{v_L}{v_i} \approx 1 \tag{7–119}$$

In other words, the load voltage is approximately the same as the input voltage, in magnitude and phase, and we say that the output *follows* the input. For this reason, the common-drain amplifier is called a *source follower.*

The input resistance of the source follower can be seen from Figure 7–63 to be the same as it is for a common-source amplifier:

$$r_{in} = R_1 \| R_2 \tag{7–120}$$

Similarly, $r_{in}$ is the same as it is for a common-source amplifier when the other bias arrangements are used. When the voltage division between signal-source resistance and $r_i$ is taken into account, we find the overall voltage gain to be

$$\frac{v_L}{v_S} = \left(\frac{r_{in}}{r_S + r_{in}}\right)\left[\frac{g_m(r_d \| R_S \| R_L)}{1 + g_m(r_d \| R_S \| R_L)}\right] \tag{7–121}$$

The output resistance of the source follower ($r_{out}$), looking from $R_L$ toward the source terminal, is $R_S$ in parallel with the resistance "looking into" the JFET at the source terminal. The resistance looking into the JFET at the source terminal can be found using equation 7–118. Because we are looking to the left of $R_S$ and $R_L$, the parallel combination of those resistances is not relevant in the equation. Substituting $r_d$ for $r_d \| R_S \| R_L$, equation 7–118 becomes

$$A_v = \frac{v_o}{v_i} = \frac{g_m r_d}{1 + g_m r_d}$$

Now,

$$r_o = \frac{v_o}{i_o} = \frac{A_v v_i}{i_o} = \frac{A_v}{g_m} = \frac{r_d}{1 + g_m r_d}$$

Thus,

$$r_{out} = R_S \left\| \left(\frac{r_d}{1 + g_m r_d}\right)\right. \tag{7–122}$$

It is almost always true that $g_m r_d \gg 1$, so (7–122) reduces to

$$r_{out} \approx R_S \left\| \left(\frac{1}{g_m}\right)\right. \tag{7–123}$$

Like the BJT emitter follower, the source follower is used primarily as a buffer amplifier because of its large input resistance and small output resistance.

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**EXAMPLE 7–18**

The JFET in Figure 7–65 has $g_m = 5 \times 10^{-3}$ S and $r_d = 100$ kΩ. Find

1. the input resistance,
2. the voltage gain, and
3. the output resistance of the amplifier stage.

**Solution**

1. $r_{in} = R_1 \| R_2 = (1.8\ \text{M}\Omega) \| (470\ \text{k}\Omega) = 372.7\ \text{k}\Omega$.
2. Since $r_d \| R_S \| R_L = (100\ \text{k}\Omega) \| (1.5\ \text{k}\Omega) \| (3\ \text{k}\Omega) = 990\ \Omega$, we have, from equation 7–121

$$\frac{v_L}{v_S} = \left(\frac{372.7\ \text{k}\Omega}{10\ \text{k}\Omega + 372.7\ \text{k}\Omega}\right)\left[\frac{(5 \times 10^{-3}\ \text{S})(990\ \Omega)}{1 + (5 \times 10^{-3}\ \text{S})(990\ \Omega)}\right) = 0.81$$

3. From equation 7–122,

$$r_{out} = (1.5\ \text{k}\Omega) \left\| \left(\frac{100\ \text{k}\Omega}{1 + (5 \times 10^{-3}\ \text{S})(100\ \text{k}\Omega)}\right)\right.$$
$$= (1.5\ \text{k}\Omega) \| (199.6\ \Omega) = 176.2\ \Omega$$

Note that the approximation for $r_o$ (equation 7–123) gives a nearly equal result:

$$r_{out} \approx R_S \| (1/g_m) = (1.5\ \text{k}\Omega) \| 200 = 176.5\ \Omega$$

## Common-Gate Amplifier

Figure 7–66 shows a common-gate amplifier and its small-signal equivalent circuit. We see that the load voltage is developed across the parallel combination of $r_d$, $R_D$, and $R_L$:

$$v_L = -\, i_d r_L = g_m v_{gs} r_L \tag{7–124}$$

where $r_L = R_D \| R_L$. The voltage gain $v_L/v_{gs}$ is, therefore,

$$\frac{v_L}{v_{gs}} = \frac{g_m v_{gs} r_L}{v_{gs}} = g_m r_L \tag{7–125}$$

We see that the magnitude of this gain is calculated in the same way as it is for the common-source amplifier. Note, however, that the gain is a positive quantity, so there is no phase inversion between input and output.

When signal-source resistance $r_S$ is taken into account, voltage division occurs at the input, and the gain $v_L/v_S$ becomes

$$\frac{v_L}{v_S} = \left(\frac{r_{in}}{r_S + r_{in}}\right) g_m r_L \tag{7–126}$$

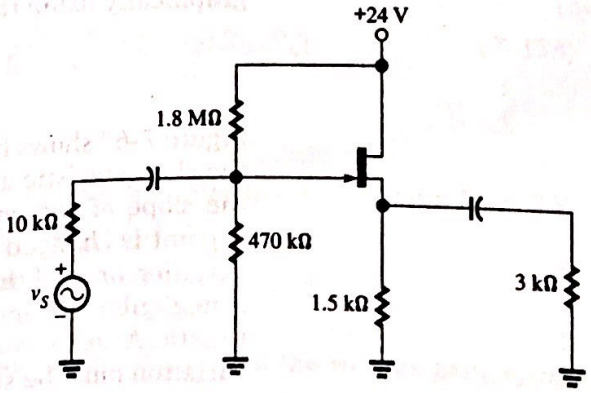


**FIGURE 7–65** (Example 7–18)

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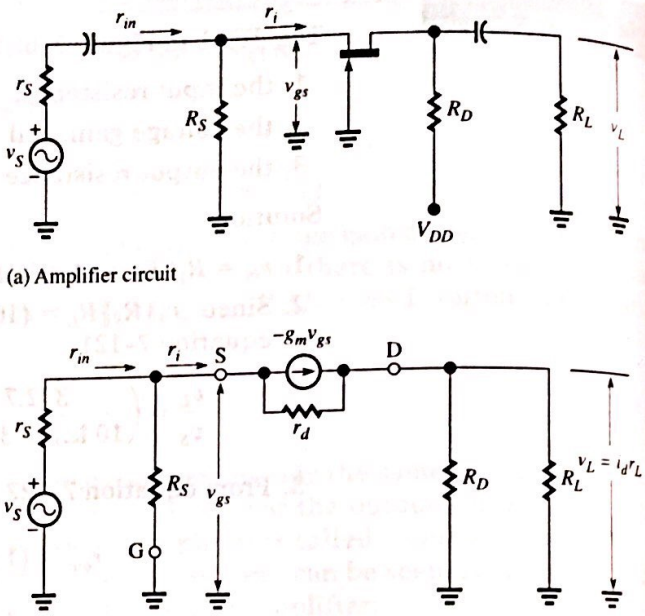
FIGURE 7–66 The common-gate amplifier




The input resistance, $r_{in}$, is the parallel combination of $R_S$ and the resistance $r_i$ looking into the source terminal. As can be seen in Figure 7–66(b),

$$r_i = \frac{v_{gs}}{i_s} = \frac{v_{gs}}{i_d} = \frac{v_{gs}}{g_m v_{gs}} = \frac{1}{g_m} \tag{7–127}$$

Therefore,

$$r_{in} = r_i \| R_S = \frac{1}{g_m} \Big\| R_S \tag{7–128}$$

The input resistance of the common-gate amplifier is much smaller than its common-source and common-drain counterparts. Using the typical values $g_m = 4000\ \mu S$ and $R_S = 500\ \Omega$, we find $r_{in} = (1/4000\ \mu S) \| (500\ \Omega) = (250\ \Omega) \| (500\ \Omega) = 166.7\ \Omega$. To avoid the large reduction in voltage gain predicted by equation 7–126 when such a small value of $r_{in}$ is used, it is clear that signal-source resistance $r_S$ must be very small.

## 7–8 SMALL-SIGNAL MOSFET AMPLIFIERS

The most convenient small-signal model for a MOSFET, like that of a JFET, incorporates the transconductance of the device.

The transconductance of the *enhancement*-type MOSFET can be found graphically using the transfer characteristic and the definition:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{V_{DS} = \text{constant}} \tag{7–129}$$

Figure 7–67 shows how $g_m$ is computed as the slope of a line drawn tangent to the characteristic at the operating or Q-point. It is clear from the figure that the slope of the characteristic, and hence the value of $g_m$, changes as the Q-point is changed. Therefore, small-signal analysis requires that the signal variation around the Q-point be confined to a limited range over which there is negligible change in $g_m$, i.e., to an essentially linear segment of the characteristic. Also, to ensure that the device is operated within its active region, the variation must be such that the following inequality is always satisfied:

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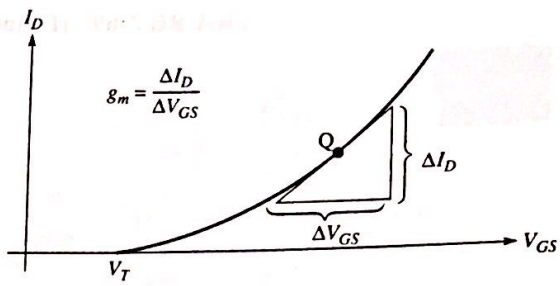
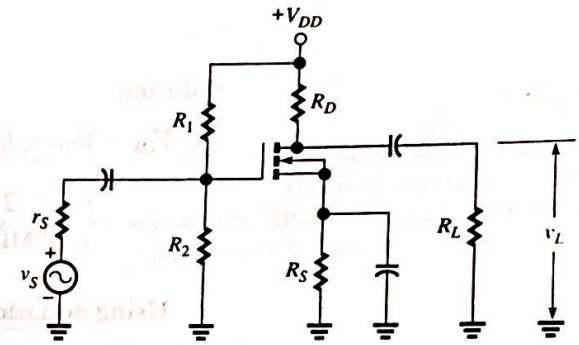
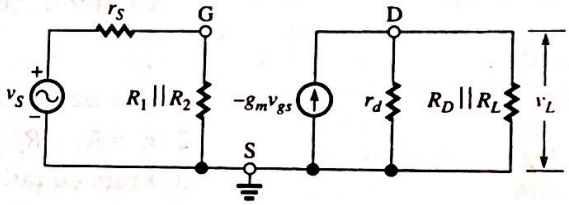



**FIGURE 7–67** The transconductance of an enhancement MOSFET is the slope of a line drawn tangent to the transfer characteristic at the Q-point




(a) An $n$-channel enhancement MOSFET (NMOS) amplifier with voltage-divider bias




(b) The small-signal equivalent circuit of (a)

**FIGURE 7–68** A common-source NMOS amplifier and its equivalent circuit

$$|V_{DS}| > |V_{GS} - V_T| \tag{7–130}$$

It can be shown that under small-signal conditions the transconductance of an enhancement MOSFET can be determined from

$$g_m = \beta(V_{GS} - V_T) \text{ siemens} \tag{7–131}$$

Figure 7–68 shows a common-source enhancement MOSFET amplifier and its small-signal equivalent circuit. The MOSFET is biased using the voltage-divider method (Figure 5–38), where

$$r_i = R_1 \parallel R_2 \tag{7–132}$$

$$\frac{v_L}{v_S} = \left(\frac{R_1 \parallel R_2}{r_S + R_1 \parallel R_2}\right)(-g_m)(r_d \parallel R_D \parallel R_L) \tag{7–133}$$

**EXAMPLE 7–19**

The MOSFET shown in Figure 7–69 has the following parameters: $V_T = 2$ V, $\beta = 0.5 \times 10^{-3}$, $r_d = 75$ kΩ. It is biased at $I_D = 1.93$ mA.

1. Verify that the MOSFET is biased in its active region.
2. Find the input resistance.
3. Draw the small-signal equivalent circuit and find the voltage gain, $v_L/v_S$.

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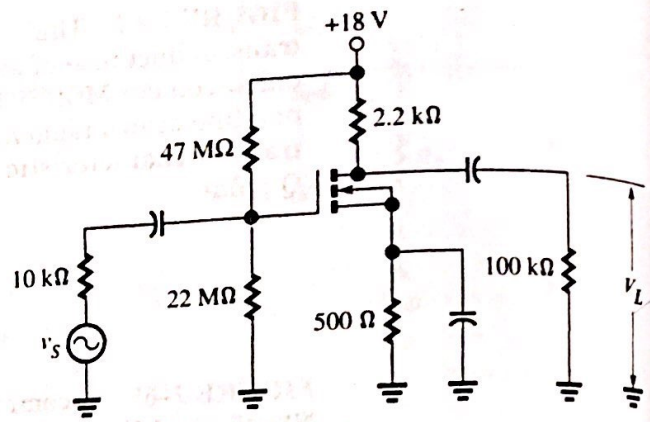
FIGURE 7–69 (Example 7–19)




**Solution**

1. $V_{DS} = V_{DD} - I_D(R_D + R_S) = 18\text{ V} - (1.93\text{ mA})(2.2\text{ k}\Omega + 500\ \Omega) = 12.78\text{ V}$

$$V_G = \left(\frac{2.2\text{ M}\Omega}{4.7\text{ M}\Omega + 2.2\text{ M}\Omega}\right)18\text{ V} = 5.74\text{ V}$$

Using equation 5–14 to find $V_{GS}$, we have

$$V_{GS} = 5.74\text{ V} - (1.93\text{ mA})(500\ \Omega) = 4.78\text{ V}$$
$$|V_{GS} - V_T| = |4.78 - 2| = 2.78\text{ V}$$

Therefore, condition 7–130 is satisfied:

$$12.78 = |V_{DS}| > |V_{GS} - V_T| = 2.78$$

and we conclude that the MOSFET is biased in its active region.

2. $r_i = R_1 \parallel R_2 = (4.7\text{ M}\Omega) \parallel (2.2\text{ M}\Omega) = 1.5\text{ M}\Omega.$
3. From equation 7–131

$$g_m = 0.5 \times 10^{-3}(4.78\text{ V} - 2\text{V}) = 1.4 \times 10^{-3}\text{ S}$$

The small-signal equivalent circuit is shown in Figure 7–70. From equation 7–133

$$\frac{v_L}{v_S} = \left(\frac{15 \times 10^6}{10 \times 10^3 + 15 \times 10^6}\right)$$
$$\times (-1.4 \times 10^{-3})[(75 \times 10^3) \parallel (2.2 \times 10^3) \parallel (100 \times 10^3)]$$
$$= (0.999)(-1.4 \times 10^{-3})(2.09 \times 10^3) = -2.92$$

FIGURE 7–70 (Example 7–19) The small-signal equivalent circuit of Figure 7–69

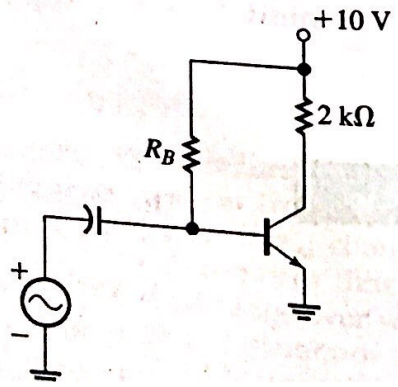



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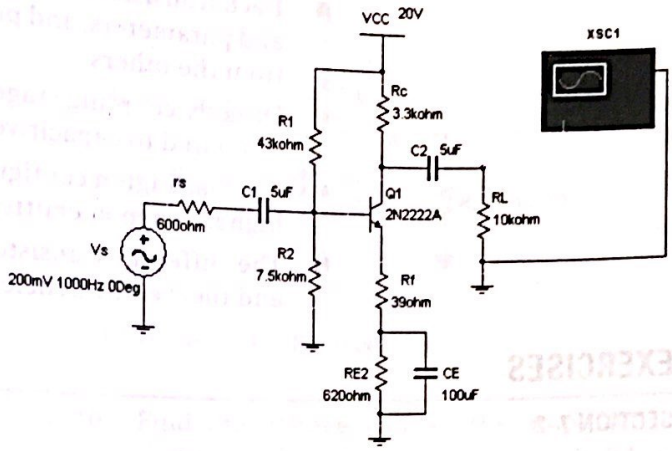
FIGURE 7–71 Common-emitter stage from Example 7–7




Like JFETs, MOSFETs can be operated in common-drain and common-gate configurations. Because the JFET and MOSFET small-signal models are identical, the gain and impedance equations are also identical, MOSFET amplifier circuits are discussed in greater detail in Chapter 8.

## 7–9 MULTISIM EXERCISE

We will test the design described in Example 7–7. Figure 7–71 shows the circuit as drawn on the EWB Multisim schematic editor. Note that the input voltage is 10 mV peak. Before you run the simulation, set up the oscilloscope to 200 mV/div for the vertical scale and 1 ms/div for the horizontal scale.

Observe the output waveform on the oscilloscope. You should read about 440 mV of peak voltage, which corresponds to an overall gain of 44 in magnitude. We had designed the amplifier stage for a gain of 45.

To obtain the maximum output voltage swing, change the peak value of the input voltage to 200 mV peak, the vertical scale to 5 V/div, run the simulation again, and observe the clipping of the waveform occurring on the lower side only. This means that the Q-point is not on the center of the ac line as expected; it is actually slightly above the center. Increase the input voltage to 220 mV and you will see that the upper side just begins to clip. Increase the input voltage to 300 mV, and both sides will be clipped. Calculate the expected maximum output voltage swing and verify that it agrees closely with the measured value.

If you measure the actual collector current, you will see that it is slightly larger than the nominal value used in the design. By changing $R_2$ to 6.8 kΩ, the collector current will be reduced slightly and the clipping will occur with more symmetry.

## SUMMARY

This chapter presented detailed information regarding transistor amplifiers of both bipolar junction and field-effect types. Emphasis in the use of models was consistently present throughout the chapter. At the end of this chapter the student should have learned the following concepts:

- Transistors must be properly biased in the center of their active region before they can be used as amplifiers.
- Small-signal voltage or current refers to a signal level that will confine the operation of an amplifier to a relatively small portion of its linear operation region.
- The localization of the Q-point has a direct effect on the linearity and maximum output swing of a transistor amplifier stage.

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- Each transistor configuration (CE, CB, CC, CS, CG, CD) has its own model and parameters, and presents unique characteristics that distinguishes it from the others.
- Directly coupling stages reduces the number of required components as compared to capacitively coupled stages.
- The Darlington configuration can be seen as a super-beta transistor with higher common-emitter input resistance.
- The different transistor models have many characteristics in common, and their equivalencies can be easily established.

## EXERCISES

### SECTION 7–2

***Analysis of the CE Amplifier***

7–1. Suppose the signal source voltage $v_S$ in Figure 7–72 causes the transistor base current to vary sinusoidally between 10 μA and 50 μA. Assuming that the transistor has the output characteristics shown in Figure 7–76, what is the total (peak-to-peak) variation in $V_{CE}$ and the total variation in $I_C$?

7–2. Assuming that the transistor shown in Figure 7–73 has the input characteristics shown in Figure 7–75 and the output characteristics shown in Figure 7–76, find

(a) $V_{CE}$ and $I_C$ at the Q-point; and

(b) the voltage gain.

7–3. If $R_B$ in Figure 7–73 is changed to 1.934 MΩ, what is the maximum peak-to-peak output voltage without clipping?

7–4. At $V_{CE}$ = 10 V, the CE output characteristics of a certain transistor show that $I_C$ has the values listed in the following table for different values of $I_B$:

| $I_B$ | $I_C$ |
|---|---|
| 10 μA | 0.5 mA |
| 15 μA | 0.75 mA |
| 20 μA | 1.00 mA |
| 25 μA | 1.25 mA |
| 30 μA | 2.10 mA |
| 35 μA | 3.15 mA |
| 40 μA | 4.00 mA |

At the quiescent voltage $V_{CE}$ = 10 V, what maximum range of $I_B$ values results in the output being a linear reproduction of the input?

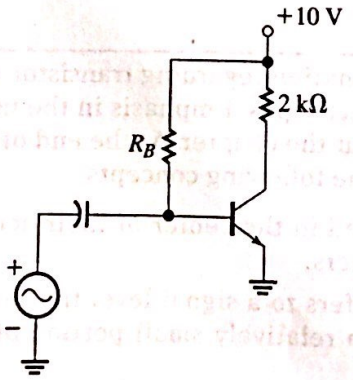


FIGURE 7–72 (Exercise 7–1)

7–5. Show that equations 7–14 and 7–15 correctly give the intercepts of a dc load line when $R_C$ is substituted for $r_L$. (This shows that the dc load line is a special case of the ac load line, the case where $R_L = \infty$.)

7–6. The transistor shown in Figure 7–74 has the CE output characteristics shown in Figure 7–76.

(a) Plot the dc and ac load lines on the output characteristics.

(b) Determine the voltage gain of the circuit if a 24-mV p-p input voltage causes a 20-μA p-p variation in base current.

7–7. Repeat Exercise 7–6 when $R_L$ is changed to 10.5 kΩ.

### SECTION 7–3

***Amplifier Analysis Using Small-Signal Models***

7–8. The silicon transistor in the amplifier stage shown in Figure 7–77 has an α of 0.99 and collector resistance $r_c$ = 2.5 MΩ. Find

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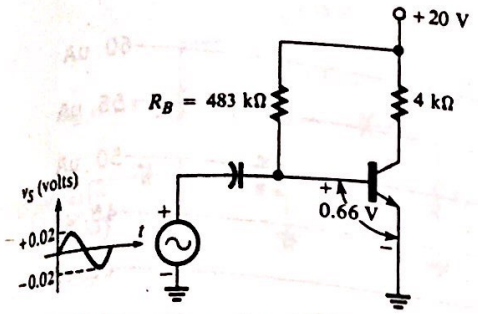



FIGURE 7–73 (Exercises 7–2 and 7–3)

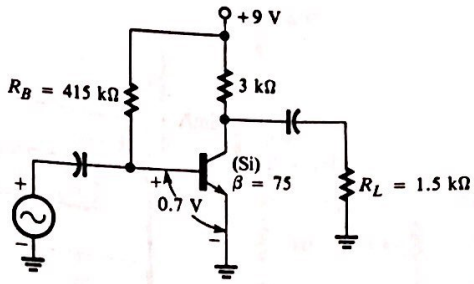



FIGURE 7–74 (Exercise 7–6)

(a) the input resistance of the amplifier stage,

(b) the output resistance of the amplifier stage,

(c) the voltage gain of the amplifier, and

(d) the current gain of the amplifier.

7–9. The silicon transistor in the amplifier stage shown in Figure 7–78 has a collector resistance $r_c$ = 1.5 MΩ. Find

(a) the input resistance of the amplifier stage,

(b) the output resistance of the amplifier stage, and

(c) the rms load voltage $v_L$.

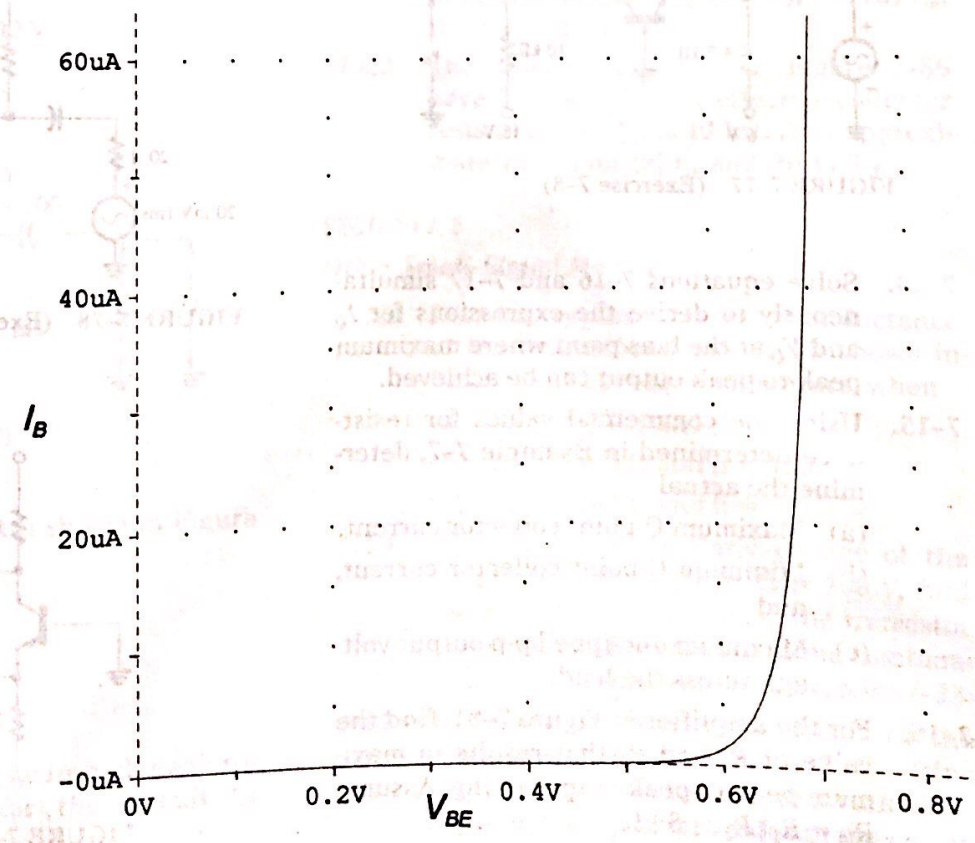
7–10. Find the voltage gain of the amplifier shown in Figure 7–79. The transistor is germanium.

7–11. What value of $R_L$ in the amplifier of Exercise 7–10 would result in a voltage gain of 100?

7–12. Find the rms load voltage $v_L$ in the amplifier of Figure 7–80 when $R_L$ = (a) 1 kΩ, (b) 10 kΩ, and (c) 100 kΩ. Assume that β = 100.

7–13. Find the maximum peak-to-peak output voltage swing for each value of $R_L$ in Exercise 7–12.

FIGURE 7-75 (Exercise 7–2)

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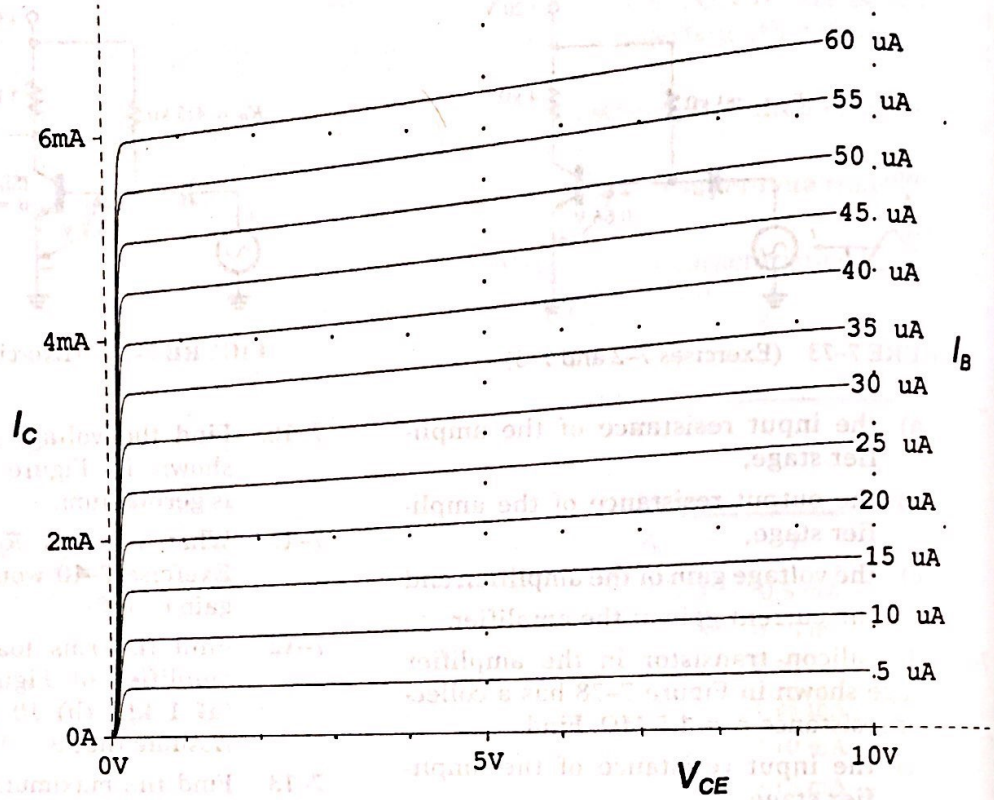


FIGURE 7–76 (Exercise 7–6)

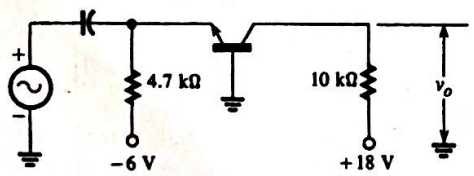


FIGURE 7–77 (Exercise 7–8)

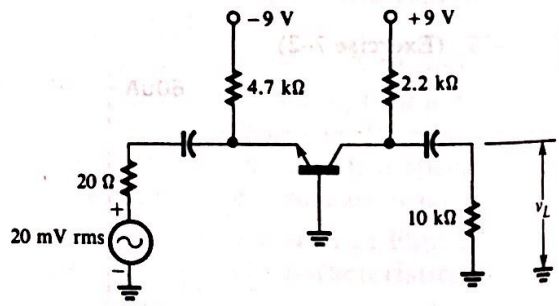


FIGURE 7–78 (Exercise 7–9)

7–14. Solve equations 7–16 and 7–17 simultaneously to derive the expressions for $I_Q$ and $V_Q$ at the bias point where maximum peak-to-peak output can be achieved.

7–15. Using the commercial values for resistance determined in Example 7–7, determine the actual

(a) Maximum Q-point collector current,

(b) Minimum Q-point collector current, and

(c) Maximum unclipped p-p output voltage across the load.

7–16. For the amplifier in Figure 7–81, find the value of $R_1$ and $R_2$ that results in maximum peak-to-peak output swing. Assume $R_B = R_1 \| R_2 = 8\ \text{k}\Omega$.

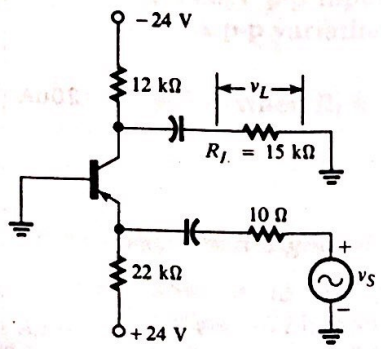


FIGURE 7–79 (Exercise 7–10)

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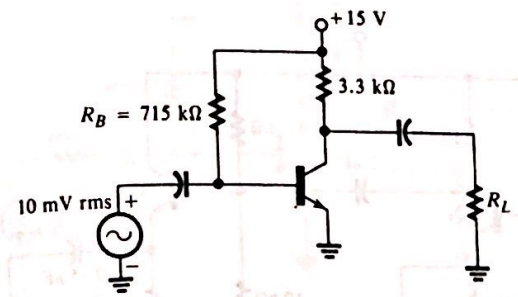


FIGURE 7–80 (Exercise 7–12)

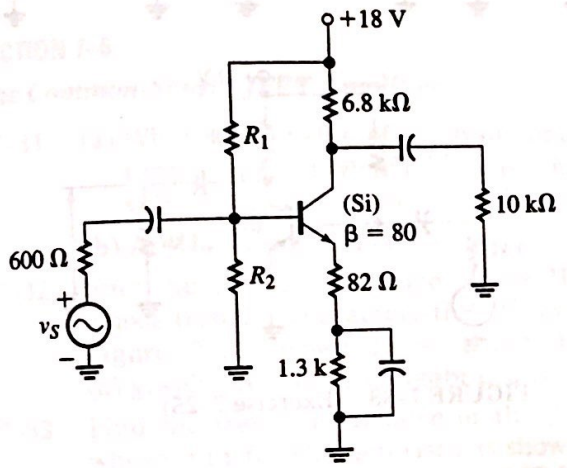


FIGURE 7–81 (Exercise 7–16)

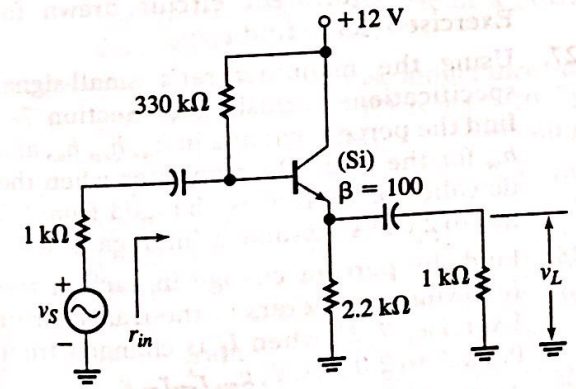


FIGURE 7–82 (Exercise 7–17)

7–17. For the amplifier circuit shown in Figure 7–82, find
(a) $r_{in}$
(b) $r_{out}$
(c) $A_v$ and
(d) $A_{vs}$

7–18. Find the maximum unclipped peak-to-peak load voltage for the circuit in Figure 7–82.

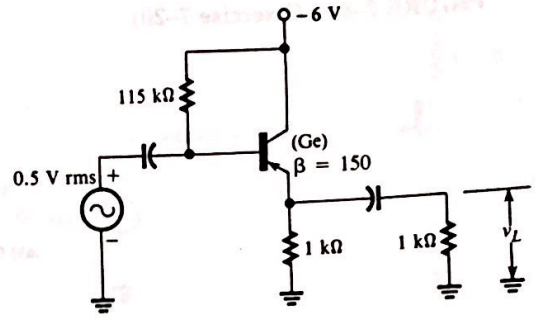


FIGURE 7–83 (Exercise 7–19)

7–19. Find the output voltage $v_L$ in Figure 7–83.

7–20. The transistors in Figure 7–84 have the following parameter values:
$Q_1$: $r'_{e1}$ = 12 Ω, $\beta_1$ = 200, $r_{c1}$ = 2 MΩ
$Q_2$: $r'_{e2}$ = 10 Ω, $\beta_2$ = 100
Find the midband values of
(a) the voltage gain $v_L/v_S$; and
(b) the current gain $i_L/i_S$.

## SECTION 7–4
### *Direct Coupling*

7–21. The silicon transistors in Figure 7–85 have $\beta_1$ = 120 and $\beta_2$ = 110. Find (a) $r_{in}$, (b) $v_L/v_S$, and (c) $i_L/i_S$.

7–22. The silicon transistors in Figure 7–86 have $\beta_1 = \beta_2$ = 50. The effective collector resistance (at $Q_2$) is 10 kΩ. Find approximate values for (a) $r_{in}$ and (b) $V_L/V_S$.

## SECTION 7–5
### *Other Small-Signal Models*

7–23. Find the (approximate) transconductance of the transistor in the circuit shown in Figure 7–87 at room temperature, when
(a) $R_B$ = 330 kΩ and β = 50,
(b) $R_B$ = 330 kΩ and β = 150, and
(c) $R_B$ = 220 kΩ and β = 50.

7–24. Assuming that the Early voltage of the transistor in Exercise 7–23 is 100 V, find the output resistance of (a) the transistor and (b) the stage for each of the combinations of parameters given in Exercise 7–23.

7–25. Draw the ac equivalent circuit of the amplifier, shown in Figure 7–88, using the hybrid-π model for the transistor. Label all component values in the circuit

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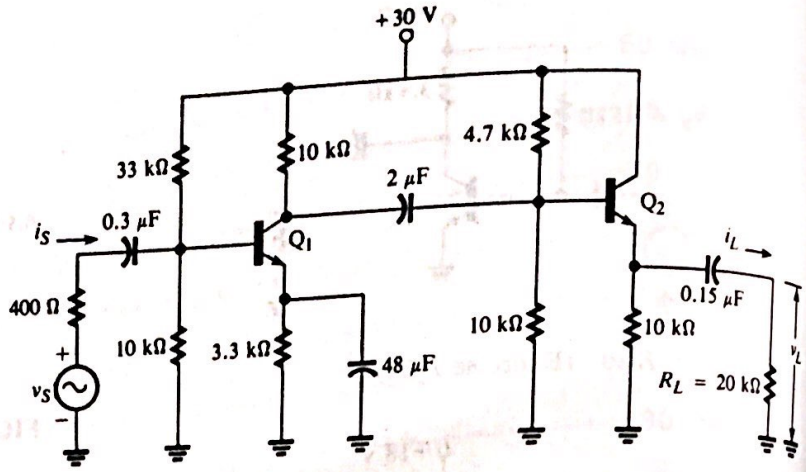
FIGURE 7–84 (Exercise 7–20)



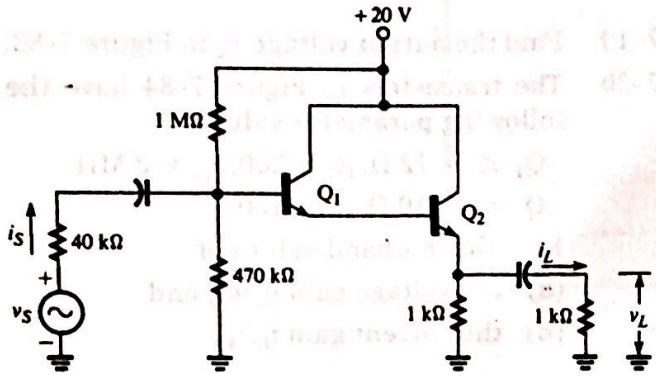




FIGURE 7–85 (Exercise 7–21)

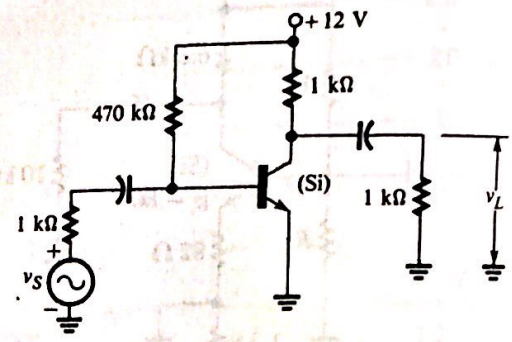



FIGURE 7–88 (Exercise 7–25)

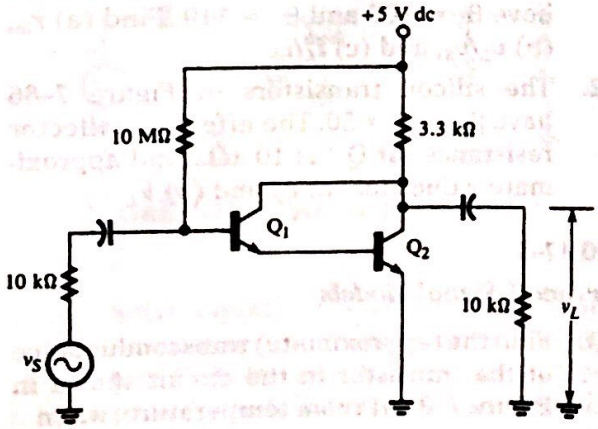



FIGURE 7–86 (Exercise 7–22)

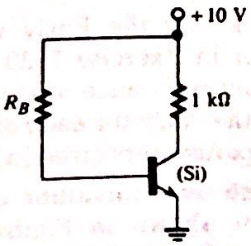



FIGURE 7–87 (Exercise 7–23)

and the model. Assume that $\beta = 100$ and $V_A = 100$ V.

7–26. Use the equivalent circuit drawn for Exercise 7–25 to find $v_L/v_S$.

7–27. Using the manufacturer's small-signal specifications furnished in Section 7-5 find the percent change in $h_{fe}$, $h_{re}$, $h_{ie}$, and $h_{oe}$ for the 2N2222A transistor when the dc collector current is changed from 0.5 mA to 2.0 mA. Assume a "high-gain" unit.

7–28. Find the percent change in each of the following parameters of the transistor in Exercise 7–27 when $I_C$ is changed from 0.5 mA to 2.0 mA: $\beta$, $g_m$, $r'_e$, $r_\pi$, $g_o$.

7–29. A circuit has been designed using the 2N2221A transistor to amplify 1-kHz signals. After each unit is manufactured, the bias point of the transistor is adjusted so that $I_C = 1$ mA and $V_{CE} = 10$ V. What are the ranges of values of $\beta$ and $g_m$ that could be expected for the transistors that are used in the circuit?

7–30. The transistor shown in Figure 7–89 has the following $h$ parameters: $h_{fe} = 120$, $h_{ie} = 2.2$ kΩ, $h_{oe} = 40$ μS, and $h_{re} = 6 \times 10^{-4}$. Draw the complete ac equivalent circuit and find the value of the load voltage $v_L$.

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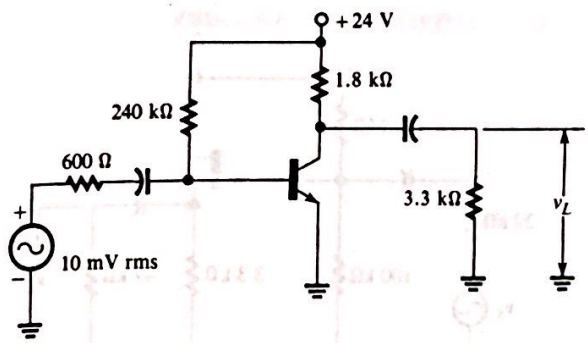


FIGURE 7–89 (Exercise 7–30)

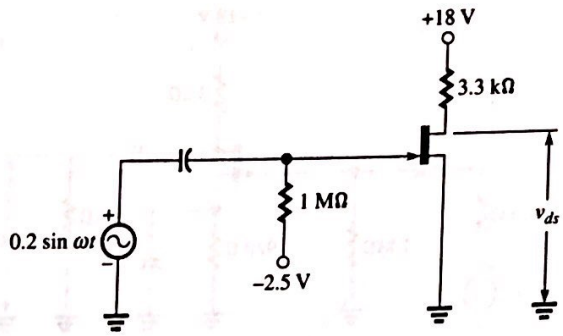


FIGURE 7–90 (Exercise 7–37)

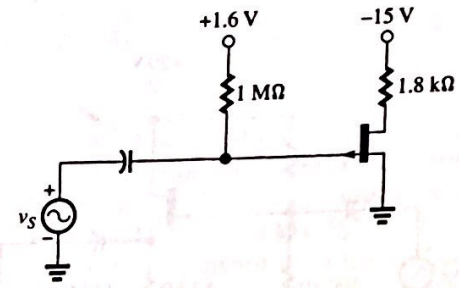


FIGURE 7–91 (Exercise 7–38)

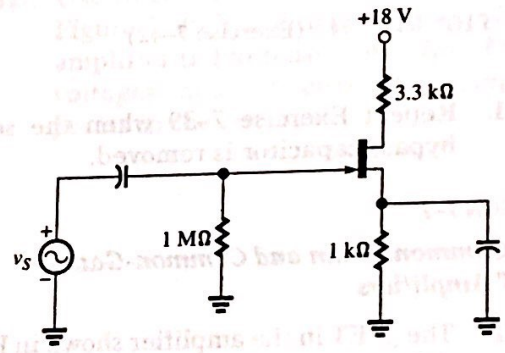


FIGURE 7–92 (Exercise 7–39)

## SECTION 7–6

### *The Common-Source JFET Amplifier*

7–31. (a) What is the value of the transconductance of a JFET when its gate-to-source voltage equals its pinch-off voltage?

(b) At what value of $I_D$ does $g_m = 0$?

7–32. Find the transconductance of the JFET whose transfer characteristic is shown in Figure 7–55, when $I_D = 1$ mA both (a) graphically and (b) algebraically.

7–33. Find the transconductance of the JFET whose transfer characteristic is shown in Figure 7–55, when $V_{GS} = -0.5$ V both (a) graphically and (b) algebraically.

7–34. Use equation 7–100 and the equation of the transfer characteristic of a JFET to derive equation 7–101.

7–35. The maximum transconductance of a certain *n*-channel JFET is $9.8 \times 10^{-3}$ S. If $I_{DSS} = 18$ mA, what is its pinch-off voltage?

7–36. The following measurements were taken from a curve-tracer display of the output characteristics of a *p*-channel JFET along the line $V_{GS} = +2.5$ V: $I_D = 4.2$ mA at $V_{DS} = -4.5$ V; $I_D = 4.3$ mA at $V_{DS} = -12$ V. What is the drain resistance at $V_{GS} = 2.5$ V?

7–37. The JFET in the amplifier shown in Figure 7–90 has $I_{DSS} = 16$ mA, $V_p = -4.5$ V, and $r_d = 80$ kΩ.

(a) Find the quiescent values of $I_D$ and $V_{DS}$.

(b) Find $g_m$.

(c) Draw the ac equivalent circuit.

(d) What is the peak value of the ac component of $v_{ds}$?

7–38. The JFET in the amplifier shown in Figure 7–91 has $I_{DSS} = 14$ mA, $V_p = 3$ V, and $r_d = 120$ kΩ.

(a) Find the quiescent values of $I_D$ and $V_{DS}$.

(b) Find $g_m$.

(c) Draw the ac equivalent circuit.

(d) Find the voltage gain.

7–39. The JFET in the amplifier shown in Figure 7–92 has $r_d = 75$ kΩ, $V_p = -3.6$ V, and $I_{DSS} = 9$ mA. The dc voltage drop across the 3.3-kΩ resistor is 6.38 V. Find the voltage gain of the amplifier.

7–40. The JFET in the amplifier shown in Figure 7–93 has $r_d = 60$ kΩ, $V_p = 3.9$ V, and $I_{DSS} = 10$ mA. The quiescent value of $V_{DS}$ is −9.24 V. Find the voltage gain $v_L/v_S$.

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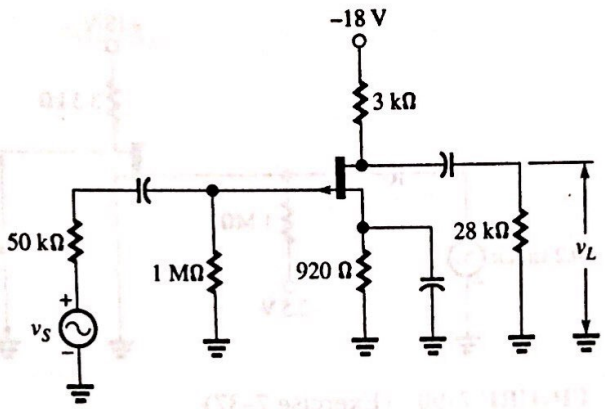


FIGURE 7–93 (Exercise 7–40)

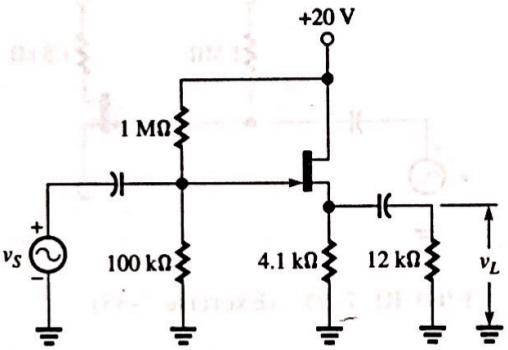


FIGURE 7–94 (Exercise 7–42)

7-41. Repeat Exercise 7–39 when the source bypass capacitor is removed.

**SECTION 7–7**

***The Common-Drain and Common-Gate JFET Amplifiers***

7–42. The JFET in the amplifier shown in Figure 7–94 has $g_m = 0.004$ S and $r_d = 90$ kΩ.

(a) Find the voltage gain $v_L/v_S$.

(b) Find the input resistance.

7–43. The JFET in the amplifier shown in Figure 7–95 has $g_m = 5200$ μS and $r_d = 80$ kΩ.

(a) Find the voltage gain $v_L/v_S$.

(b) Find the output resistance.

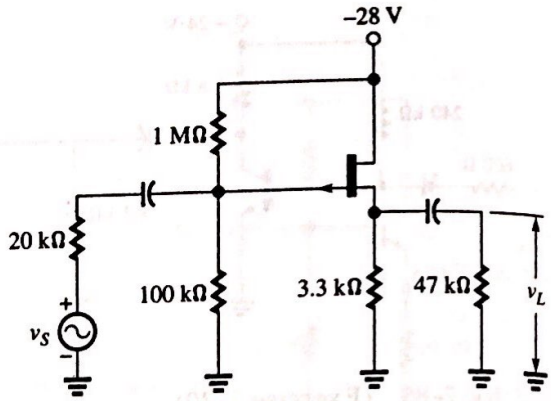


FIGURE 7–95 (Exercise 7–43)

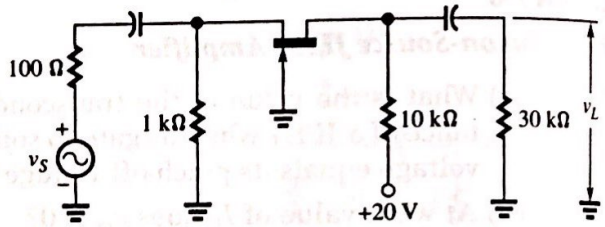


FIGURE 7–96 (Exercise 7–44)

7–44. The JFET in the amplifier in Figure 7–96 has $g_m = 3.58$ mS and $r_d = 100$ kΩ. Find the voltage gain $v_L/v_S$.

7–45. The amplifier in Figure 7–66(a) has $r_S = 50\ \Omega$, $R_S = 680\ \Omega$, $R_D = 2$ kΩ, $R_L = 4$ kΩ, and $V_{DD} = 15$ V. The pinch-off voltage of the JFET is −3.9 V and the saturation current is 15 mA. The dc voltage drop across $R_D$ is 6.24 V. Find the voltage gain $v_L/v_S$. Drain resistance $r_d$ can be neglected.

**SECTION 7–8**

***Small-Signal MOSFET Amplifiers***

7–46. Graphically determine the transconductance of the MOSFET whose transfer characteristic is shown in Figure 7–97 when $V_{GS} = 7$ V.

7–47. Algebraically determine the transconductance of the MOSFET in Exercise 7–46 given that its β is $0.5 \times 10^{-3}$.

## SPICE EXERCISES

*Note:* In the exercises that follow, assume that all devices have their default values unless otherwise specified. The capacitor values and frequencies specified in these exercises are such that capacitive reactances are negligible and have no effect on amplifier performance.

7–48. Use SPICE to determine the quiescent point, voltage gain $v_L/v_S$, and current gain $i_L/i_S$ of the common-emitter amplifier shown in Figure 7–26. The transistor has a beta of 200. Component values are: $r_S = 1$ kΩ, $R_1 = 47$ kΩ, $R_2 = 8.2$ kΩ, $R_E = 470\ \Omega$, $R_C = 2.2$ kΩ, and $R_L = 10$ kΩ. Both coupling capacitors are 10 μF, and $V_{CC} = 18$ V. The analysis should be performed at 10 kHz.

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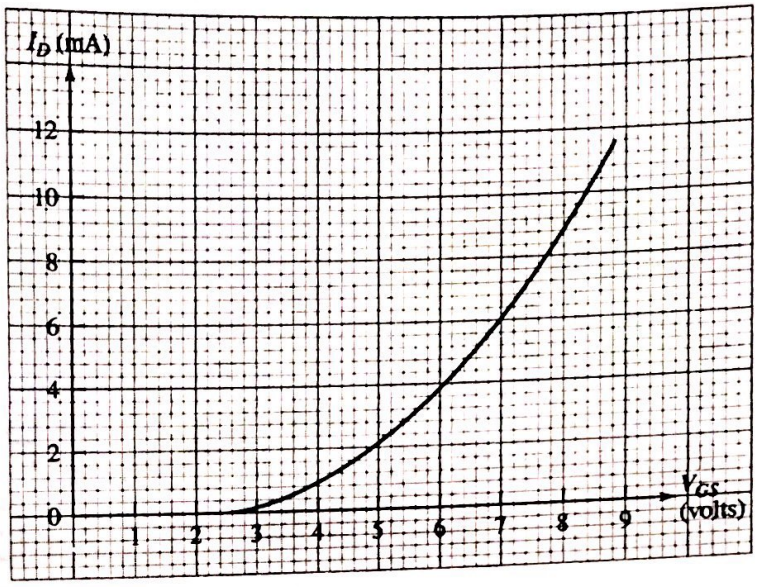
FIGURE 7–97 (Exercise 7–46)




7-49. Use SPICE to determine the quiescent point, voltage gain $v_L/v_S$, and current gain $i_L/i_S$ of the common-base amplifier shown in Figure 7–21(a). The transistor has a beta of 80. Component values are: $r_S$ = 100 Ω, $R_E$ = 2.2 kΩ, $R_C$ = 6.2 kΩ, and $R_L$ = 10 kΩ. The input coupling capacitor is 100 μF, and the output coupling capacitor is 10 μF. $V_{CC}$ = 36 V and $V_{EE}$ = 6 V. The analysis should be performed at 10 kHz.

7-50. Use SPICE to determine the quiescent point, voltage gain $v_L/v_S$, and current gain $i_L/i_S$ of the common-collector amplifier shown in Figure 7–29(a). The transistor has a beta of 150. Component values are: $r_S$ = 1 kΩ, $R_B$ = 180 kΩ, $R_E$ = 1 kΩ, and $R_L$ = 300 Ω. The input coupling capacitor is 10 μF, and the output coupling capacitor is 100 μF. $V_{CC}$ = 9 V.

7–51. Use SPICE to determine $r_i$ and $r_{in}$ (see Figure 7–29(b)) of the common-collector amplifier in Exercise 7–50. (*Hint*: Find ac voltages and currents at appropriate points in the circuit.)

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