Name	Faizan Azam, Muhammad Asad
Reg. #	2019-ee-381 2019-ee-383
Marks	

Experiment #6

Frequency Response in Common Emitter Amplifier

Objectives:

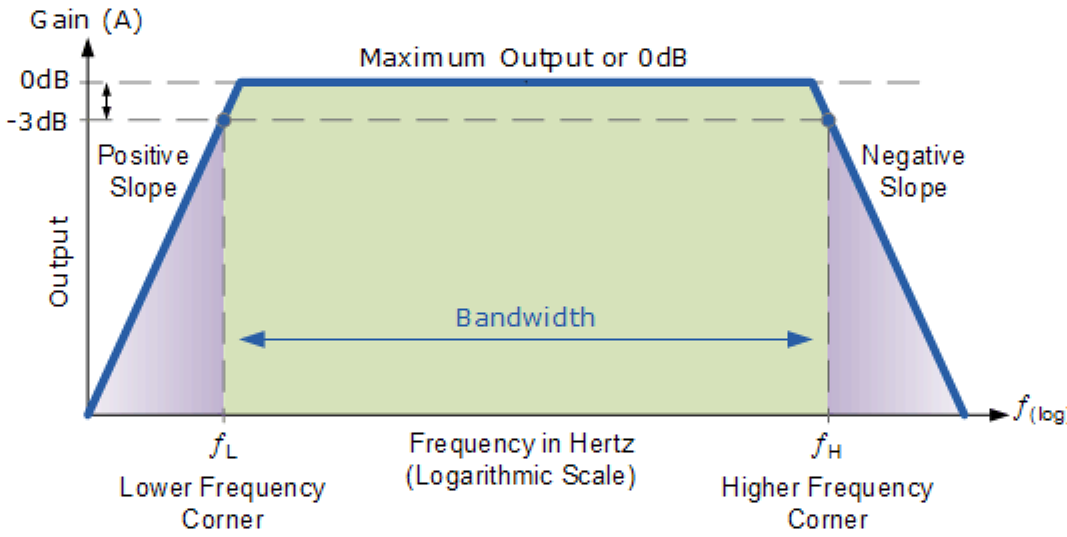
- To measure the higher and lower cutoff frequencies of common emitter amplifier
- To measure the bandwidth of common emitter amplifier

Apparatus:

Transistor - 2N3904 , Capacitors, Resistors, DMM, CRO, Function Generator, Jumpers, Connecting wires, DC source bread board.

Theory:

The voltage gain of an amplifier varies with signal frequency. It is because reactance of the capacitors in the circuit changes with signal frequency and hence affects the output voltage. The curve between voltage gain and signal frequency of an amplifier is known a frequency response. Figure 3-1-2 shows the frequency response of a typical CE amplifier.

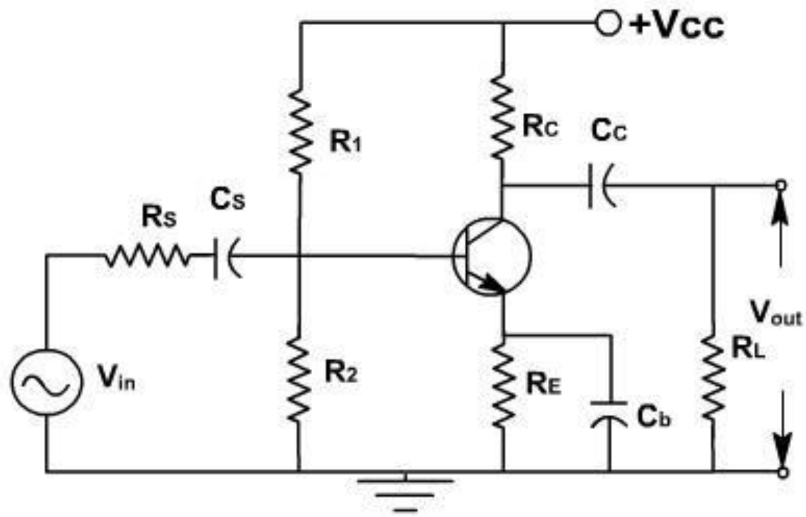


It is clear that the voltage gain drops off at low (< f_L) and high (> f_H) frequencies whereas it is uniform over mid-frequency range (f_L to f_H).

(i) *At low frequencies (< f_L)*, the reactance of coupling capacitor is quite high and hence very small part of signal will pass from amplifier stage to the load. Moreover, CE cannot shunt the RE effectively because of its large reactance at low frequencies. These two factors cause a falling of voltage gain at low frequencies.

(ii) *At high frequencies (> f_H)*, the reactance of C_2 is very small and it behaves as a short circuit. This increases the loading effect of amplifier stage and serves to reduce the voltage gain. Moreover, at high frequency, capacitive reactance of base-emitters junction is low which increases the base current. These reduce the current amplification factorβ. Due to these two reasons, the voltage gain drops off at high frequency.

(iii) *At mid frequencies (fL to fH),* the voltage gain of the amplifier is constant. The effect of coupling capacitor C_2 in this frequency range is such as to maintain a uniform voltage gain. Thus, as the frequency increases in this range, reactance of C_C decreases which tend to increase the gain. However, at the same time, lower reactance means higher almost cancel each other, resulting in a uniform fain at mid-frequency.



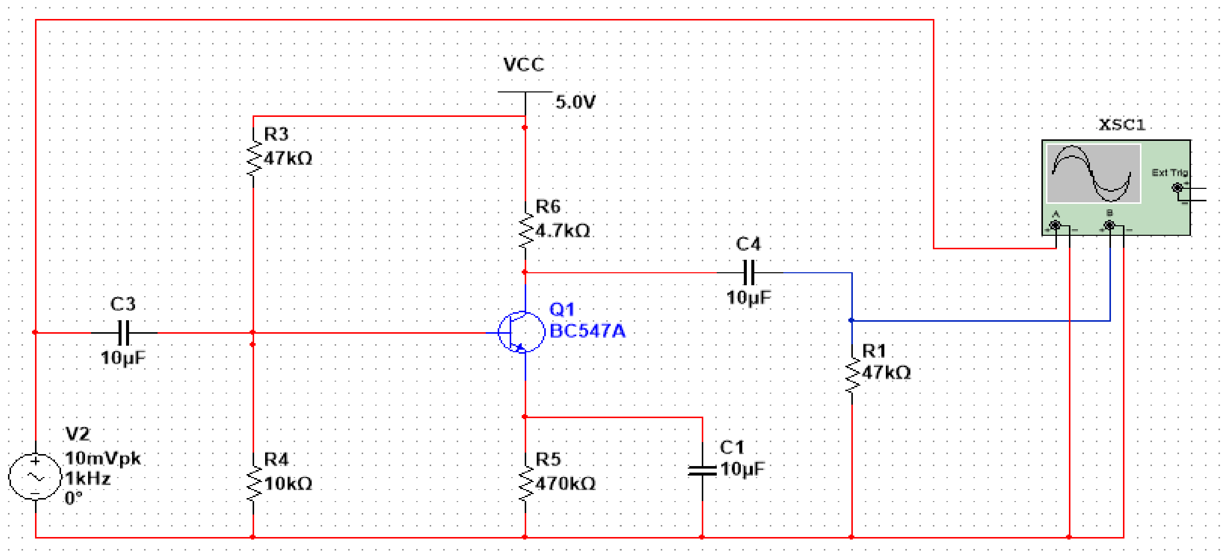
General procedure:

- Connect the circuit as shown in figure. Don't forget to connect the power supply bypass capacitor. Using the DMM measure the DC collector current and V_{be} .
- Switch the V_{out} probe to x1 position. Using a signal generator, set Vs so that V_{out} is 1V(p-p) sine wave, keeping the frequency at 10KHz.
- Decrease the frequency of the Vs. Note the lower cutoff frequency at which the V_{out}(p-p)= 0.707 x 1V(p-p).
- Switch the V_{out} probe x10 position, Adjust Vs so that V_{out} is 0.1V(p-p).
- Before measuring f_H make sure that collector and emitter terminals are one breadboard column apart from the base terminal, so that the wiring capacitance fo the breadboard doesn't affect the upper cutoff frequency. Increase thte frequency of the Vs. Note down the higher cutoff frequency at which the V_{out}(p-p)=0.707 x 1V(p-p).
- Restore the frequency of V back to 10KHz. Now we will observe the impact of wiring of the breadboard on the upper cutoff frequency. Plug out the transistor and reinsert is such that the collector, base and emitter terminals are in consecutive breadboard columns. Again measure the f_H .
- Remove the CE.
- Repeat the above steps.

Design:

Design the common emitter amplifier and find out the lower and upper cutoff frequencies. Also find out the Bandwidth

Circuit:



Calculations:

uation:-

For the above circu...

$\beta_{ac} = 125$

$V_B = \left(\frac{R_2}{R_1+R_2}\right) V_{cc} = \left(\frac{4.7k\Omega}{26.7k}\right) 10$

$V_E = V_B - 0.7 = 1.06V$

$I_E = \frac{V_E}{R_E} = \frac{1.06}{470\Omega} = 2.26mA$

$r'_e = \frac{25mV}{I_E} = 11.1\Omega$

$(Total) = R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac} r'_e$

$R_{in}(Total) = 600\Omega \parallel 2.2k\Omega \parallel 4.7k \parallel 125(11.1\Omega)$

$R_{in}(Total) = 3$

AV (mi

$= 99$

(1)

$C_{in} = C_{bc}(A_{v(mid)} + 1)$

$= (2.4pf)(100) = 240pf$

$C_{in(Total)} = C_{in} + C_{be}$

$= 240pf + 20pf$

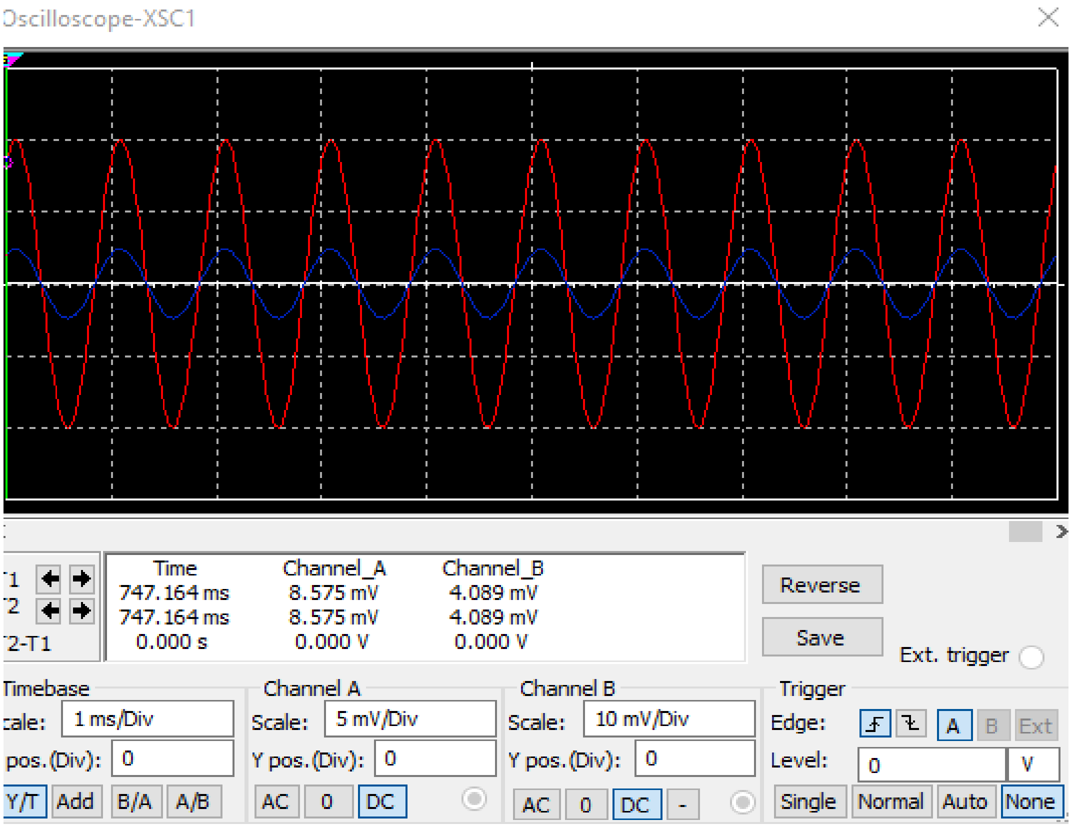
$= 260pf$

$$f_{cv(input)} = \frac{1}{2\pi (R_{in(Total)})(C_{in(out)})}$$

$$= \frac{1}{2\pi (378\Omega)(260pf)}$$

$f_{cv(input)} = 1.62\,MHz$

Frequency Graph:



Result:

Sr.#	$f_{L(th)}$	$f_{L(Prac)}$	$f_{H(th)}$	$f_{H(Prac)}$	$f_{bw(th)}$	$f_{bw(Prac)}$
01	500Hz	500Hz	80kHz	79.5KHz	50.7kHz	49.8kHz

Questions:

- **In an amplifier, which capacitor affects the low frequency gain?**

In capacitively coupled amplifiers, the coupling and bypass capacitors affect the low frequency cutoff. These capacitors form a high-pass filter with circuit resistances. A typical BJT amplifier has three high-pass filters

- **How is the high frequency gain of an amplifier limited?**
  At higher frequencies the coupling and bypass capacitors become effective AC shorts and don't affect an amplifiers response. Internal transistor junction capacitances, however, do come into play, reducing an amplifiers gain and introducing phase shift as the signal frequency increases.
- **Can coupling and bypass capacitor be neglected?**
  Circuits designed for DC or required to respond down to low frequencies including zero. (Coupling capacitors won't pass DC.)
  Circuits in which a DC response is acceptable even though not used. (Thus saving the cost of the coupling capacitor.)
  Circuits using other forms of coupling, e.g. transformer coupling, opto-coupling.
  Circuits where the gain is small at frequencies where unintended feedback is possible. (Bypass capacitors shunt signals at those frequencies away from the paths with gain. This prevents unwanted parasitic oscillations.)