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Reg. #	2019-EE-383
Marks	

Experiment # 10

Understanding of JK and flip flops and designing of counter circuits

Objective:

- *Designing of JK Flipflop in HDL Verilog*
- *Designing of synchronous counters*
- *Designing of asynchronous counters*

Apparatus:

Workstation Core 2 Duo, Uni*Tr@inLucas Nulle, SO4201-9T*Card, Jumpers wires, Power Supplies

Theory:

- **Counters**

Counters are circuits for continuous counting of electrical signals. Counting is generally performed by adding and storing values. Counters are mainly built using flip-flops.
The simplest pulse counter is a JK master-slave flip-flop (termed only 'flip-flop' in the following) whose inputs **J** and **K** are set to logical 1. The frequency applied to its C input is divided in the ratio **2:1**. The **counting states** of several flip-flops connected together are determined as follows:

$$m = 2^n$$

$$= 2$$

Accordingly, the **maximum count** is:

$k = m - 1$		
n	Number of flip-flops	
m	Number of counting states	
k	maximum count	

Consequently, **3** flip-flops have $2^3 = 8$ counting states and a maximum count $k = m - 1 = 8 - 1 = 7$.

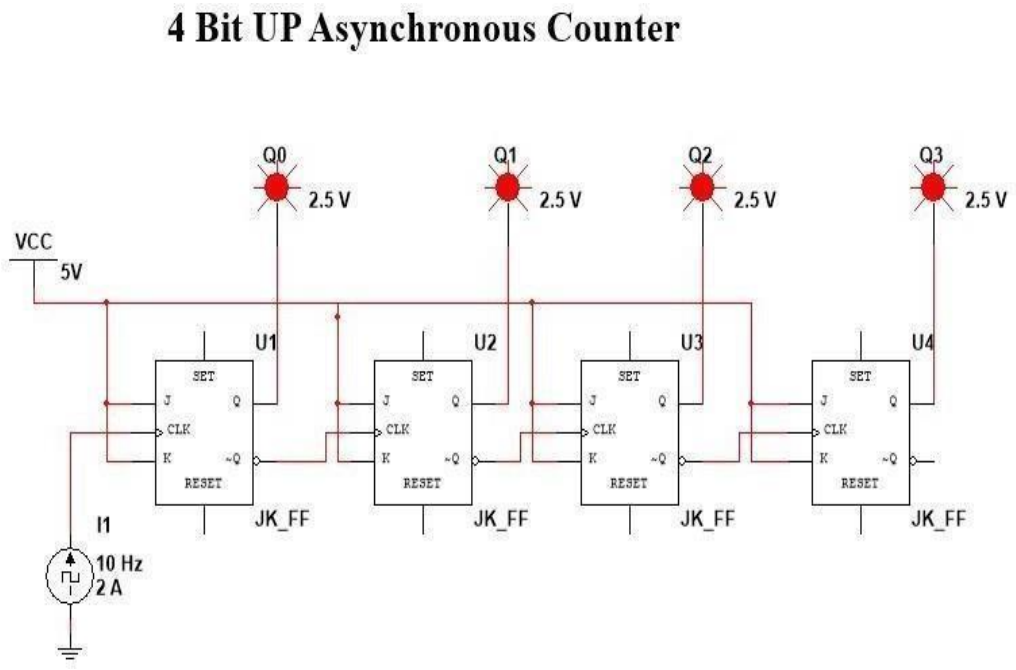
Counters with a large maximum count are not built using discrete components these days, as a large number of integrated modules are now available for this purpose. However, discrete counter circuits are still very suitable for promoting an understanding of the design of digital circuits. The flip-flop inputs influence the outputs Q1 and Q1' as follows:

• Clock input C1	:	Controls the dynamic response of the flip-flop.
• JK inputs	:	Control outputs Q1 and Q1'
	J = 0, K = 0	: Previous state
	J = 1, K = 0	: Set
	J = 0, K = 1	: Reset
	J = Q1, K = Q1'	: No change
	J = 1, K = 1	: Toggle
• Set input S1	:	Has priority. Uses a 0 signal to set the opposite output Q1 to 1 (irrespective of C1, J1, K1).
• Reset input R1	:	Has priority. Uses a 0 signal to set output Q1' to 1 (irrespective of C1, J1, K1). S1 and R1 should never receive a 0 signal simultaneously.

Exercise 1:

Design 4-bit asynchronous counter JK flipflop in Verilog HDL**.**

Circuit diagram:

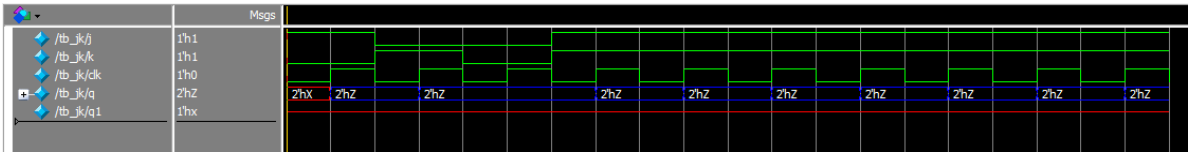


HDL Code:

```
module jk_ff(j,k,clk,q);
input j,k,clk;
output q;
reg q;
always @ (posedge clk)
case ({j,k})
2'b00 : q <= q;
2'b01 : q <= 0;
2'b10 : q <= 1;
2'b11 : q <= ~q;
endcase
endmodule
module tb_jk;
reg j;
reg k;
reg clk;
wire [1:0]q;
jk_ff jk0(j,k,clk,q);
jk_ff jk1(q,q,clk,q1);
initial
begin
clk=0;
end
always #5 clk = ~clk;
initial
begin

j = 1;
k = 0;
#10 j = 0;
k =1;
#10 j = 0;
k = 0;
#10 j = 1;
k = 1;
end
endmodule
```

Waveform:



What is the maximum count of the circuit?

In the 4 bit counter circuit so there are **4** flip-flops that is $2^4 = 16$ counting states.

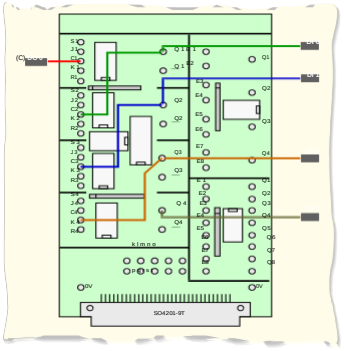
Maximum count which is denoted by k = m - 1 = 16 - 1 = 15.

Exercise 2:

Implement the circuit and fill the table below:

Experiment steps: Asynchronous counters

1. Connect the card to the Uni*Tr@in*-I as shown in the list of connections on the right.



Click on the image for a schematic representation of the wiring

Note: Inputs which are not connected (for example, J and K inputs) are set to a **high level** by pull-up resistors

List of connections

2. Open the following virtual instruments from the *Instruments* menu:
   - Function generator
   - Digital inputs

Settings

Function generator	Amplitude: 50% at 1:1 Frequency: 1Hz
Logic	
Power ON	

3. Start the function generator and observe the display of the digital inputs.

What do you observe after the circuit has been started up?

In the 4 Q outputs of the flip flops are initially 0000. When the rising edge of the clock pulse is applied to the U1, then the output Q0 will change to logic 1.

At next clock pulse will change the Q0 output to logic 0. This means the output state of the clock pulse toggles (changes from 0 to1) for one cycle.

As the Q' of U1 is connected to the clock input of U2, then the clock input of second flip flop will become 1. This makes the output of U2 to be high.

In this way the next clock pulse will make the Q0 to become high again.So now both Q0 and Q1 are high, this results in making the 4 bit output 1100. Now if we apply the fourth clock pulse, it will make the Q0 and Q1 to low state and toggles the U3. So the output Q2 will become 0010. As this circuit is 4 bit up counter.

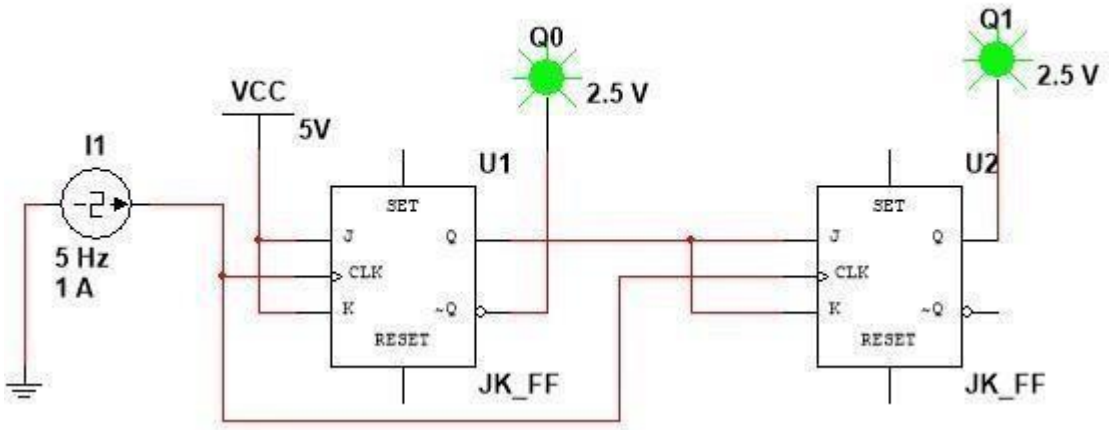
Previous State	Next State
0000	1000
1000	0100
0100	1100
1100	0010
0010	1010
1010	0110
0110	1110
1110	0001
0001	1001
1001	0101
0101	1101
1101	0011
0011	1011
1011	0111
0111	1111
1111	0000

Exercise 3:

Design 2-bit synchronous counter JK flipflop in Verilog HDL**.**

Circuit diagram:

2 Bit Synchronous Counter



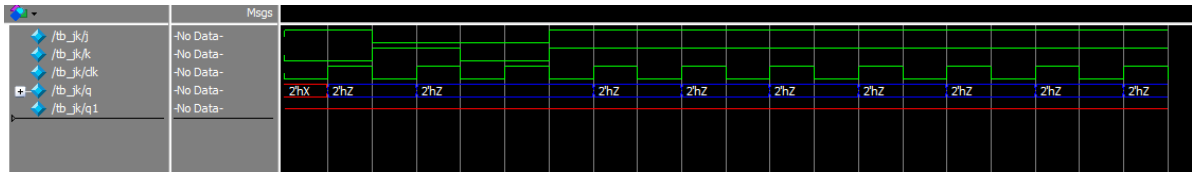
HDL Code:

```
module jk_ff(j,k,clk,q);
input j,k,clk;
output q;
reg q;
always @ (posedge clk)
case ({j,k})
2'b00 : q <= q;
2'b01 : q <= 0;
2'b10 : q <= 1;
2'b11 : q <= ~q;
endcase
endmodule
module tb_jk;
reg j;
reg k;
reg clk;
wire [1:0]q;
jk_ff jk0(j,k,clk,q);
jk_ff jk1(q,q,clk,q1);
initial
begin
clk=0;
end
always #5 clk = ~clk;
initial
begin

j = 1;
k = 0;

#10 j = 0;
k =1;
#10 j = 0;
k = 0;
#10 j = 1;
k = 1;
end
endmodule
```

Waveform:

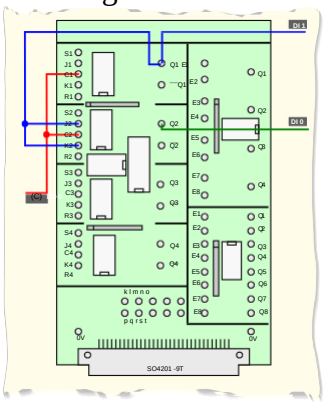

Msgs
/tb_jk/j
/tb_jk/k
/tb_jk/clk
/tb_jk/q
/tb_jk/q1
-No Data-
-No Data-
-No Data-
-No Data-
-No Data-
2'hX
2'hZ
2'hZ
2'hZ
2'hZ
2'hZ
2'hZ
2'hZ
2'hZ
2'hZ

Exercise 4:

This experiment is intended to investigate the operation of a synchronous counter with 4 counting states.

Experiment steps: Synchronous counters (m=4)

1. Connect the card to the Uni*Tr@in*-I as shown in the list of connections on the right.



Click on the image for a schematic representation of the wiring

Note: Inputs, which are not connected (for example, J and K inputs), are set to a **high level** by pull-up resistors.

List of co nections

From	*To*
Digital Out 0	Terminal FF **C1, C2**
Terminal FF **Q1**	Terminal FF **J2**
Terminal FF **Q1**	Terminal FF **K2**
Digital In 0	Terminal FF **Q2**
Digital In 1	Terminal FF **Q1**

2. Change over to the *logic analyzer* and load the workspace titled
'**Synchronous counter m=4**'.

If the FF outputs are high, reset the FFs (briefly connect **R** to ground).

Logic analyzer

3. Draw the truth table of the waveform.

Previous State	Next State
00	01
01	10
10	11
11	00