Name	Muhammad Asad
Reg. #	2019-EE-383
Marks	

Experiment # 7

Design Combinational Circuits using Decoders

Objective:

- *Designing of different Digital Systems*
- *Implementation of function using decoder*

Exercise 1:

You are a digital system engineer and you are required to design a digital system based on the following criteria. The system has three buttons. Each button sends logic 1 when the button is being pressed and a zero once it is released. The system should light an LED (by sending it a logic 1) whenever only one button is pressed at a time, and should turn off the LED (by sending it a logic 0) when more than one button is pressed. At least one button will always be pressed so we do not care what the circuit does when no buttons are pressed. Design a minimized circuit to control the LED.

Design a 3×8 line decoder using ModelSim in Verilog. Use this decoder and implement the above system.

Design Calculations:

Truth Table:

X	Y	Z	O
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

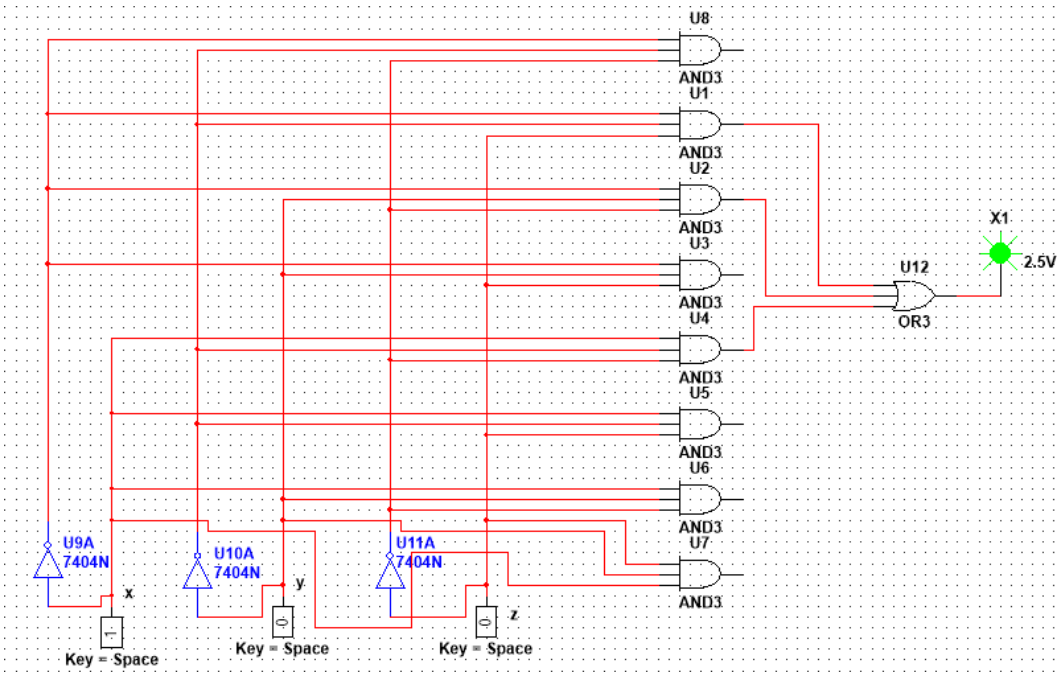
K-MAP:

×	$x'y'$	xy'	xy	$x'y$
z'	0	1	0	1
z	1	0	0	0

Minimized Function:

$$F = x'y'z + xy'z' + x'yz'$$

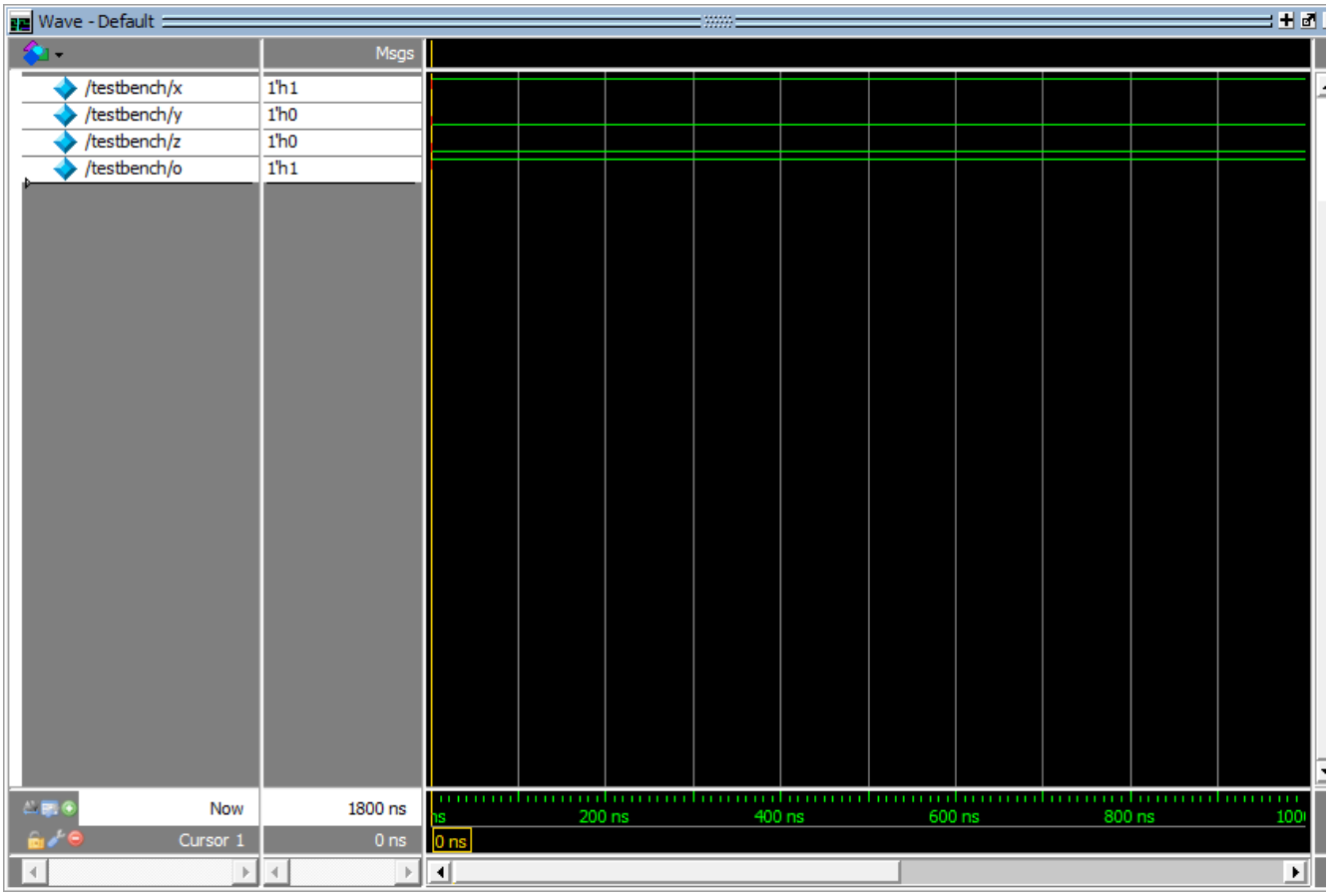
Decoder Circuit Diagram:



HDL code:

```
module decoder(x,y,z,o);
input x,y,z;
output o;
wire a,b,c,d,e,f,g,h,i,j,k;
not a1(a,x);
not a2(b,y);
not a3(c,z);
and a4(d,x',y',z');
and a5(e,x',y',z);
and a6(f,x',y,z');
and a7(g,x',y,z);
and a8(h,x,y',z');
and a9(i,x,y',z);
and a10(j,x,y,z');
and a11(k,x,y,z);
or  a12(o,e,f,h);
endmodule
module testbench();
reg x,y,z;
wire o;
decoder a13(x,y,z,o);
initial
begin
x=0;
y=0;
z=0;
end
endmodule
```

Output waveforms



Observations

- We observe that how to use the concept of decoder . .
- In this lab we verify that the decoder in circuit by using multisim by drawing the circuit and than we can write the HDL decoder code on modelsim and take output both outputs are same of modelsim and multisim.
- In this lab if decoder circuit are used we observe that if only one input is “on” the output is “on” otherwise it give “off”.
- In this lab if more than one button is pressed it give “off” output.

Exercise 2:

Four large tanks at a chemical plant contain different liquids being heated. Liquid-level sensors are being used to detect whenever the level in tank A or tank B rises above a predetermined level. Temperature sensors in C and D detect when the temperature in either of the tanks drops below a prescribed temperature limit. Assume that the liquid-level sensor outputs A and B are LOW when the level is satisfactory and HIGH when the level is too high. Also, the temperature sensor outputs C and D are LOW when the temperature is satisfactory and HIGH when the temperature is too LOW.

Design a logic circuit using **4 x 16 line decoder** that will detect whenever, the level in tank A or tank B is too high at the same time when the temperature in either tank C or tank D is too low. List the truth table and implement the design.

Design Calculations:

Truth table:

A	B	C	D	O
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

K-Map:

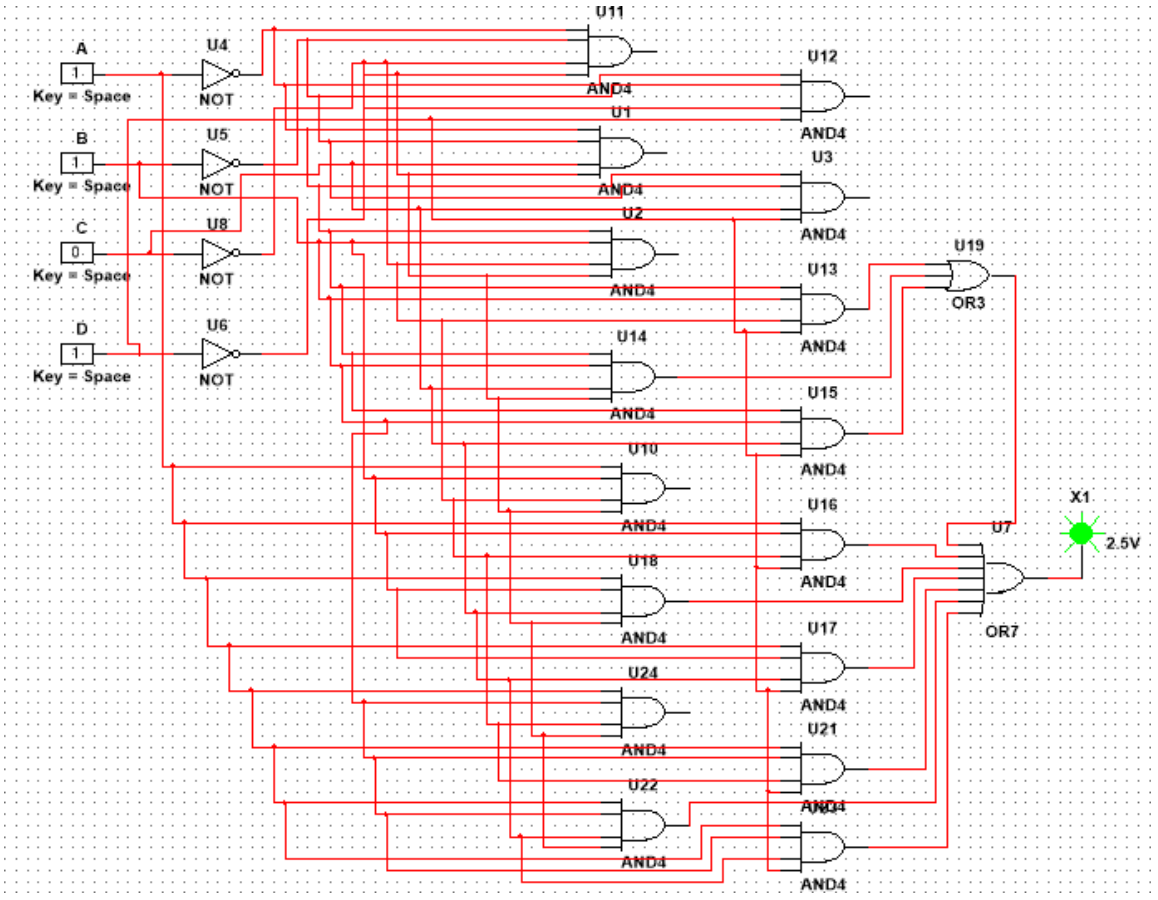
×	$C'D'$	$C'D$	CD	CD'
$A'B'$				
$A'B$		1	1	1
AB		1	1	1
AB'		1	1	1

Minimized Function:

$$F=A'BC'D + A'BCD + A'BCD' + ABC'D + ABCD + ABCD' + AB'C'D + AB'CD + AB'CD'$$

$$F=A'B(C'D + CD + CD') + AB(C'D + CD + CD') + AB'(C'D + CD + CD')$$

Circuit Diagram:

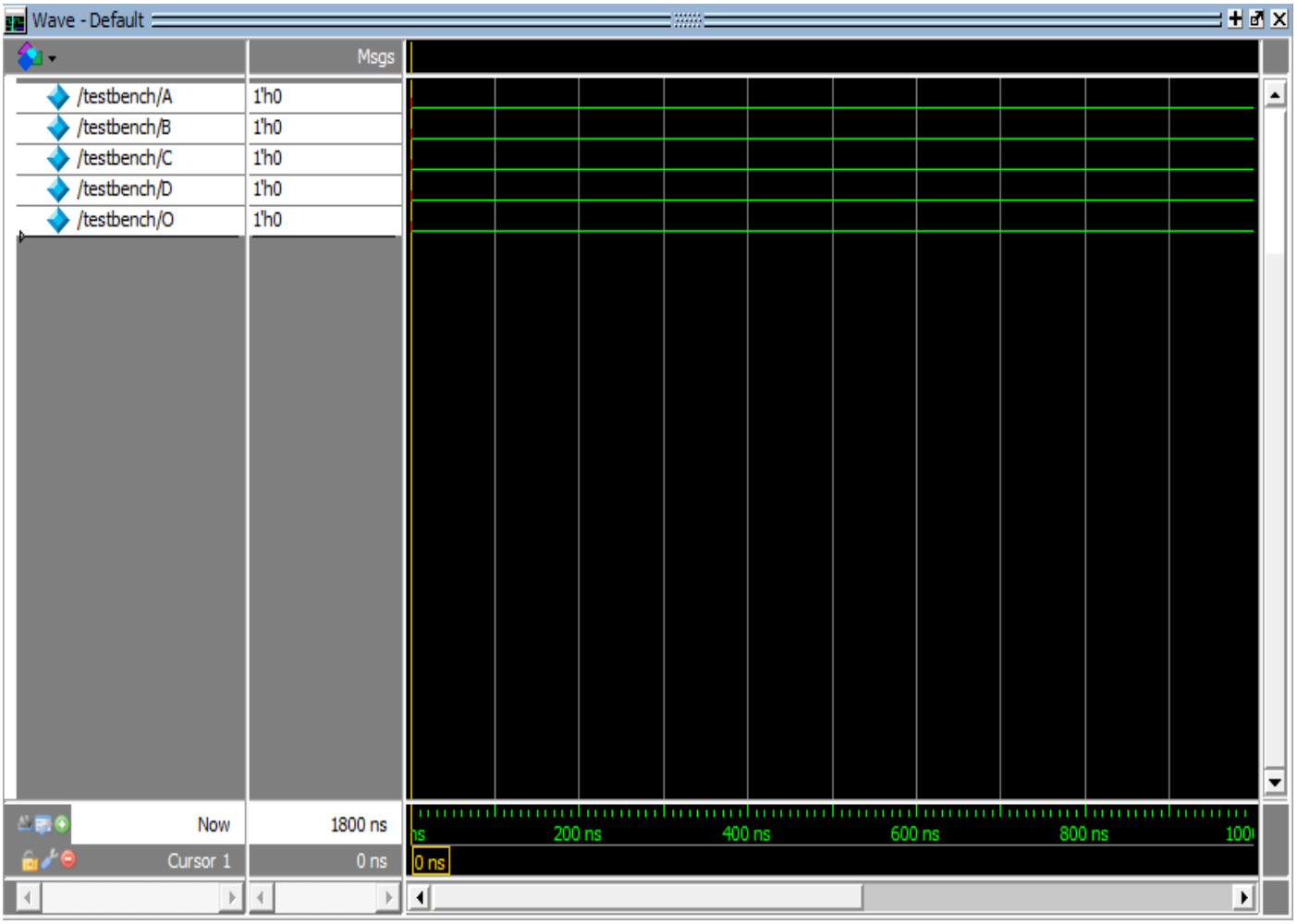


HDL code:

```
module decoder(A,B,C,D,O);
input A,B,C,D;
output O;
wire a,b,c,d,e,f,g,h,i,j,k,l,m,n,o,p,q,r,s;
not u1(a,A);
not u2(b,B);
not u3(c,C);
not u4(d,D);
and u5(e,A,B,C,D);
and u6(f,A,B,C,D);
and u7(g,A,B,C,D);
and u8(h,A,B,C,D);
and u9(i,A,B,C,D);
and v1(i,A,B,C,D);
and v2(j,A,B,C,D);
and v3(k,A,B,C,D);
and v4(l,A,B,C,D);
and v5(m,A,B,C,D);
and v6(n,A,B,C,D);
and v7(o,A,B,C,D);
and v8(p,A,B,C,D);
and v9(q,A,B,C,D);
and w1(r,A,B,C,D);
and w2(s,A,B,C,D);
or  w3(O,i,j,k,m,n,o,q,r,s);
endmodule
module testbench();
reg A,B,C,D;
wire O;
decoder w4(A,B,C,D,O);
```

```
initial
begin
A=0;
B=0;
C=0;
D=0;
end
endmodule
```

Output waveforms



Observations

- In this lab we use decoder we detect the liquid level in the tanks .
- We use four tanks and use liquid level sensors in it who detects the liquid level of the tanks.
- And after this we make truth table logic for this purpose and minimized the function and draw its circuit on multisim and HDL code on modelsim and run this function which will gave the same output that we need for this purpose .
- In this lab logic is very helpful for tanker level dectector.