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Experiment # 12

Understanding the Operation and Designing of Registers and Shift Registers

Objective:

- *DesignofashiftregisterinVerilog*
- *Workingouthediferencebetweenserialandp araleloutput.*

Apparatus:

*Workstation Core 2 Duo, UniTr@inLucasNu**l**e,SO4201-9TCard, Jumpers wires, Power Supplies*

Theory:

Registers:

*In terms of information processing **Registers** are miniature **memory units** for a modest number of bits. Normally they serve for short-term storage of information. The simplest register is the D flip- flop (Latch). An arrangement of more than one flip-flop in series, triggered synchronously by one common clock signal, is termed a **Shift Register**. Shift registers can also be made of JK flip-flops and as such can be used as counters in some special applications.*

Shift registers are used mainly for the following tasks:

1. *As **buffer storage** and **memory** (small and particularly fast):*
2. *For **converting** serial data into parallel data and parallel data into serial data:*
3. *For **synchronization** and **time delay** of data:*

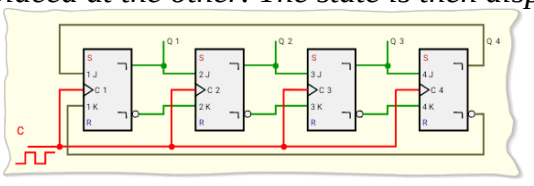
*In actual practice only synchronous shift registers are used. The design of shift registers is based on the procedures used in designing synchronous counters. Only the input functions for **J** and **K** are determined. The input functions of the following flip-flops are the same as the previous output variables.*

Shift register - serial input/serial output

Inthis experiment, wewillset up andinvestigateone 4-bitshift register withserialinputandserial output.

- ***Circular shift register***

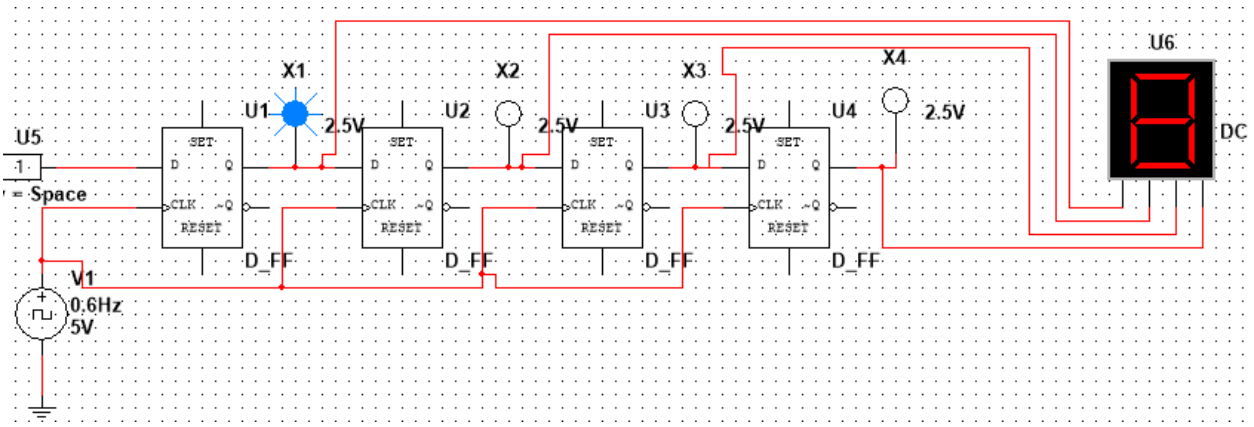
*Inacircularshiftregister, anumbersequenceis continuously'**shiftedthrough**'sothatthelast binary digit is shifted out of one end andreplaced at the other. The state is then displayed.*



Exercise 1:

Design a 4-bit shift register in Verilog using D flip flops.

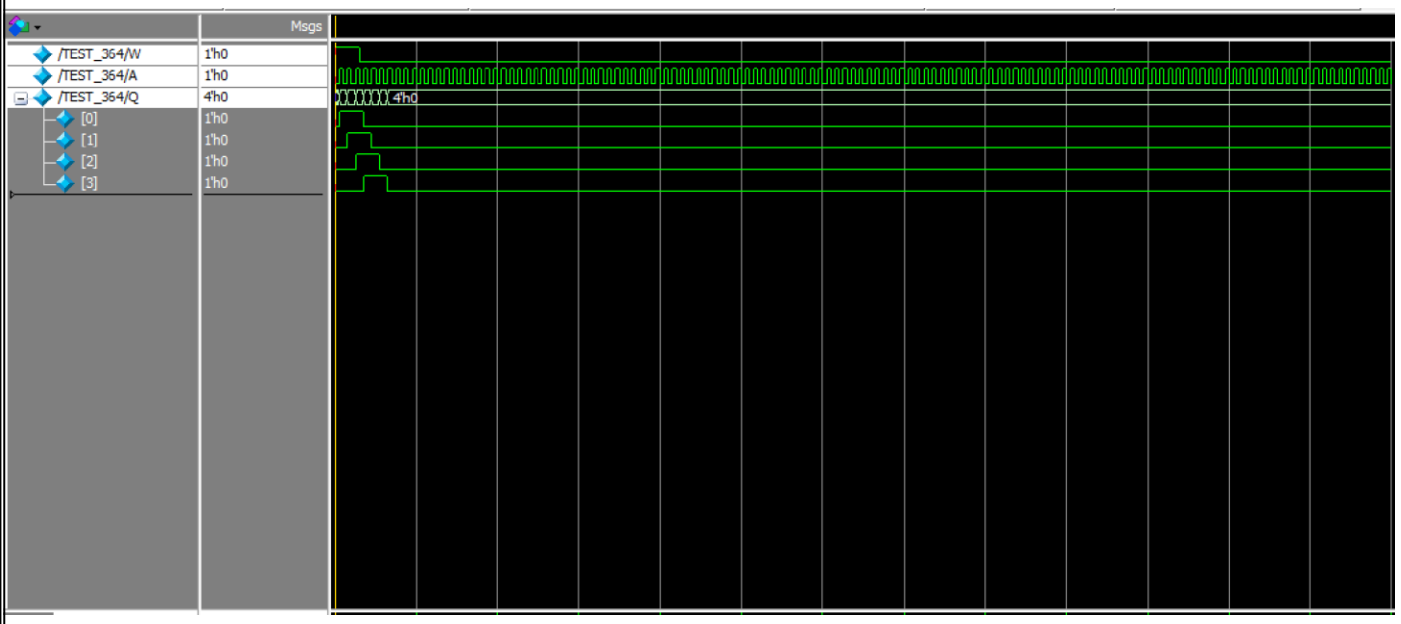
CIRCUIT:



HDL Code:

```
Ln#
 1  module lab(W,A,Q);
 2  input W,A;
 3  output Q;
 4  reg Q;
 5
 6  initial begin
 7
 8  Q=0;
 9  end
10  always @(posedge A)
11  case ({W})
12  1'b0 : Q <= 0;
13  1'b1 : Q <= 1;
14  endcase endmodule
15  module TEST_364();
16  reg W,A;
17  wire [0:3]Q;
18  lab a1 (W,A,Q[0]);
19  lab a2 (Q[0],A,Q[1]);
20  lab a3 (Q[1],A,Q[2]);
21  lab a4 (Q[2],A,Q[3]);
22  initial begin
23  A = 0;
24  end
25  always #5 A=~A;
26  initial begin
27  W=1;#30;
28  W=0;#30;end
29  endmodule
30
```

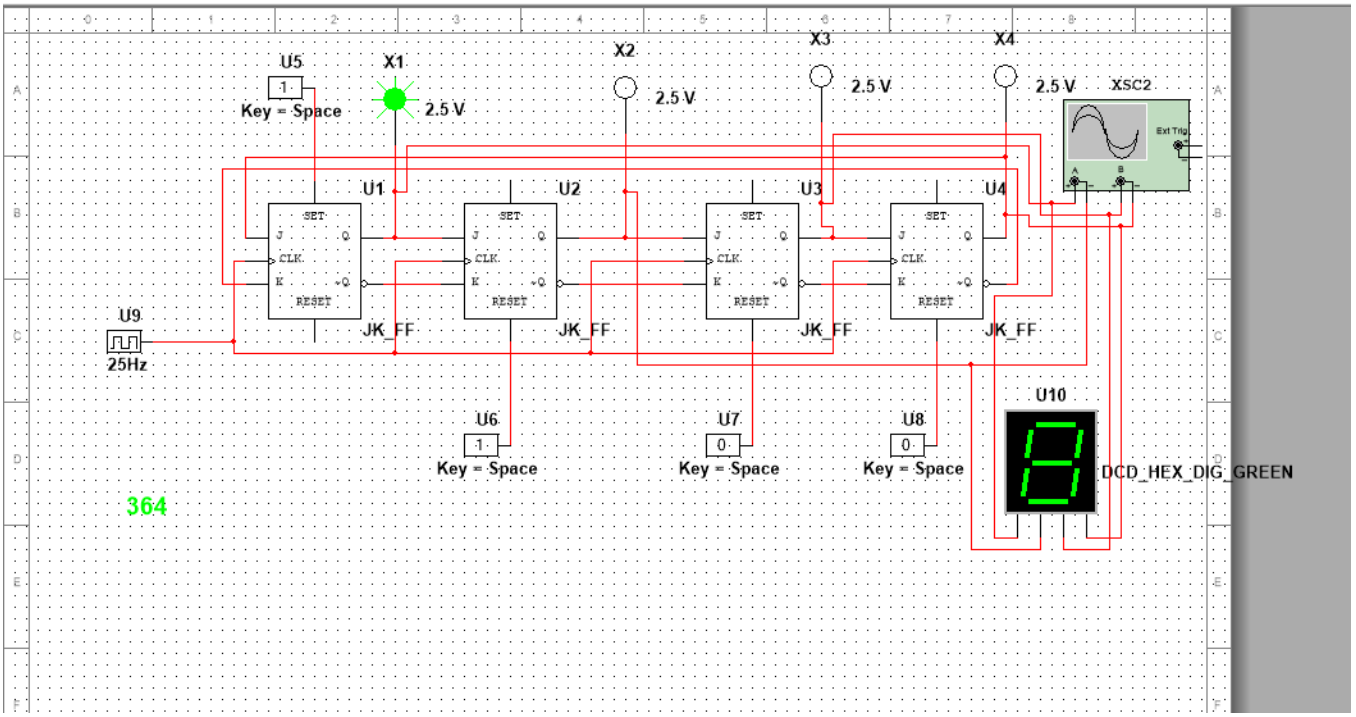
Wavefprm:

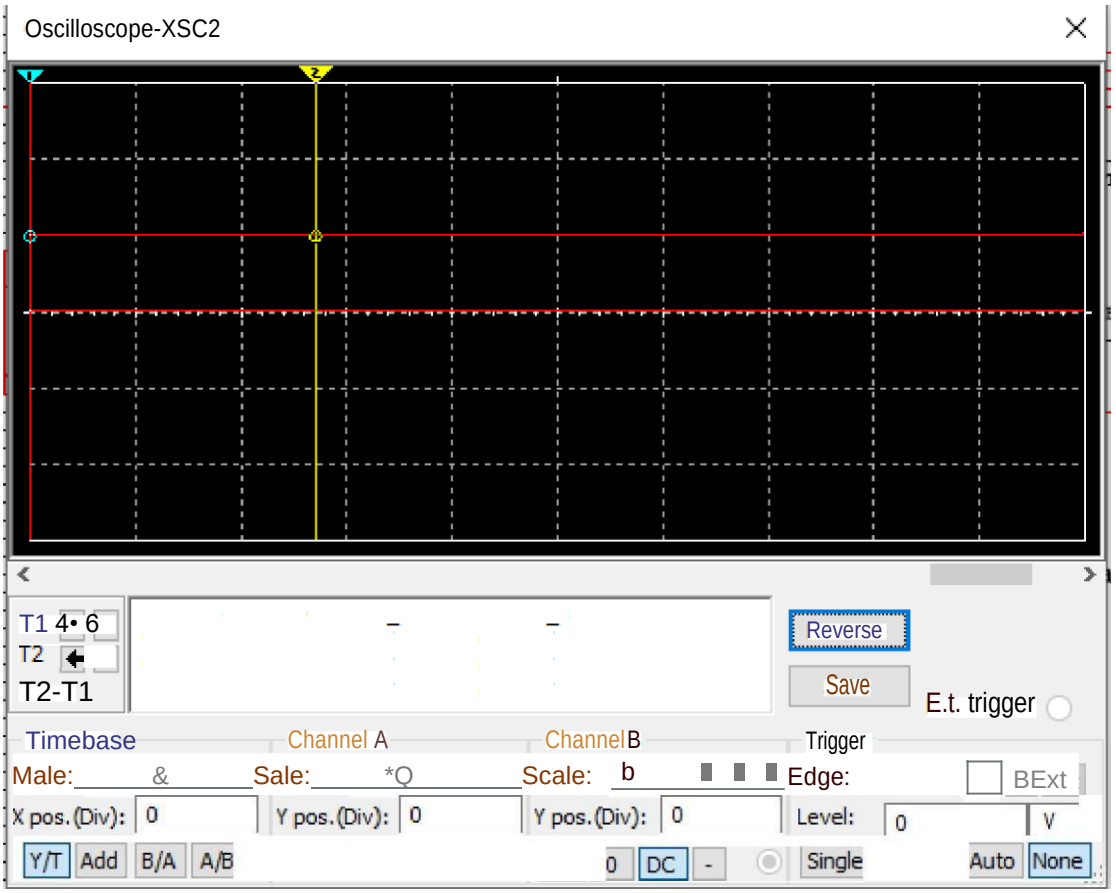


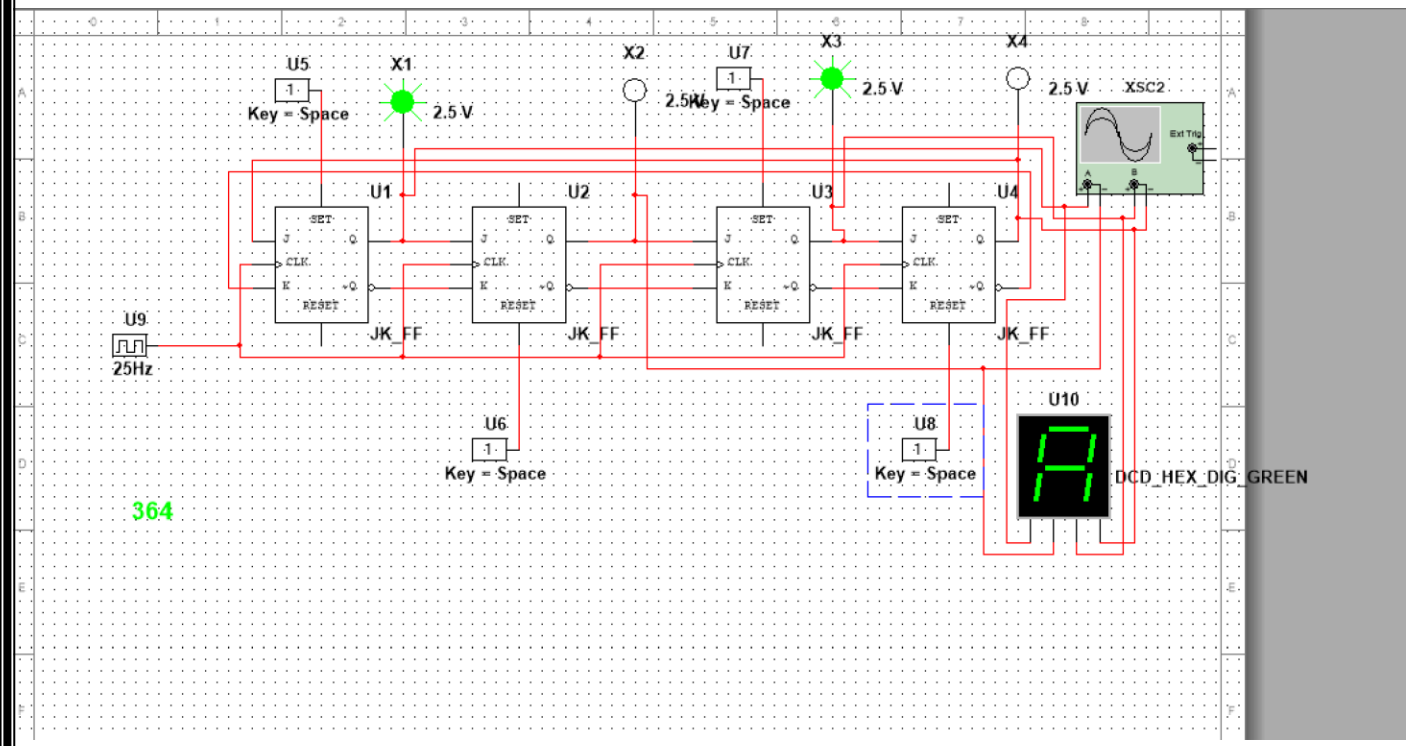
Exercise 2:

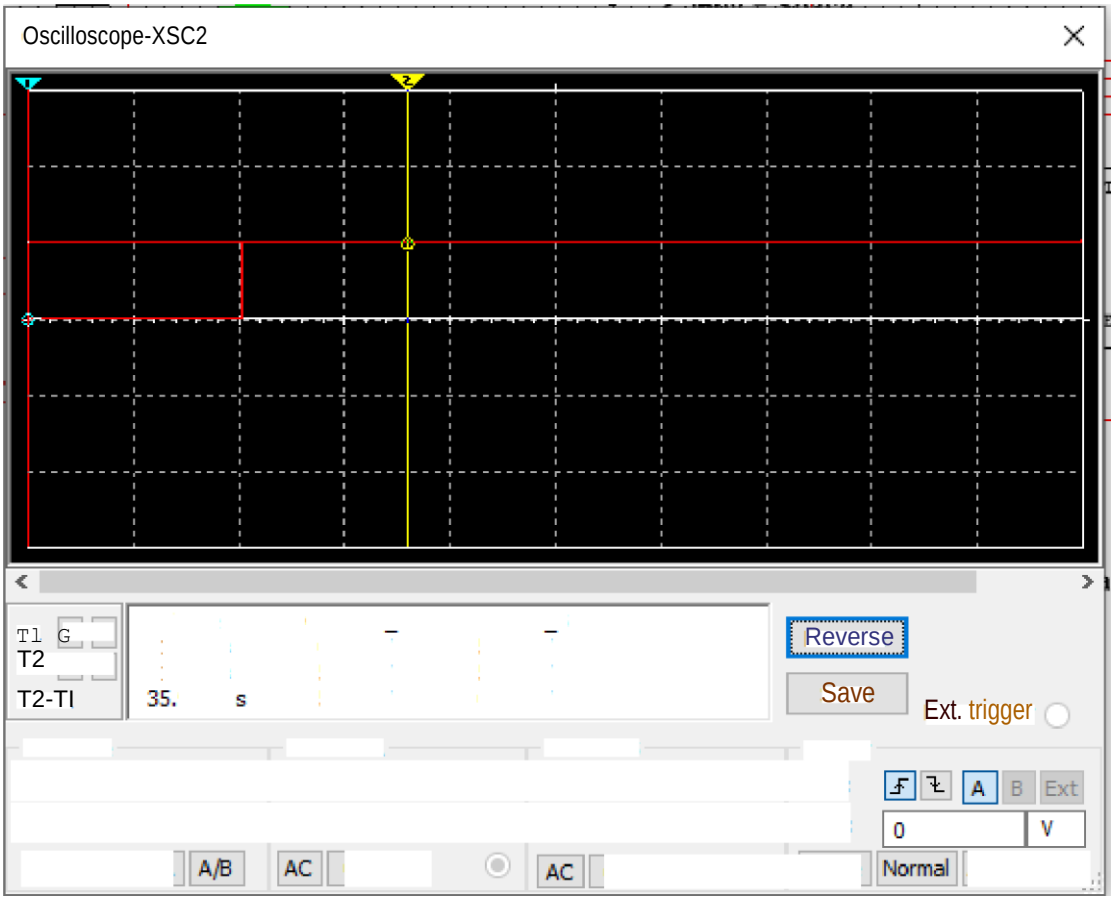
Modify the circuit with JK flip flops and implement modified circuit. Using the ***S*** *(Set) and* ***R*** *(Reset) buttons apply a random bit pattern (**e.g.** Q1=1, Q2=0, Q3=0, Q4=0) or (Q1=1, Q2=0, Q3=1, Q4=0).*

Attach Oscilloscope waveform for both patterns.



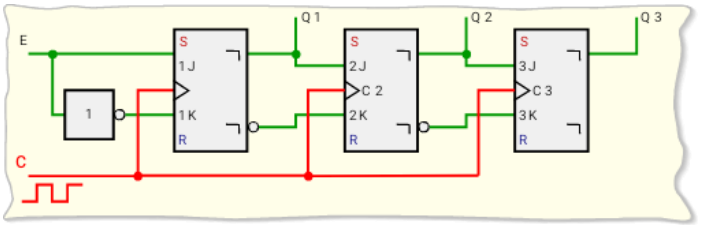

Oscilloscope-XSC2
T1 4• 6
T2
T2-T1
Reverse
Save
E.t. trigger
Timebase
Channel A
Channel B
Trigger
Male: &
Sale: *Q
Scale: b
Edge:
BExt
X pos.(Div): 0
Y pos.(Div): 0
Y pos.(Div): 0
Level: 0
V
Y/T
Add
B/A
A/B
0
DC
-
Single
Auto
None


U5
Key = Space
X1
2.5 V
X2
U7
2.5 V
Key = Space
X3
2.5 V
X4
2.5 V
XSC2
U1
U2
U3
U4
JK_FF
JK_FF
JK_FF
JK_FF
U9
25Hz
U6
Key = Space
U8
Key = Space
U10
DCD_HEX_DIG_GREEN
364



Exercise 3:

In this experiment, the shift register used in the previous experiment will be used for serial to parallel operation.



To access the data "111" in parallel, how many clock cycles needed for parallel access of data? Give reason.

There are four (3) clock cycles are required for three(3) bit data.In first cycle value is equal to 100

I get 1 value at first Flip Flop.in second cycle value is equal to 110 at this first two FlipFlop get 1 value

In third clock cycle I get 111 value which is required.

To access the data "1111" in parallel, how many clock cycles needed for parallel access of data? Give reason.

There are five(4) clock cycles are required to access the data 1111.as I mentioned in previous question

That I required 3 clock cycle for 111 .similarly we need four clock cycle for 1111.