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Experiment # 3

To Understand Negation Laws (De Morgan's Laws) and XOR & XNOR Operation

Objective:

- *Negation of logic*
- *Antivalence and Equivalence operation*

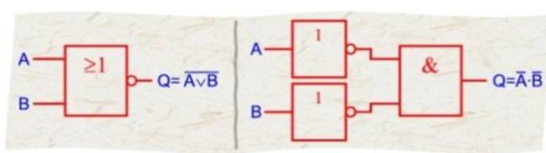
Apparatus:

Gate ICs, Breadboard, Jumpers wires and Power Supplies

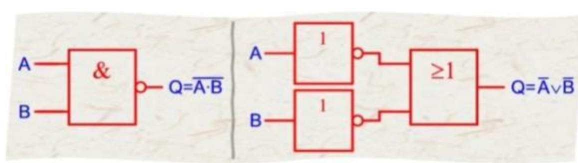
Theory:

- Negation Laws (De Morgan's Laws)

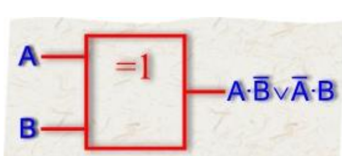
Negation law 1: $\overline{\boldsymbol{A}+\boldsymbol{B}} = \overline{\boldsymbol{A}}.\overline{\boldsymbol{B}}$



Negation law 2: $\overline{\boldsymbol{A}.\boldsymbol{B}} = \overline{\boldsymbol{A}}+\overline{\boldsymbol{B}}$

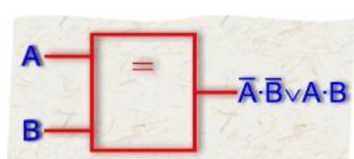


- BOOLEAN OPERATIONS



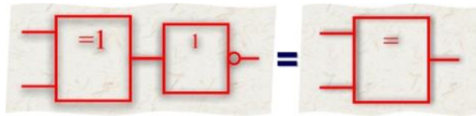
EXOR

ANTIVALENCE

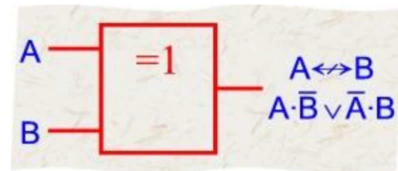


EXNOR

EQUIVALENCE



EXOR (Antivalence)

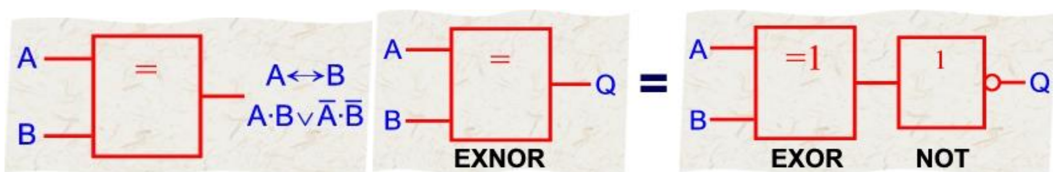


The symbol for EXOR is that shown in the illustration. The operation is termed "Exclusive OR" or "Antivalence".

The logical function is given as $\boldsymbol{Q = \bar{A}.B + A.\bar{B}}$ This statement will be tested in the following experiment.

EXNOR (Equivalence)

The symbol for EXNOR is that shown in the illustration. The operation is termed "Exclusive NOR" or "Equivalence".



An EXNOR operation simply corresponds to an inverted EXOR

The logical function is given as $\boldsymbol{Q = \bar{A}.\bar{B} + A.B}$. This statement will be tested in the following experiment.

<u>Procedure and observation:</u>

Exercise 1:

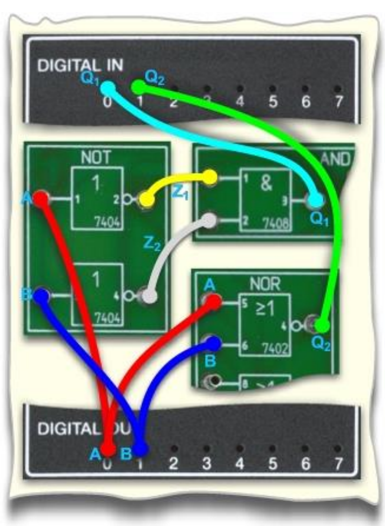


Fig.1: Experiment set-up -

$Q_1 = A' \cdot B'$ $\quad Q_2 = (A+B)'$

In this experiment, both sides of the equation are experimentally reproduced and can be directly compared with one another. Confirm the validity of the negation law from the table.

Table 1

Q_1	Q_0	I_1	I_0
B	**A**	**Q_2**	**Q_1**
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

$\uparrow$ $(A+B)'$ $\qquad$ $\uparrow$ $A' \cdot B'$

Exercise 2:

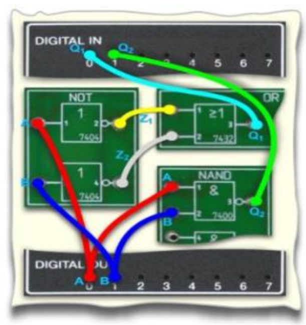


Fig.2: Experiment set-up -

$Q_1 = A' + B'$ $\qquad$ $Q_2 = (A \cdot B)'$

Table 2

Q_1	Q_0	I_1	I_0
B	**A**	**Q_2**	**Q_1**
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

$\uparrow$ $(A \cdot B)'$ $\qquad$ $\uparrow$ $A' + B'$

Exercise 3: *EXOR*

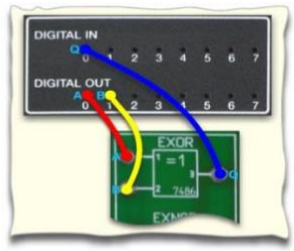


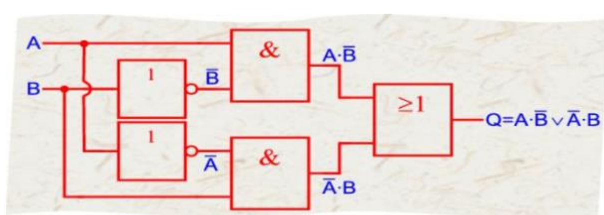
Fig.1 : Experiment set-up - EXOR

Table 1

Q_1	*Q_0*	*I_0*
B	**A**	**Q**
0	0	0
0	1	1
1	0	1
1	1	0

EXOR

Exercise 4:



This is how an EXOR gate is reproduced using OR/AND/NOT gates.

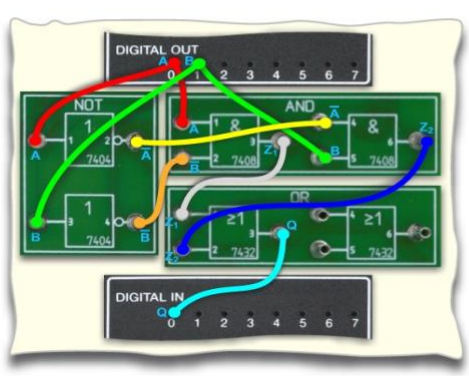


Fig.2: Experiment set-up - $Q = A'\cdot B + A\cdot B'$

Table 2

Q_1 Q_0 I_0

B	**A**	**Q**
0	0	0
0	1	1
1	0	1
1	1	0

↑

A′·B + A·B′

Confirm from the values in Tables 1 and 2 that the EXOR function can be represented by the function Q = A′·B + A·B′.

Exercise 5: *EXNOR*

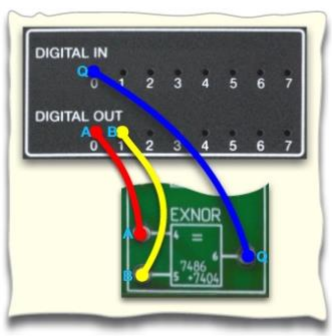


Fig.1 : Experiment set-up - EXNOR

Table 1

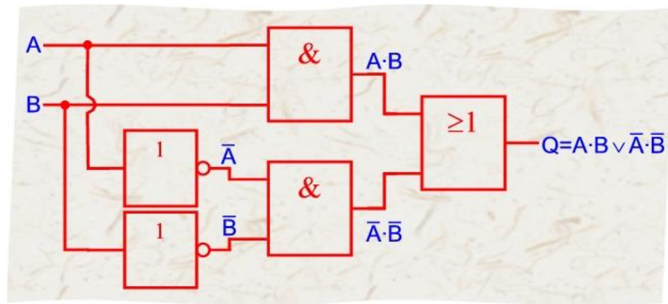
Q_1 Q_0 I_0

B	**A**	**Q**
0	0	1
0	1	0
1	0	0
1	1	1

EXNOR

Exercise 6:

This is how an EXNOR gate is reproduced using OR/AND/NOT gates.



Experiment set-up

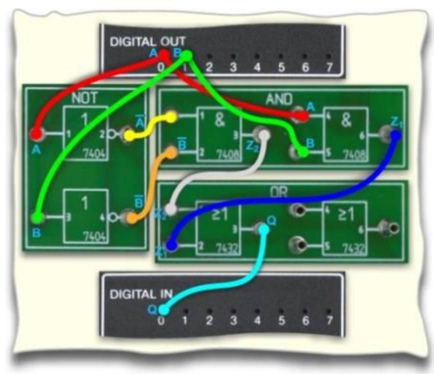


Fig.2 : Experiment set-up - Q = A·B + A′·B′

Table 2

Q_1	Q_0	I_0
B	**A**	**Q**
0	0	1
0	1	0
1	0	0
1	1	1

↑

A·B + A'·B'

Confirm from the values in Tables 1 and 2 that the EXNOR function can be represented by the function Q = A·B + A'·B'

Lab Exercises:

- Q3.1 Describe how an EXOR gate works. Why is it also known as an "antivalence" (inequality) gate?

  Ans: XOR gate is a digital logic gate that gives a true (1 0r HIGH) output when the number of true inputs is odd. An XOR gate implements an exclusive or; that is, a true output results if one, and only one, of the inputs to the gate is true.

  XOR represents the “ anti valence ” (inequality) gate because the output is true if the inputs are not same otherwise the output is false. A way to remember XOR is “ must have one or the other but not both “. It acts according to the truth to the above.

- Q 3.2 Describe how an EXNOR gate works. Why is it also known as an "equivalence" (equality) gate?

  Ans: An XNOR Gate is a type of digital logic gate that receives two inputs and produces one output. Both inputs are treated with the same logic, responding equally to similar inputs. Sometimes referred to as an "Equivalence Gate," the gate's output requires both inputs to be the same to produce a high output.

- Q 3.3 Write the Equation output of 3 input XOR gate.

  Ans: I can use the two or more inputs in exclusive OR gate, the output equation of the three inputs in XOR gate is.

$$Q = A.B.C' + A.B'.C + A'.B.C$$