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Reg. #	2019-EE-383
Marks	

Experiment # 11

Designing of up counter and down counters

Objective:

- *To design up & down counter*
- *Working out the essential distinctive features of synchronous and asynchronous counters.*

Apparatus:

Workstation Core 2 Duo, Uni*Tr@inLucas Nulle, SO4201-9T*Card, Jumpers wires, Power Supplies

Procedure:

Exercise 1:

Implement the 2-bit up/down asynchronous counter circuit in Verilog HDL.

Use a control bit to allow selection between the **up** and **down** counting modes.

If control bit **S** is set (S = 0), the counter is to count **up**.
If control bit **S** is not set (S = 1), the counter is to count **down**.

The following table shows the bit patterns occurring during up and down counts:

Up counter

	Q2	**Q1**
0	0	0
1	0	1
2	1	0
3	1	1
0	0	0

Down counter

	Q2	**Q1**
0	0	0
3	1	1
2	1	0
1	0	1
0	0	0

From the experiment set-up, determine the condition for clock input C2:

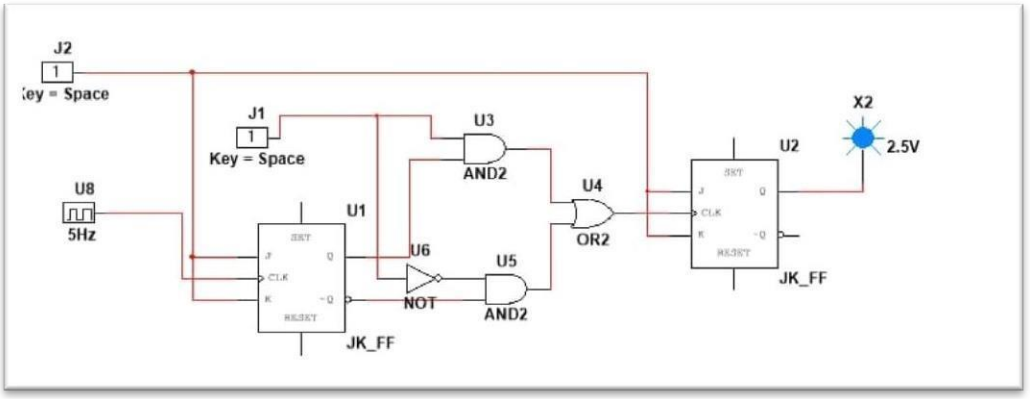
Equation:
C2=SQ+S'Q'

Accordingly:

If **S=1**: C2 = Q

If **S=0**: C2 = Q'

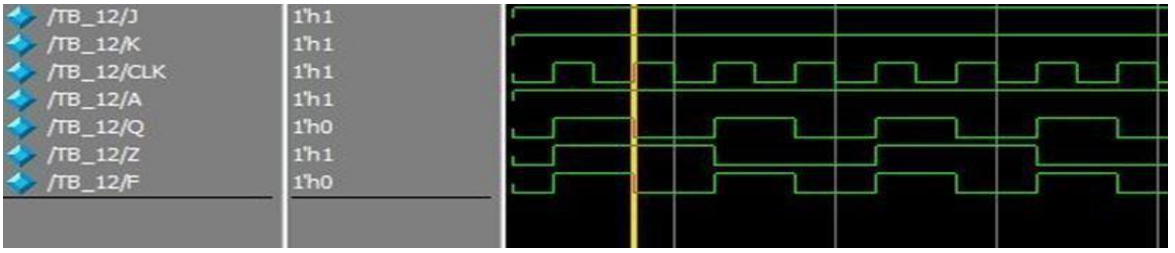
Circuit diagram:



HDL Code:

```
Ln#
 1
 2  module Task1(J,K,CLK,Q);
 3  input J,K,CLK;
 4  output Q;
 5  reg Q;
 6  initial begin
 7  Q=0;
 8  end
 9  always @(posedge CLK)
10  case ({J,K})
11  2'b00 : Q <= Q;
12  2'b01 : Q <= 0;
13  2'b10 : Q <= 1;
14  2'b11 : Q <= ~Q;
15  endcase endmodule
16  module Gates(A,Q,F);
17  input A,Q;
18  output F;
19  wire B,C,D,E,F;
20  not n1(B,A);
21  not n2(C,Q);
22  and a1(D,A,Q);
23  and a2(E,B,C);
24  or r1(F,D,E);
25  endmodule
26  module TB_12();
27  reg J,K,CLK;
28  reg A;
29  wire Q,Z;
30  Task1 h1 (J,K,CLK,Q);
31  Gates g1(A,Q,F);
32  Task1 h2 (J,K,F,Z);
33  initial begin
34  CLK = 0;
35  end
34  CLK = 0;
35  end
36  always #5 CLK=~CLK;
37  initial begin
38  J=1; K=1; A=1;
39  end
40  endmodule
```

Waveform:

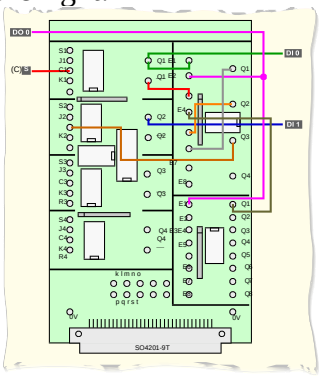


Exercise 2:

Asynchronous up and down counter experiment:

Experiment steps: Asynchronous up and down counter

1. Connect the card to the Uni*Tr@in*-I as shown in the list of connections on the right.



Click on the image for a schematic representation of the wiring

Note: Inputs which are not connected (for example, J and K inputs),

List of connections

From	*To*
Interface **S**	Terminal FF **C1**
Digital In 0	Terminal FF **Q1**
Digital In 1	Terminal FF **Q2**
Digital Out 0	Terminal NOT **E1**
Terminal NOT **E1**	Terminal NAND**E4**
Terminal FF **Q1**	Terminal NAND**E3**
Terminal FF **Q1**	Terminal NAND**E2**
Terminal NOT **Q1**	Terminal NAND**E1**
Terminal NAND**Q1**	Terminal NAND**E5**
Terminal NAND**Q2**	Terminal NAND**E6**
Terminal NAND**Q3**	Terminal FF **C2**

2. Open the following virtual instruments from the *Instruments* menu:

Settings

- Function generator
- Extended digital inputs and outputs

Frequency: 1Hz
Logic
Power ON

3. Start the function generator and observe the display of the digital inputs. Switch **S** (DO0) from**0** to **1**.
4. **What can you observe after the circuit has been started up?**

This circuit can count upto 4 from 0to3. It depends on input of S. If S is equal to 1 it counts down from 3-0 and if S is equal to 0 it counts up 0-3.

Exercise 3:

- **Synchronous up and down counter**

This experiment is intended to investigate the operation of a synchronous up and down counter. A synchronous counter is capable of binary up and down counting between 0 and 3. A control bit is to allow selection between the **up** and **down** counting modes.

Determine the number of JK flip-flops required here.

n = 2

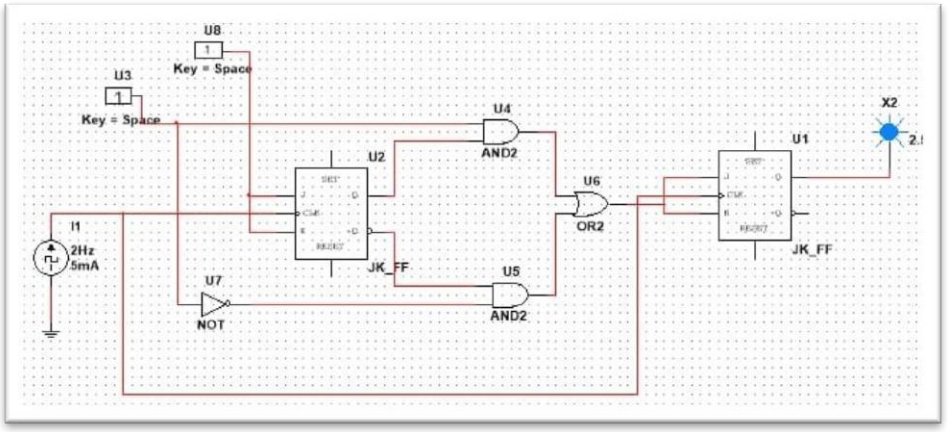
In the following table, enter the values which occur in the up and down counting modes.

Table

Counting direction	for t_n		for t_{n+1}	
	2^1	2^0	2^1	2^0
	$Q2_n$	$Q1_n$	$Q2_{n+1}$	$Q1_{n+1}$
Down	0	0	1	1
	1	1	1	0
	1	0	0	1
	0	1	0	0
Up	0	0	0	1
	0	1	1	0
	1	0	1	1

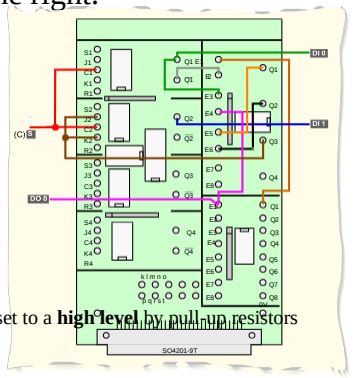
	1	1	0	0

Circuit configuration using a JK flip-flop and gates



Experiment steps: Synchronous up and down counter

1. Connect the card to the Uni*Tr@in*-I as shown in the list of connections on the right.



Note: are set to a **high level** by pull-up resistors

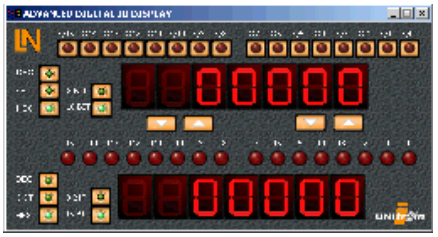
Click on the image for a schematic representation of the wiring

List of Connections

From	*To*
Interface	Terminal FF **C1,C2**
Digital In 0	Terminal FF **Q1**
Digital In 1	Terminal FF **Q2**
Digital Out 0	Terminal NOT **E1**
Terminal NOT **E1**	Terminal NAND**E4**
Terminal FF **Q1**	Terminal NAND**E3**
Terminal FF **Q1**	Terminal NAND**E2**
Terminal NOT **Q1**	Terminal NAND**E1**
Terminal NAND**Q1**	Terminal NAND**E5**
Terminal NAND**Q2**	Terminal NAND**E6**

Terminal NAND **Q3**	Terminal FF **J2,K2**

2. Open the following virtual instruments from the *Instruments* menu:
   - Function generator
   - Extended digital inputs and outputs



Settings

Function generator	Amplitude: 50% at 1:1 Frequency: 1Hz **Logic**
	Power ON

3. Start the function generator and observe the display of the digital inputs. Switch **S** (DO0) from **0** to **1**.
4. **What can you observe after the circuit has been started up?**
   I observed that the circuit is built using JK flip flops. Its output depends on Up or Down inputs .