Laboratory Exercise 7

Clocks and Timers

Part I 3-digit BCD counter

Implement a 3-digit BCD counter. Display the contents of the counter on the 7-segment displays, *HEX2−0*. Derive a control signal, from the 50-MHz clock signal provided on the Altera DE2-115 board, to increment the contents of the counter at one-second intervals. Use the pushbutton switch KEY_0 to reset the counter to 0.

1. Create a new Quartus project which will be used to implement the desired circuit on the DE2-115 board.
2. Write a Verilog file that specifies the desired circuit.
3. Include the Verilog file in your project and compile the circuit.
4. Simulate the designed circuit to verify its functionality.
5. Assign the pins on the FPGA to connect to the 7-segment displays and the pushbutton switch, as indicated in the User Manual for the DE2-115 board.
6. Recompile the circuit and download it into the FPGA chip.
7. Verify that your circuit works correctly by observing the display.

Part II Real-time Clock

Design and implement a circuit on the DE2-115 board that acts as a time-of-day clock. It should display the hour (from 0 to 23) on the 7-segment displays *HEX7−6*, the minute (from 0 to 60) on *HEX5−4* and the second (from 0 to 60) on *HEX3−2*. The button switch KEY0 can be used to reset the real-time clock and KEY1 to load the values of hour and minute preset by the SW_{15-0}.

Part III Reaction Timer

Design and implement on the DE2-115 board a reaction-timer circuit. The circuit is to operate as follows:

1. The circuit is reset by pressing the pushbutton switch KEY_0.
2. After an elapsed time, the red light labeled $LEDR_0$ turns on and a four-digit BCD counter starts counting in intervals of milliseconds. The amount of time in seconds from when the circuit is reset until $LEDR_0$ is turned on is set by switches SW_{7-0}.
3. A person whose reflexes are being tested must press the pushbutton KEY_3 as quickly as possible to turn the LED off and freeze the counter in its present state. The count which shows the reaction time will be displayed on the 7-segment displays *HEX2-0*.

Part IV M-digit base-N Up/Down Counter

Implement a M-digit base-N up/down counter. Display the contents of the counter on the 7-segment displays, HEXM-1. Derive a control signal, from the 50-MHz clock signal provided on the DE2-115 board, to increment or to decrement the contents of the counter at one-second intervals. Use the button switch KEY0 to toggle the up/down behaviors of the counter, and KEY1 to reset the counter to 0.