EEE3096S - Tutorial 4
2022

7 Digital to Analog Convertors

Submit a single PDF (named correctly with STUDNUM1_STUDNUM2_Tut4.pdf) answering the following questions. If you pull from any sources, be sure to correctly cite them.

7.1 Learning Objective

By the end of this practical, you will have:

- Theoretical understanding of DACs.
- Practical experience with signal generation and low-pass filtering.

Preparatory notes: Read the lecture slides on DACs before you begin.

7.2 DAC Metrics

1. DACs opeate on the general premise that $V_{out} = K * digitalinput$. Calculate the output voltage V_{out} of a 5-bit DAC if the digital input is 0b11101. With a digital input of 0b101000 the output is 10mV. [5 Marks]
2. A common DAC metric is full-scale error, which is the maximum deviation from its ideal value, expressed as a percentage of its full scale. Calculate the range of possible outputs for an input of 0b100000000000 using a 12-bit DAC with a full-scale output of 10mA and full-scale error of $\pm 0.5\%$ FS. [5 Marks]

Provide clear explanations (or working) for both your above answers.

7.2.1 DAC Design

In Practical 4 we will be building our own "cheap and nasty" PWM DAC signal generator with a maximum output frequency of 5Khz. To do this, we need to keep the following in mind:

- We want F_{PWM} to be significantly larger than our bandwidth F_{BW} so we can design a low-pass filter that will allow our signal through but attenuate the high frequency PWM harmonics.
- Raising F_{PWM} degrades the DACs resolution according the the following:

$$Resolution_{PWM} = \frac{log(\frac{F_{CLK}}{F_{PWM}})}{log(2)}[Bits]$$

- The formula to be used in configuring the timer module in PWM mode to control the PWM output frequency is

$$F_{PWM} = \frac{F_{CLK}}{(ARR + 1)(PSC + 1)}[Hz]$$

1. Calculate the maximum PWM frequency for a 10-bit DAC. [4 Marks]
2. Pick values for ARR and PSC. Check the Discovery board datasheet to ensure your values are within range. [1 Mark]
3. Design a Sallen-key low-pass filter that will allow our signal through but attenuate the high frequency PWM harmonics. We will limit our bandwidth to 5kHz. Test your filters performance in LTSpice or similar with a 1kHz signal, 5kHz signal and 20kHz signal. Include scrrenshots of your circuit as well as its output for the 1Khz, 5kHz and 20Khz inputs. [10 Marks]