# Computer-Aided VLSI System Design
# Homework 5 Report

**Due Tuesday, Dec. 3, 13:59**

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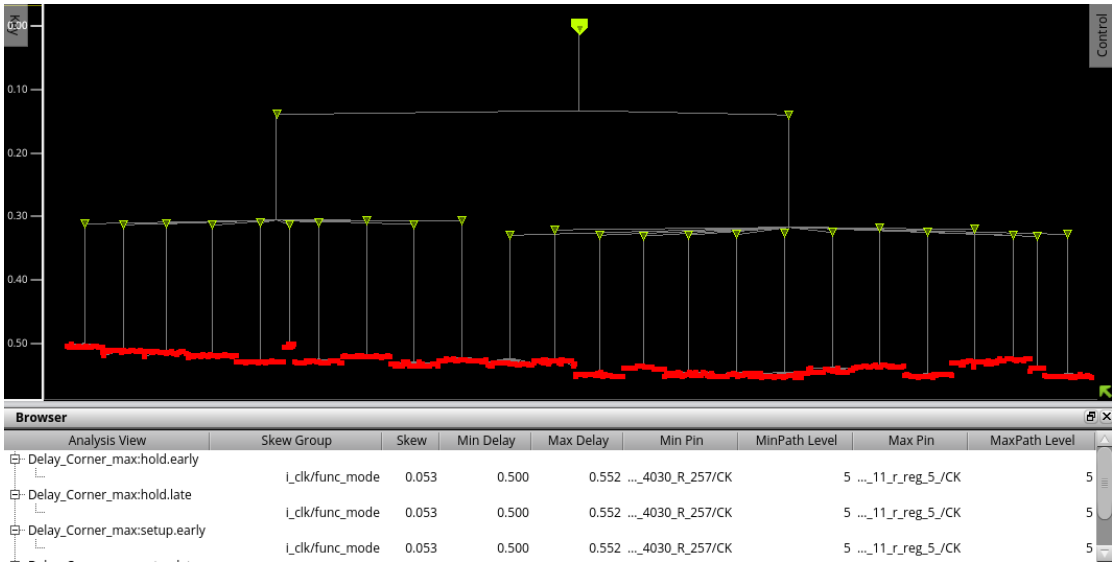
## APR Results

1. Fill in the blanks below.

| Design Stage | Description | Value |
|---|---|---|
| P&R | Number of DRC violations (ex: 0)<br>(Verify -> Verify Geometry…) | 0 |
| | Number of LVS violations (ex: 0)<br>(Verify -> Verify Connectivity…) | 0 |
| | Die Area ($um^2$) | 872808.36 |
| | Core Area ($um^2$) | 598829.14 |
| Post-layout Simulation | Clock Period for Post-layout Simulation (ex. 10ns) | 3.4ns |
| Follow your design in HW3?<br>(If not, specify student ID of the designer or 'from TA') | | Yes |

## Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).




2. Attach the snapshot of DRC and LVS checking after routing. (5%)

```
innovus 1> verify_drc
 *** Starting Verify DRC (MEM: 1508.1) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 187.680 187.680} 1 of 25
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {187.680 0.000 375.360 187.680} 2 of 25
  VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {375.360 0.000 563.040 187.680} 3 of 25
  VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {563.040 0.000 750.720 187.680} 4 of 25
  VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {750.720 0.000 936.560 187.680} 5 of 25
  VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 187.680 187.680 375.360} 6 of 25
  VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {187.680 187.680 375.360 375.360} 7 of 25
  VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {375.360 187.680 563.040 375.360} 8 of 25
  VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {563.040 187.680 750.720 375.360} 9 of 25
  VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {750.720 187.680 936.560 375.360} 10 of 25
  VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 375.360 187.680 563.040} 11 of 25
  VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {187.680 375.360 375.360 563.040} 12 of 25
  VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {375.360 375.360 563.040 563.040} 13 of 25
  VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {563.040 375.360 750.720 563.040} 14 of 25
  VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {750.720 375.360 936.560 563.040} 15 of 25
  VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 563.040 187.680 750.720} 16 of 25
  VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {187.680 563.040 375.360 750.720} 17 of 25
  VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {375.360 563.040 563.040 750.720} 18 of 25
  VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {563.040 563.040 750.720 750.720} 19 of 25
  VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {750.720 563.040 936.560 750.720} 20 of 25
  VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 750.720 187.680 931.930} 21 of 25
  VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {187.680 750.720 375.360 931.930} 22 of 25
  VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {375.360 750.720 563.040 931.930} 23 of 25
  VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {563.040 750.720 750.720 931.930} 24 of 25
  VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {750.720 750.720 936.560 931.930} 25 of 25
  VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:05.0  ELAPSED TIME: 5.00  MEM: 60.0M) ***
```

```
innovus 2> VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Tue Nov 26 11:27:50 2024

Design Name: core
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (936.5600, 931.9300)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 11:27:51 **** Processed 5000 nets.
**** 11:27:51 **** Processed 10000 nets.
**** 11:27:51 **** Processed 15000 nets.
**** 11:27:51 **** Processed 20000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Tue Nov 26 11:27:52 2024
Time Elapsed: 0:00:02.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:01.6  MEM: 23.914M)
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.059  |  0.059  |  0.321  |  0.703  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  4412   |  2252   |  2144   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 59.718%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.363  |  0.363  |  1.668  |  2.173  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  4412   |  2252   |  2144   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 59.718%
       (100.000% with Fillers)
------------------------------------------------------------
```

4. Show the critical path after post-route optimization. What is the path type? (10%)
(The slack of the critical path should match the smallest slack in the timing report)

```
Path 1: MET Setup Check with Pin processing_u0/add_tree_small_stage2_out_reg_2__
1__12_/CK
Endpoint:   processing_u0/add_tree_small_stage2_out_reg_2__1__12_/D (^) checked
with  leading edge of 'i_clk'
Beginpoint: processing_u0/i_in_data_2_r_reg_0_/Q                    (v)
triggered by  leading edge of 'i_clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.503
- Setup                         0.244
+ Phase Shift                   3.350
+ CPPR Adjustment               0.000
= Required Time                 3.610
- Arrival Time                  3.551
= Slack Time                    0.059
     Clock Rise Edge                     0.000
     + Clock Network Latency (Prop)      0.497
     = Beginpoint Arrival Time           0.497
     +-----------------------------------------------------------------------------------------------------------+
     |                    Instance                    |     Arc     |   Cell   | Delay | Arrival | Required |
     |                                                |             |          |       |  Time   |   Time   |
     |------------------------------------------------+-------------+----------+-------+---------+----------|
     | processing_u0/i_in_data_2_r_reg_0_             | CK ^        |          |       |   0.497 |    0.556 |
     | processing_u0/i_in_data_2_r_reg_0_             | CK ^ -> Q v | DFFRX1   | 0.691 |   1.188 |    1.248 |
     | processing_u0/U1840                            | B v -> Y ^  | MXI2X2   | 0.526 |   1.714 |    1.773 |
     | processing_u0/U5281                            | A ^ -> Y ^  | XOR2X1   | 0.341 |   2.055 |    2.114 |
     | processing_u0/U2160                            | A ^ -> Y ^  | CLKMX2X2 | 0.266 |   2.320 |    2.380 |
     | processing_u0/U600                             | B ^ -> CO ^ | ADDHX1   | 0.199 |   2.520 |    2.579 |
     | processing_u0/U5603                            | B ^ -> Y v  | NAND2X1  | 0.131 |   2.651 |    2.710 |
     | processing_u0/U9597                            | A1 v -> Y ^ | OAI21X2  | 0.190 |   2.841 |    2.900 |
     | processing_u0/U9599                            | A1 ^ -> Y v | AOI21X1  | 0.151 |   2.991 |    3.051 |
     | processing_u0/U9600                            | B0 v -> Y ^ | OAI21X4  | 0.132 |   3.124 |    3.183 |
     | processing_u0/U158                             | A ^ -> Y v  | INVX3    | 0.107 |   3.231 |    3.290 |
     | processing_u0/U11499                           | A0 v -> Y ^ | OAI21X1  | 0.138 |   3.369 |    3.428 |
     | processing_u0/U2302                            | A ^ -> Y ^  | XNOR2X1  | 0.182 |   3.551 |    3.610 |
     | processing_u0/add_tree_small_stage2_out_reg_2__1__ | D ^         | DFFRX1   | 0.000 |   3.551 |    3.610 |
     | 12_                                            |             |          |       |         |          |
     +-----------------------------------------------------------------------------------------------------------+
```

⇨ The critical path is “reg to reg”, with slack of 0.059 ns.

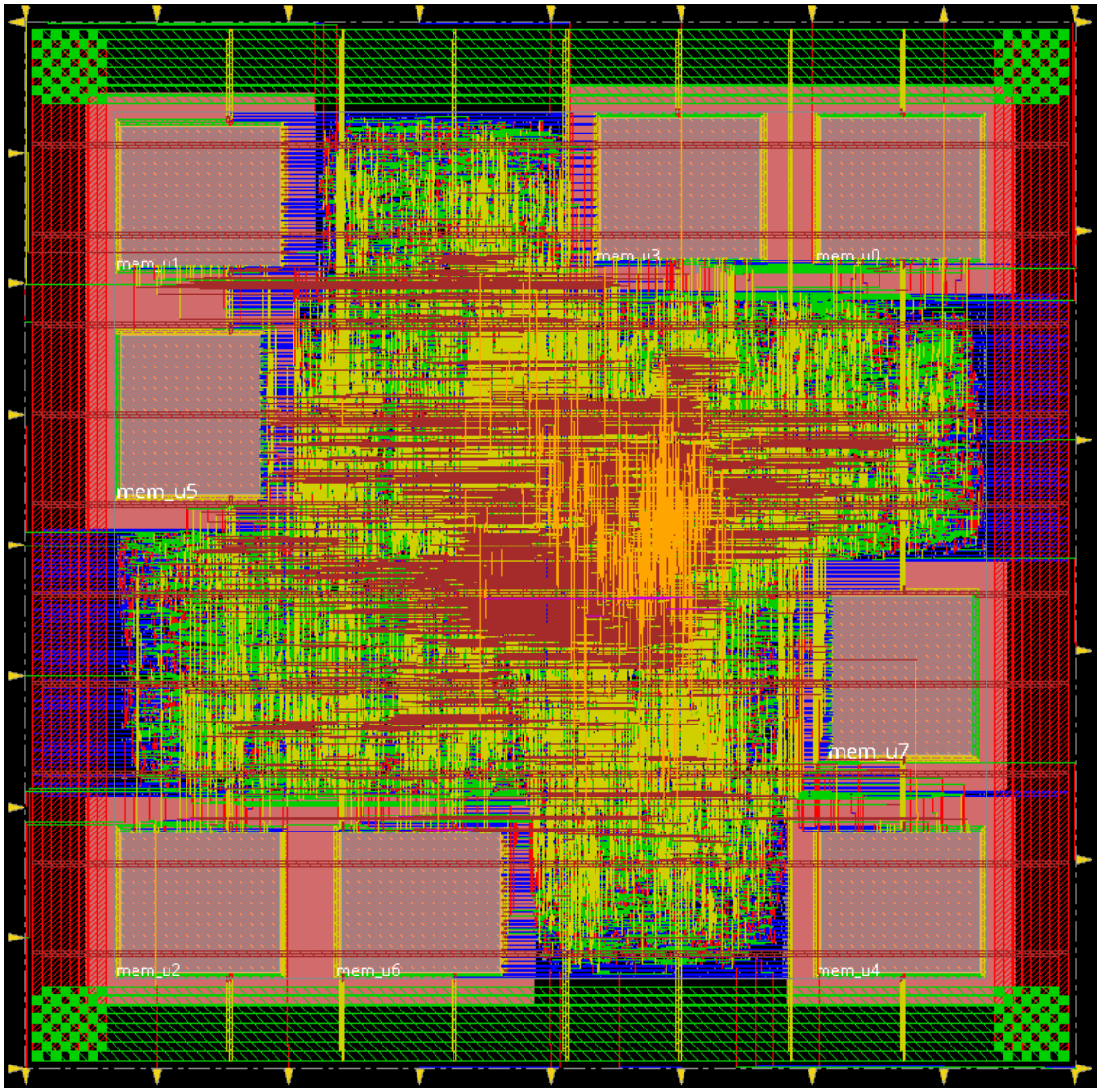
5. Attach the snapshot of GDS stream out messages. (10%)

```
Merging with GDS libraries
Scanning GDS file library/gds/tsmc13gfsg_fram.gds to register cell name ......
Scanning GDS file library/gds/tpz013g3_v1.1.gds to register cell name ......
Scanning GDS file library/gds/sram_256x8.gds to register cell name ......
Merging GDS file library/gds/tsmc13gfsg_fram.gds ......
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has version number: 5.
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file library/gds/tpz013g3_v1.1.gds ......
        ****** Merge file: library/gds/tpz013g3_v1.1.gds has version number: 5.
        ****** Merge file: library/gds/tpz013g3_v1.1.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file library/gds/sram_256x8.gds ......
        ****** Merge file: library/gds/sram_256x8.gds has version number: 5.
        ****** Merge file: library/gds/sram_256x8.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
######Streamout is finished!
```

6. Attach the snapshot of the final area result. (5%)

```
************************* Analyze Floorplan ***************************
    Die Area(um^2)              : 872808.36
    Core Area(um^2)             : 598829.14
    Chip Density (Counting Std Cells and MACROs and IOs): 56.604%
    Core Density (Counting Std Cells and MACROs): 82.502%
    Average utilization         : 100.000%
    Number of instance(s)       : 45449
    Number of Macro(s)          : 8
    Number of IO Pin(s)         : 33
    Number of Power Domain(s) : 0
************************* Estimation Results **************************
***********************************************************************
```

7. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

   In my design, I use **eight 256x8 SRAMs**. To ensure a sufficient power supply for hard macros and reserve core center for standard cell placement, SRAMs are placed at the boundary of the core. Moreover, I equally divide eight SRAMs into four corners. This balanced placement of hard macros possibly reduce congestion and easily achieve timing closure requirement. Last but not least, I reserve additional spaces between adjacent SRAMs. These sparse regions enable a more flexible routing between hard macros and standard cells.