

VLSI System Design (Graduate Level)

Fall 2023

HOMEWORK II

REPORT

Must do self-checking before submission:

- Compress all files described in the problem into one tar
- All SystemVerilog files can be compiled under SoC Lab environment
- All port declarations comply with I/O port specifications
- Organize files according to File Hierarchy Requirement
- No any waveform files in deliverables

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I. Summary

本次作業實作 CPU wrapper、SRAM wrapper 與 AXI bridge，CPU 使用第一次作業實作的 RISC-V pipelined CPU 進行修改，使 CPU 能夠透過 AXI 通道與 SRAM 進行資料傳輸和溝通，實作後先經由 rtl 驗證，並使用 JasperGold VIP 驗證 CPU wrapper、SRAM wrapper 與 AXI bridge 是否通過 assert 驗證，通過後進行電路合成，並完成合成後模擬的驗證。

II. System Structure & State diagram

i. CPU + AXI :

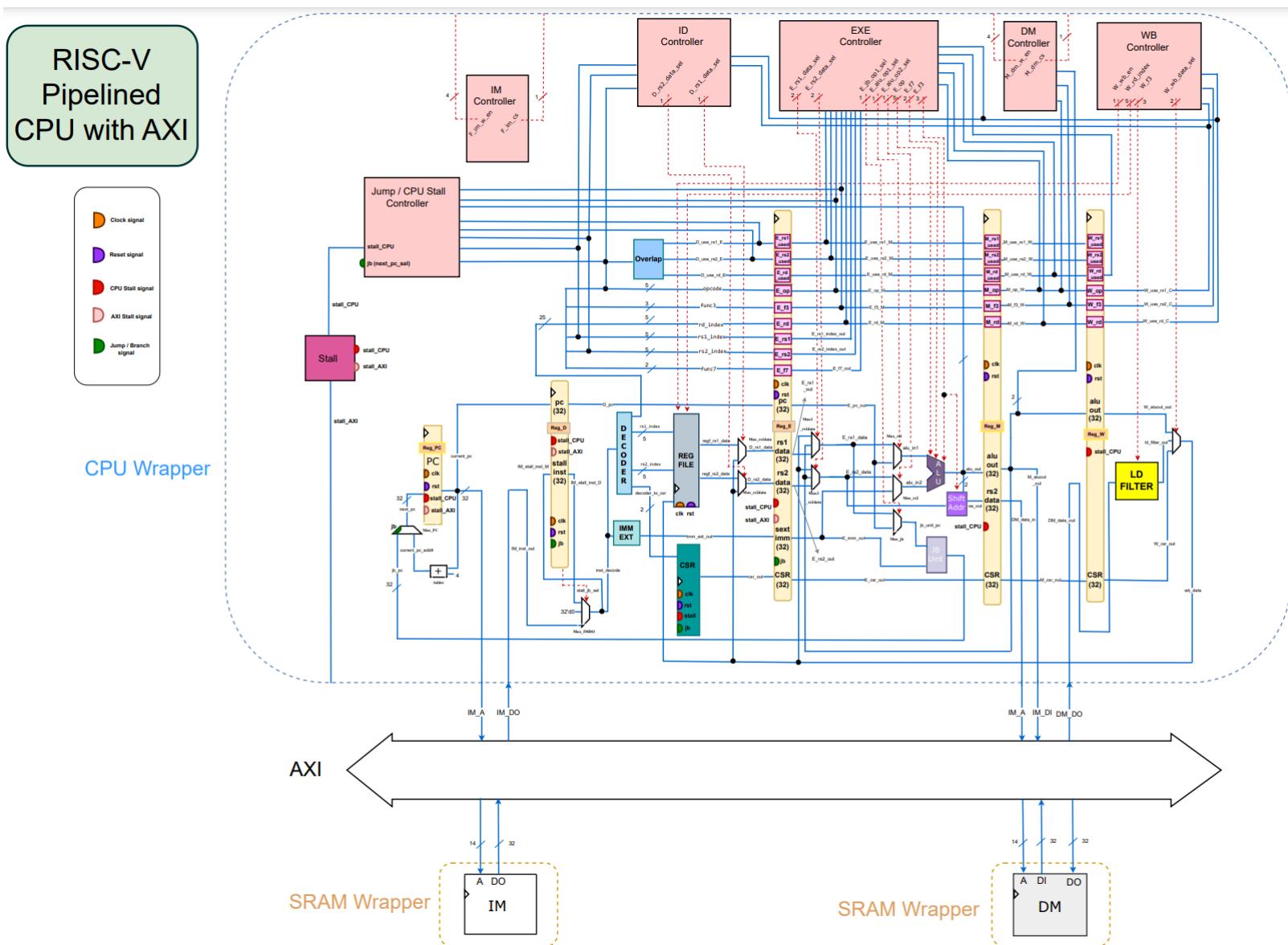


Fig. 1. System Structure

i. CPU wrapper 功能說明與有限狀態機設計：

CPU 為了能夠接上 AXI protocol，需實作 CPU wrapper 將 RISC V pipelined CPU 包裝，使其能夠接上 AXI bridge，CPU wrapper 在此情況會扮演 Master 的角色，實作上會將原本直接接到 IM 與 DM 的訊號送進 CPU wrapper，並將 CPU 對 IM 令為 Master 0、CPU 對 DM 令為 Master 1，CPU wrapper 再透過 AXI bridge 的 Slave interface 進行資料傳輸，在 CPU wrapper 中會透過 FSM 控制 Master 0 與 Master 1 的狀態，並進行資料暫存的處理，以下為 CPU wrapper 的 FSM 設計：

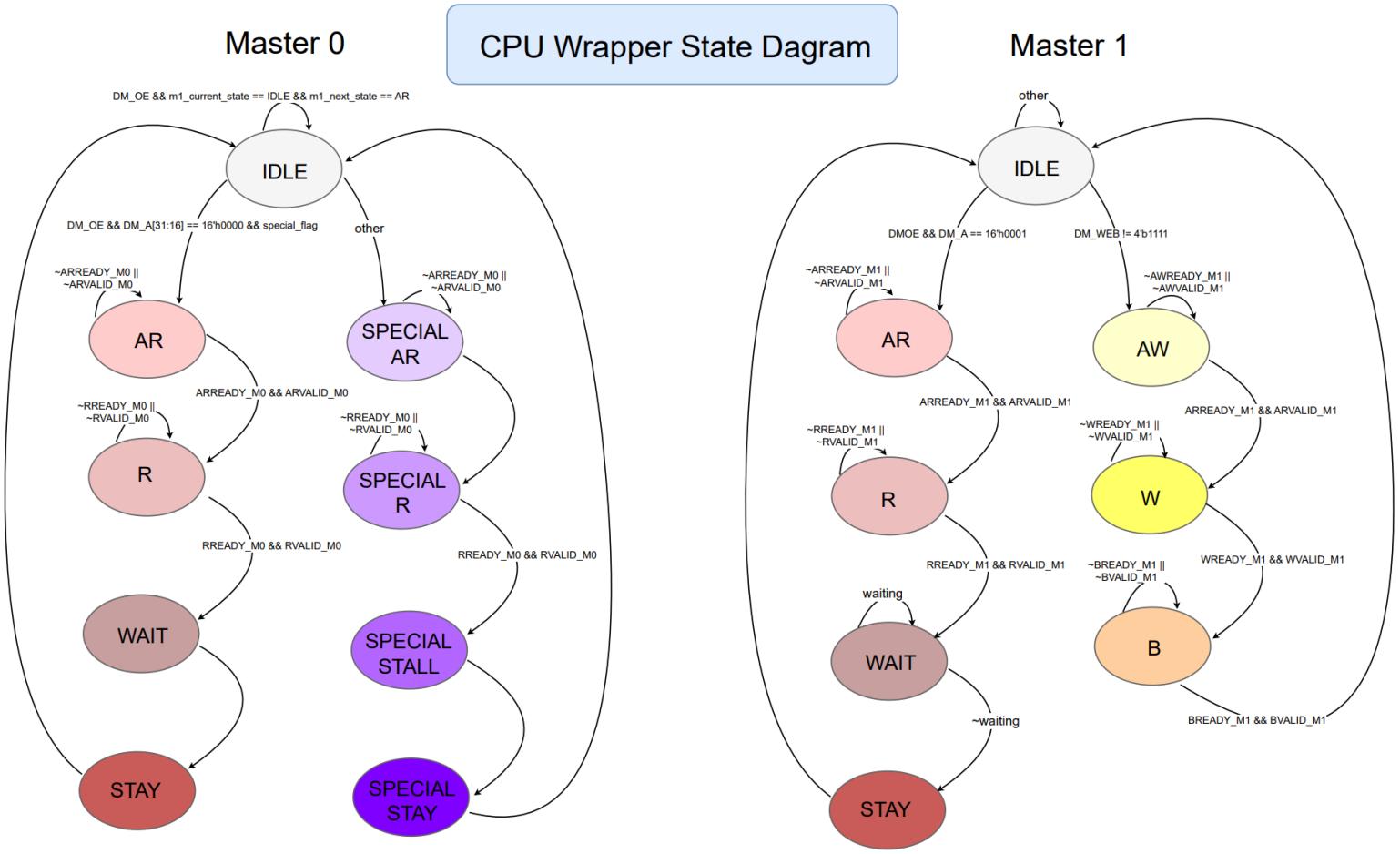


Fig. 2. CPU Wrapper FSM State Diagram

為了能夠使 Master 0 與 Master 1、Master 0 與 Slave 0、Master 1 與 Slave 1 的狀態各自對齊，設計了兩個額外的狀態 WAIT 和 STAY，在 Master 0 也設計了 4 個特殊狀態以應對測資中的特殊情形。

ii. SRAM wrapper 功能說明與有限狀態機設計

SRAM 為了能夠接上 AXI protocol，需實作 SRAM wrapper 將原本的 IM 和 DM 個別包裝，使 IM 與 DM 能夠接上 AXI bridge，SRAM wrapper 在此會作為 Slave 的角色，實作上會將原本 IM 與 DM 直接接到 CPU 的訊號送進 SRAM wrapper，並將 IM 對 CPU 令為 Slave 0、DM 對 CPU 令為 Slave 1，SRAM wrapper 再透過 AXI bridge 的 Master interface 進行資料傳輸，在 SRAM wrapper 中會透過 FSM 控制 Slave 0 與 Slave 1 的狀態，並進行資料暫存的處理，以下為 SRAM wrapper 的 FSM 設計：

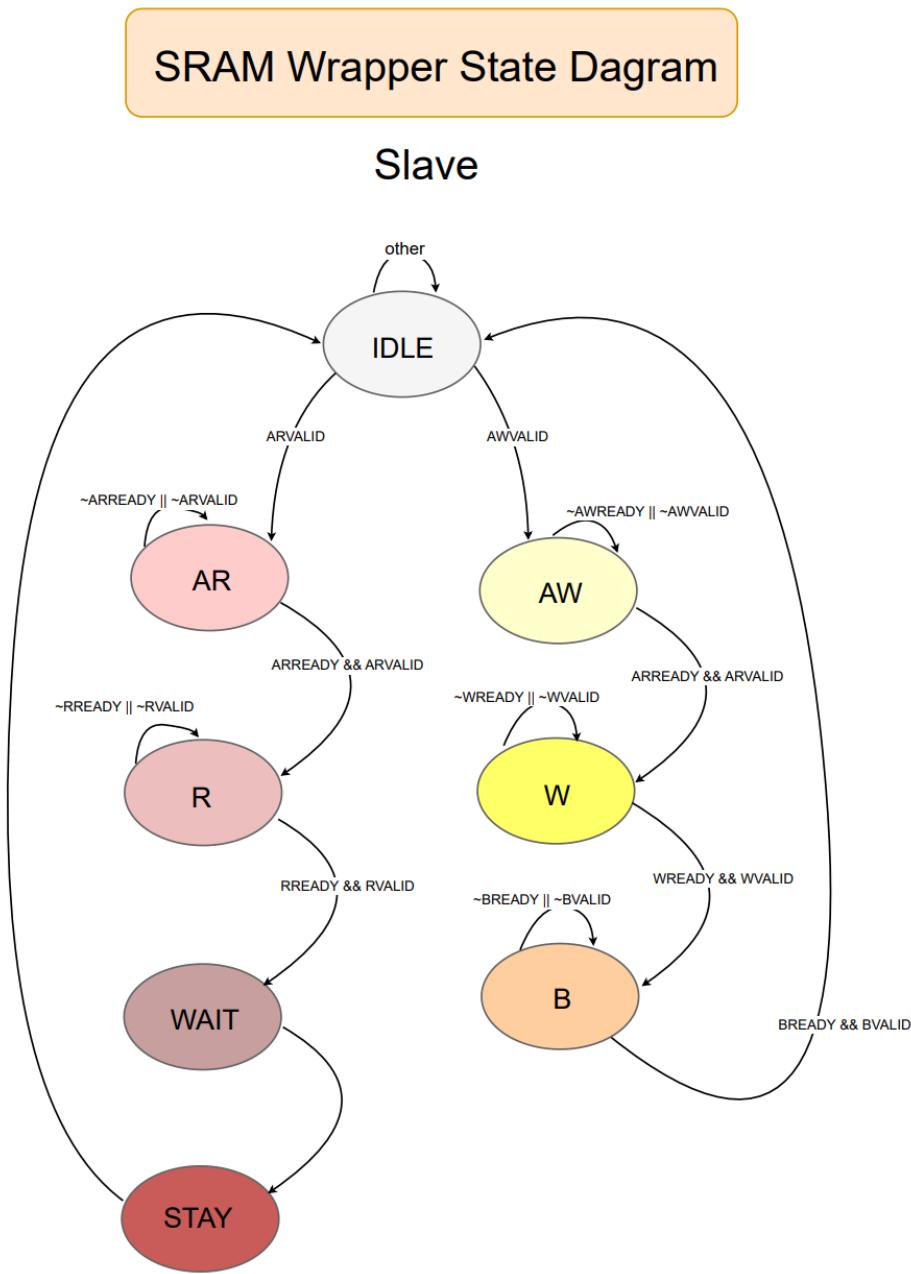


Fig. 3. SRAM Wrapper FSM State Diagram

iii. AXI Bridge
1. AR channel

AR Channel

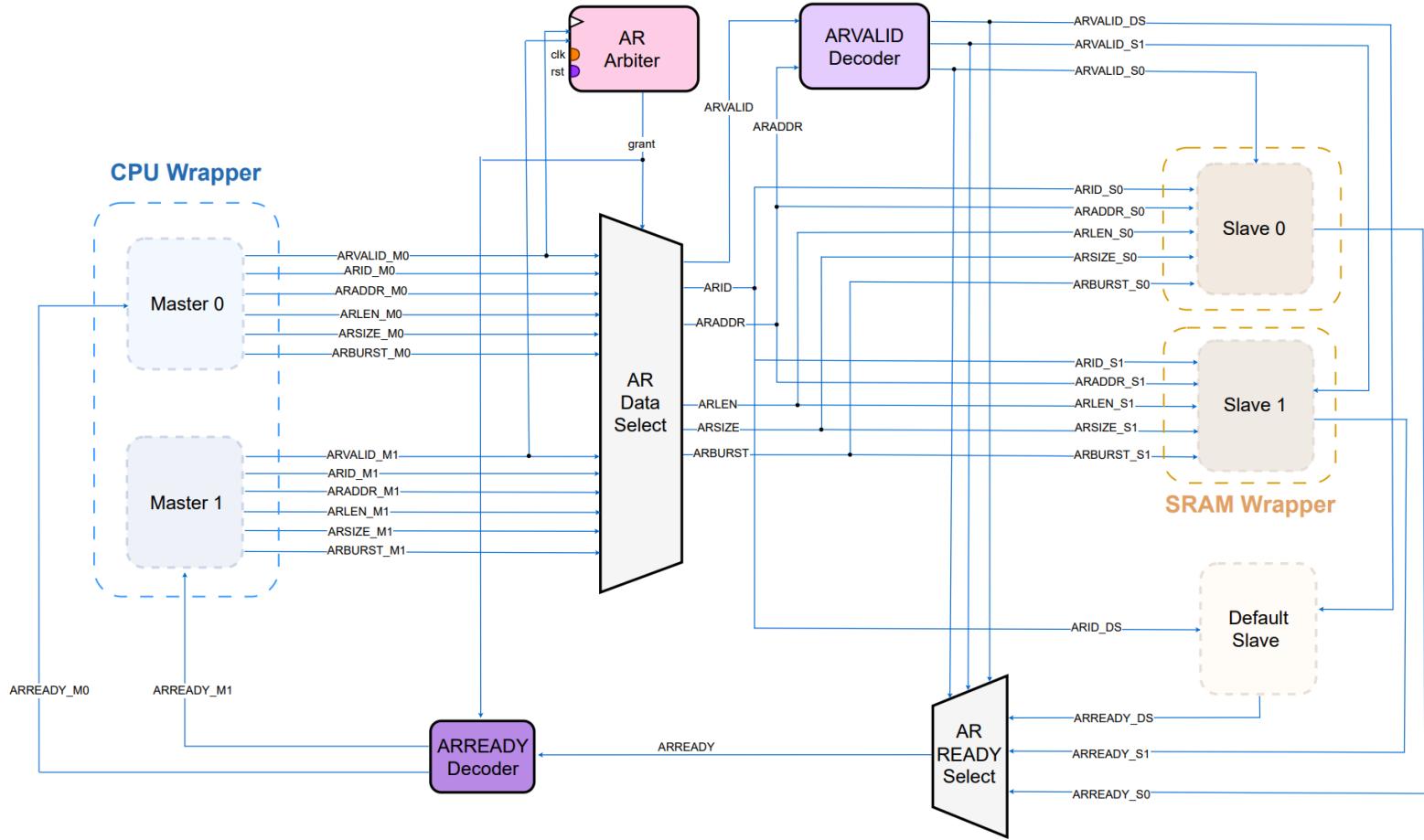


Fig. 4. AR Channel

由於在 Load 指令 Master 0 與 Master 同時需要讀取資料，會產生競爭 AR 通道的情形，因此 AR Channel 中需要設計 Arbiter，在判斷 Valid 訊號來源為哪個 Master 後送出 grant 訊號，讓正確的 Master 訊號能夠通過 AR Data Mux，並將 ARVALID 送入 ARVALID Decoder，ARVALID Decoder 會根據 ARADDR 的位址選擇要將 ARVALID 訊號送入正確的 Slave。Slave 端在接收 ARVALID 後會送出相對應的 ARREADY 訊號到經過 ARREADY MUX 及 ARREADY Decoder，最後將 ARREADY 送回給正確的 Master。

2. R channel

R Channel

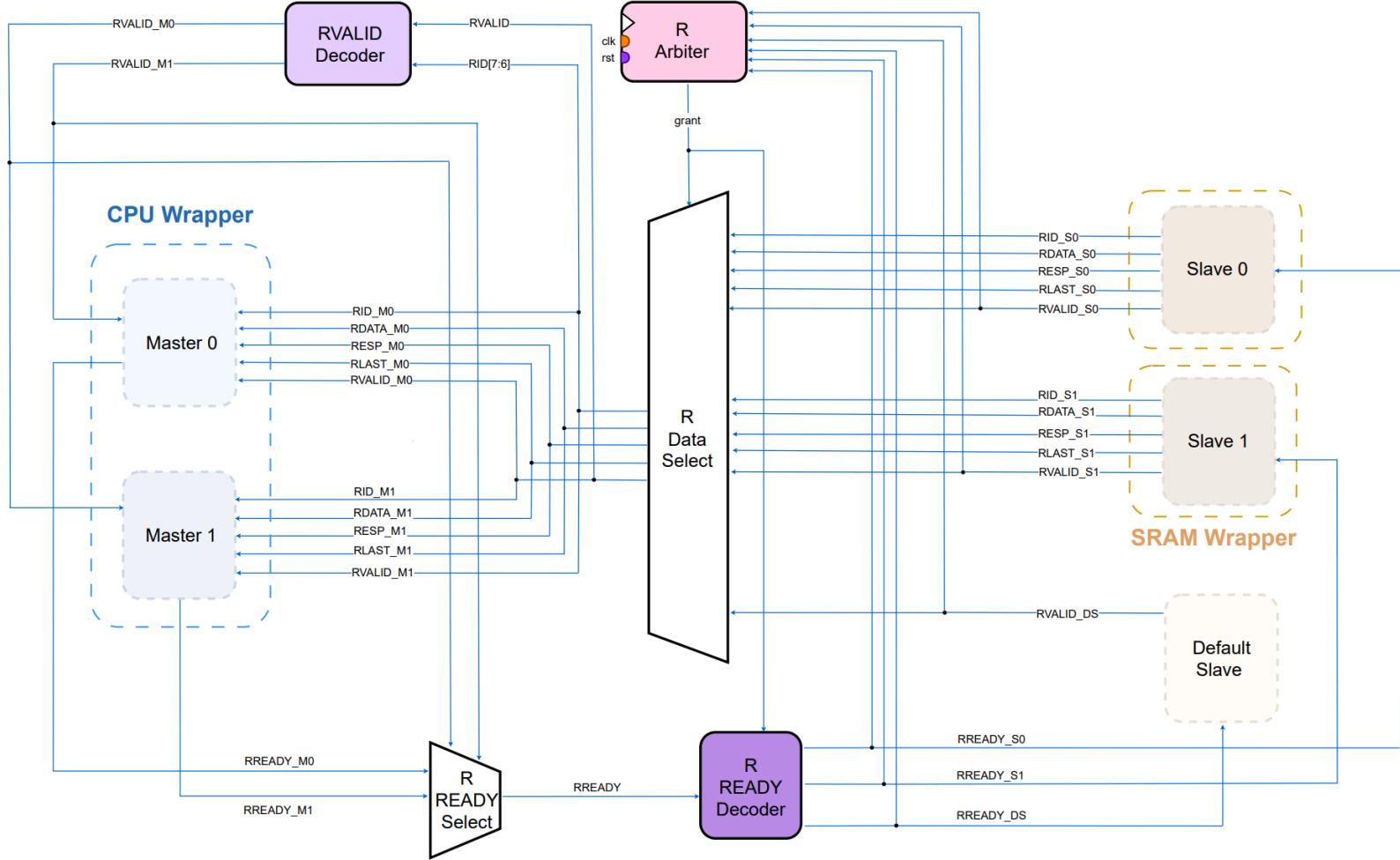


Fig. 5. R Channel

由於在 Load 指令 Slave 0 與 Slave1 同時需要回傳資料，會產生競爭 R 通道的情形，因此 R Channel 中需要設計 Arbiter，在判斷 Valid 訊號來源為哪個 Slave 後送出 grant 訊號，讓正確的 Slave 訊號能夠通過 R Data Mux，並將 RVALID 送入 RVALID Decoder，RVALID Decoder 會根據 RID 選擇要將 RVALID 訊號送入正確的 Master。Master 端在接收 RVALID 後會送出相對應的 RREADY 訊號到 RREADY Decoder 及 RREADY Decoder，最後將 RREADY 送給正確的 Slave。

3. AW Channel

AW Channel

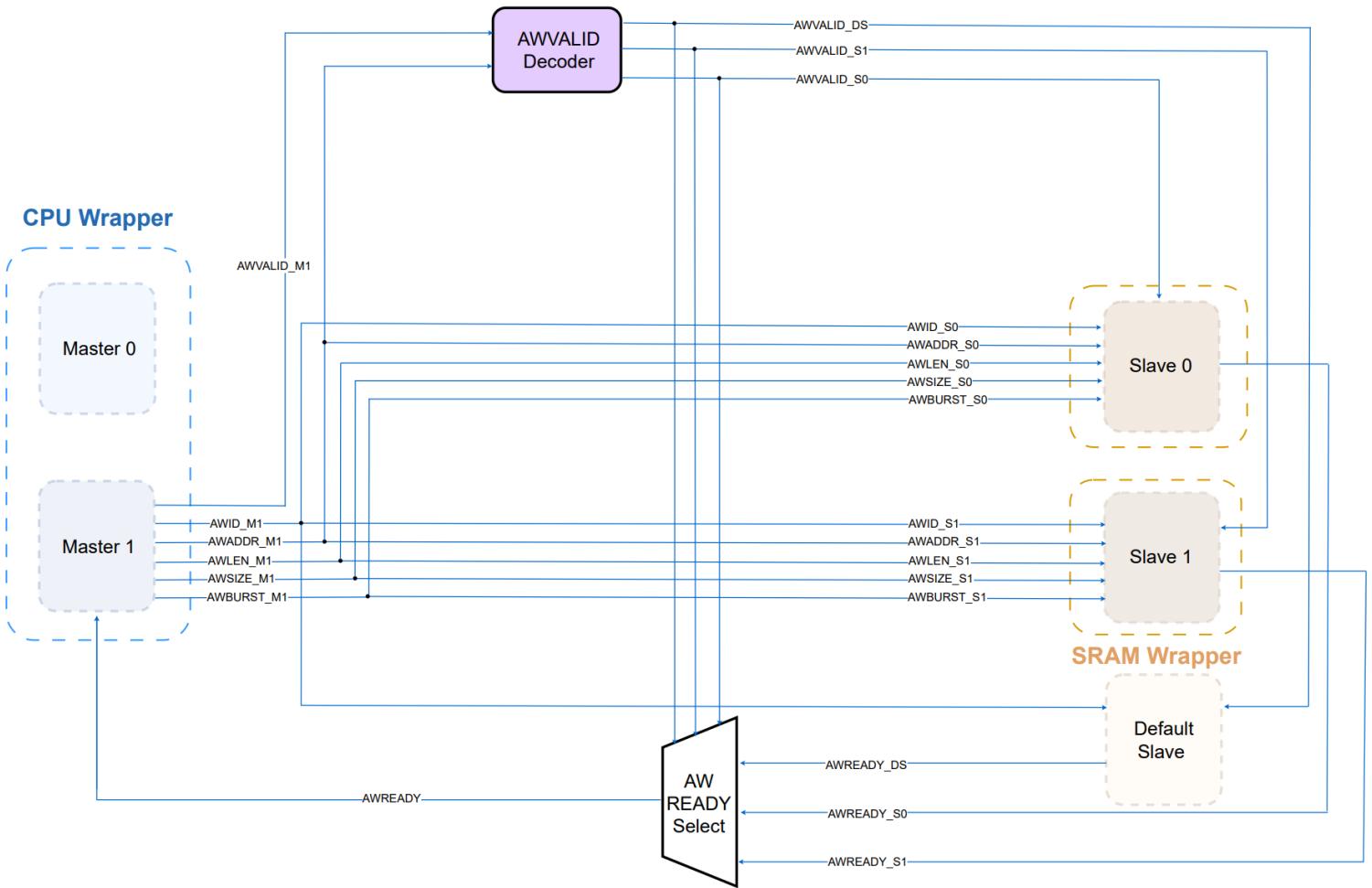


Fig. 6. AW Channel

由於只有 DM 需要執行 Store 指令，因此 AW Channel 只需要接上 MASTER 1 的訊號，不需要 Arbiter 仲裁，AWVALID Decoder 會根據 AWADDR[31:16] 選擇要將 AWVALID 訊號送入哪一個 Slave。Slave 端也會在接收 AWVALID 後送出相對應的 AWREADY 訊號，透過 MUX 將 AWREADY 送回給 Master 1。

4. W Channel

W Channel

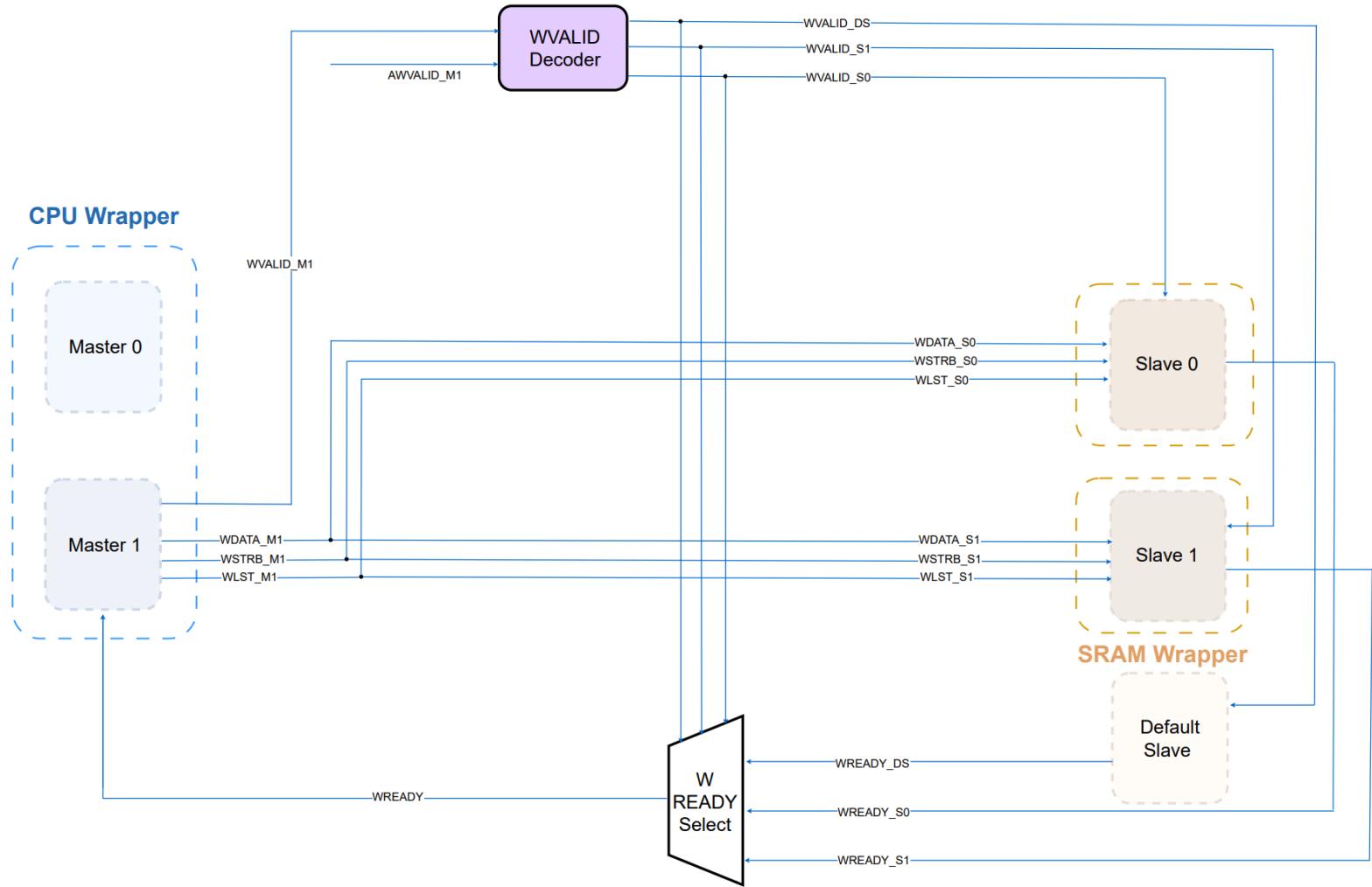


Fig. 7. W Channel

由於只有 DM 需要執行 Store 指令，因此 W Channel 只需要接上 MASTER 1 的訊號，不需要 Arbiter 仲裁，WVALID Decoder 會根據 Master1 的 AWVALID 和 WVALID 的值選出正確的 WVALID，再透過 AWADDR[31:16] 選擇要將 WVALID 訊號送入哪一個 Slave。Slave 端也會在接收 WVALID 後送出相對應的 WREADY 訊號，透過 MUX 將 WREADY 送回給 Master 1。

5. B channel

B Channel

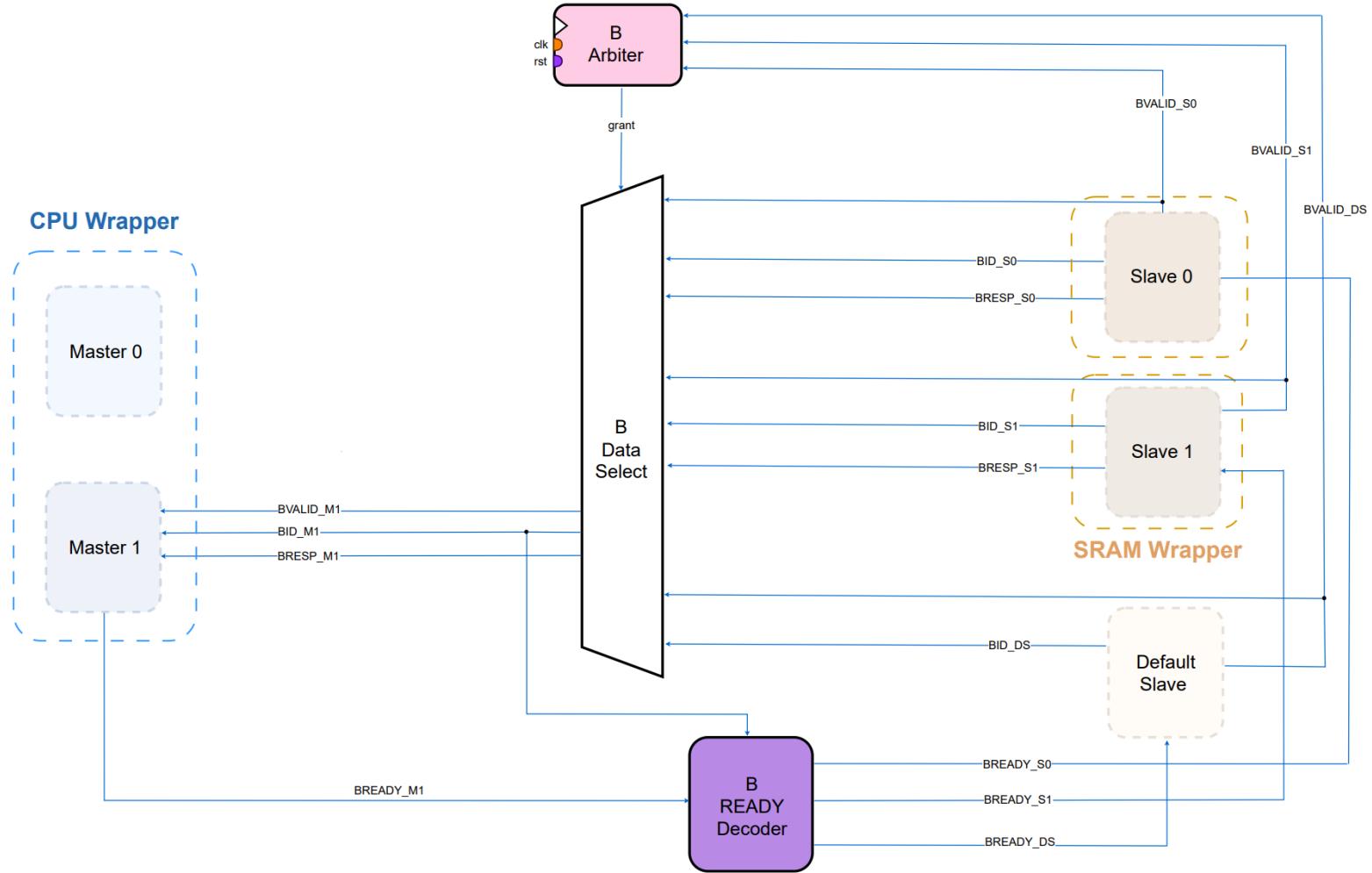


Fig. 8. B Channel

在 B Channel 中，BREADY Decoder 會根據 Master 1 的 BID 選擇 BREADY 訊號，並決定要送給那一個 Slave。Slave 端也會在接收 BREADY 後送出相對應的 BVALID 和 B Channel 的 Data 訊號，透過 B Arbiter 的 grant 選擇將 B Channel 的 Data 送回給 Master 1。

III. Waveform Explanation

本次 CPU 與 AXI 的溝通共有四種情形，以下為四種情形的解釋：

- (1) 除了 Load 與 Store 以外的指令：IM 會進行讀取的狀態跳轉，DM 則停留在 Idle 狀態，CPU Wrapper 與 SRAM Wrapper 的波形分別如下：

Master 0: Read

Master 1: Keep Idle

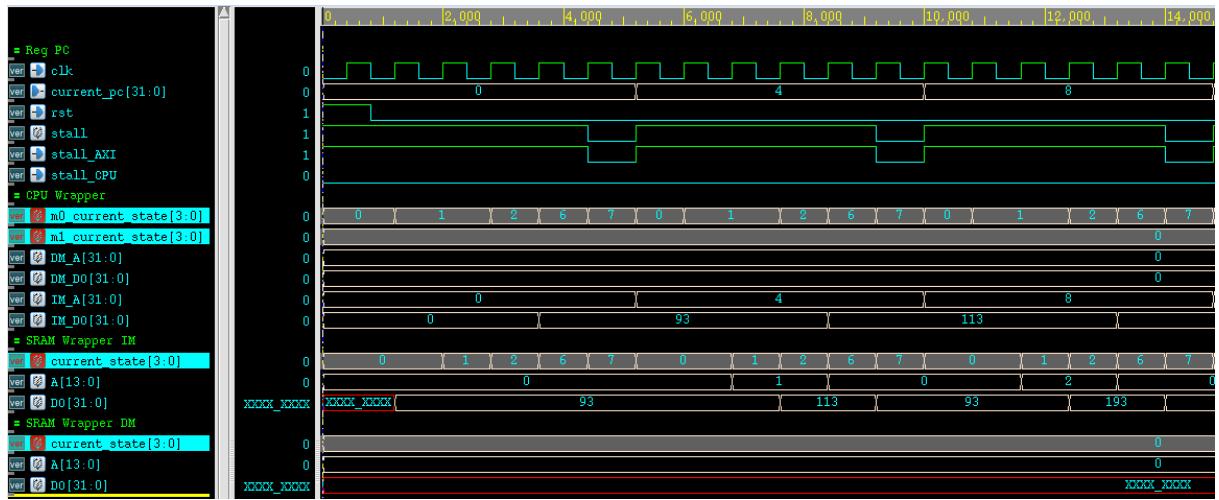


Fig. 9. M0 Read M1 Keep Idle Waveform

- (2) Load 指令：IM 與 DM 皆會進行讀取的狀態跳轉，在競爭 AR 通道的情形下設定為 DM 先讀取，接著 IM 慢一個 Cycle 開始讀取，DM 先讀取完後會在 Wait 狀態等待 IM，最後一起跳回 IDLE，CPU Wrapper 與 SRAM Wrapper 的波形分別

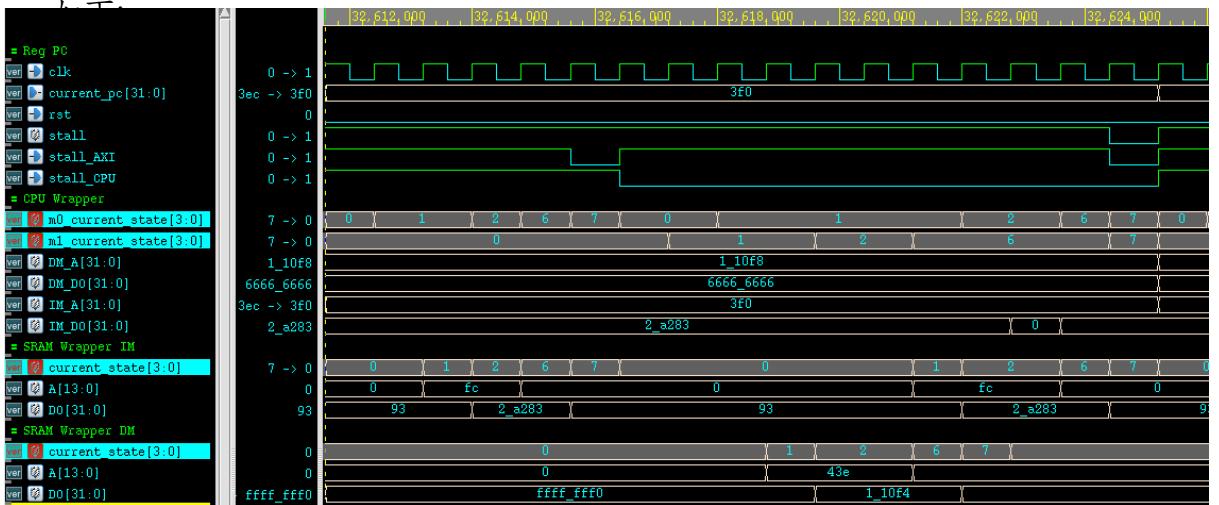


Fig. 10. M0 Read M1 Read Waveform

(3) Load 指令: IM 會進行讀取的狀態跳轉, DM 則進行寫入的狀態跳轉, CPU Wrapper 與 SRAM Wrapper 的波形分別如下(紅框的部分):

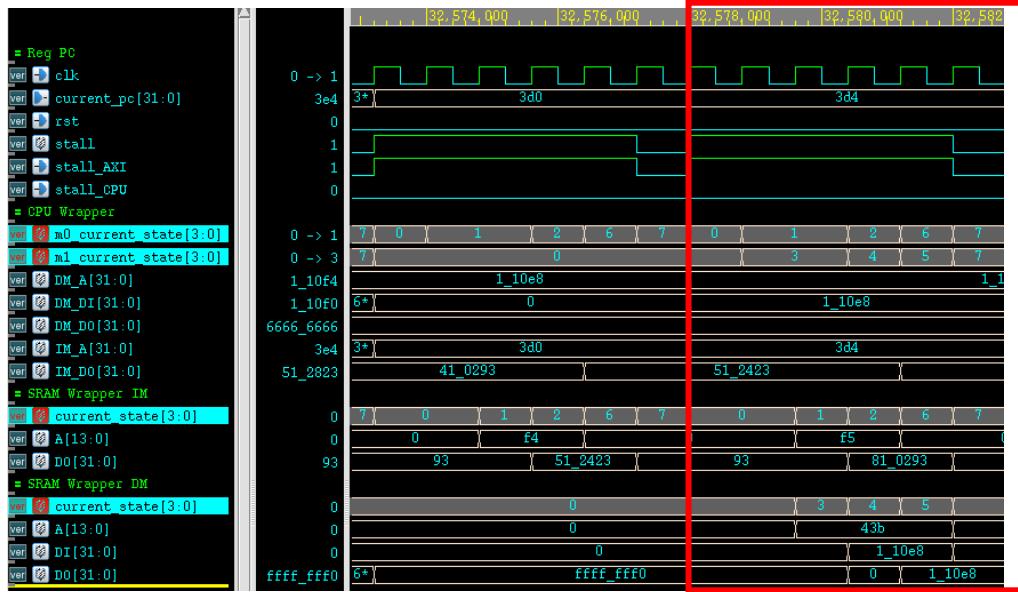


Fig. 11. M0 Read M1 Write Waveform

(4) 特殊情形：由於 DM 需要讀取的地址為 IM 的地址，需要到 IM 讀取並把讀取出
來的資料交由 DM，在此情形 IM 共會進行兩次讀取的狀態跳轉，第一次為特
殊讀取，第二次則為一般讀取，DM 則停留在 Idle，CPU Wrapper 與 SRAM
Wrapper 的波形分別如下：

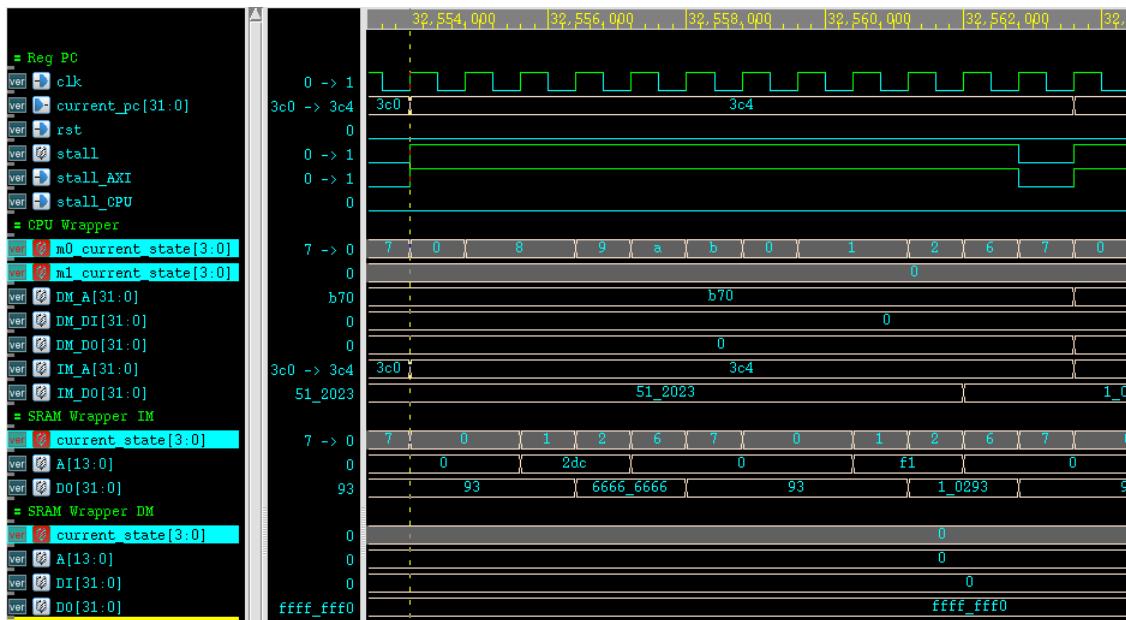


Fig. 12. Special Case Waveform

IV. Verification

i. Problem 1

利用 JasperGold 的 Verification IP 分別去驗證 CPU Wrapper、AXI、SRAM Wrapper

(1) CPU Wrapper (Master)

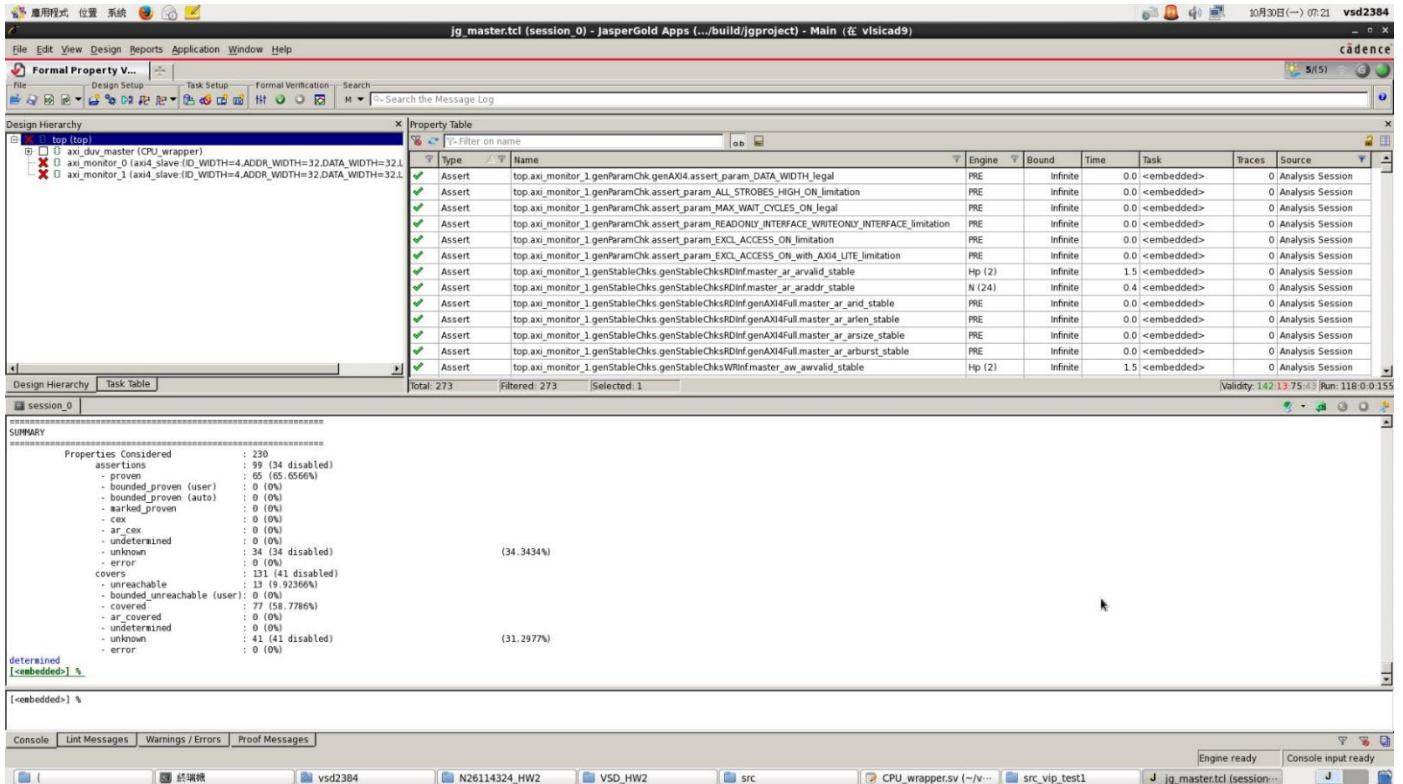


Fig. 12. CPU Wrapper JasperGold Verification IP

CPU Wrapper 的 VIP 驗證 Assertion 可全數通過，但出現 13 個 Cover (related) 問題，13 個 Cover (related) 產生的原因皆是在(rvalid && !ready)的情況下，Read 通道的 Data 需要保持穩定，但這個情況在 Handshake 機制下可保證資料正確，因此實際上不會產生此錯誤，以下分別列出這 13 個錯誤：



Fig. 13. CPU Wrapper Cover (related) 1

J Property "<embedded>::top.axi_monitor_1.genStableChks.genStableChksRDInf.slave_r_rdata_stable:precondition1" (在 vlsicad9)

Type	Cover
Name	<embedded>::top.axi_monitor_1.genStableChks.genStableChksRDInf.slave_r_rdata_stable.precondition1
Task	<embedded>
Instance	axi_monitor_1
Expression	axi_monitor_1.genStableChks.genStableChksRDInf.slave_r_rdata_stable.precondition1
Status	X Unreachable
Time	0.6
Filename	/usr/cad/cadence/VIPCAT/cur/tools/abvip/axi4/rtl/cdn_abvip_axi4_slave.svp

```

5970 slave_r_rdata_stable: assume property (
5971   (rvalid && !rready) |=> $stable(rdata_mask)
5972   else $display ("%t: rdata should remain stable if rvalid and !rready; ARM IHI 0022F: Section A3.2.1 on pg A3-41",$time);

```

Close

Fig. 14. CPU Wrapper Cover (related) 2

J Property "<embedded>::top.axi_monitor_1.genStableChks.genStableChksRDInf.genAXI4Full.slave_r_rllast_stable:precondition1" (在 vlsicad9)

Type	Cover
Name	<embedded>::top.axi_monitor_1.genStableChks.genStableChksRDInf.genAXI4Full.slave_r_rllast_stable.precondition1
Task	<embedded>
Instance	axi_monitor_1
Expression	axi_monitor_1.genStableChks.genStableChksRDInf.genAXI4Full.slave_r_rllast_stable.precondition1
Status	X Unreachable
Time	0.6
Filename	/usr/cad/cadence/VIPCAT/cur/tools/abvip/axi4/rtl/cdn_abvip_axi4_slave.svp

```

6030 slave_r_rllast_stable: assume property (
6031   (rvalid && !rready) |=> $stable(rlast))
6032   else $display ("%t: rllast should remain stable if rvalid and !rready; ARM IHI 0022F: Section A3.2.1 on pg A3-41",$time);

```

Close

Fig. 15. CPU Wrapper Cover (related) 3

J Property "<embedded>::top.axi_monitor_1.genStableChks.genStableChksRDInf.genAXI4Full.slave_r_rid_stable:precondition1" (在 vlsicad9)

Type	Cover
Name	<embedded>::top.axi_monitor_1.genStableChks.genStableChksRDInf.genAXI4Full.slave_r_rid_stable.precondition1
Task	<embedded>
Instance	axi_monitor_1
Expression	axi_monitor_1.genStableChks.genStableChksRDInf.genAXI4Full.slave_r_rid_stable.precondition1
Status	X Unreachable
Time	0.6
Filename	/usr/cad/cadence/VIPCAT/cur/tools/abvip/axi4/rtl/cdn_abvip_axi4_slave.svp

```

6035 slave_r_rid_stable: assume property (
6036   (rvalid && !rready) |=> $stable(rid))
6037   else $display ("%t: rid should remain stable if rvalid and !rready; ARM IHI 0022F: Section A3.2.1 on pg A3-41",$time);

```

Close

Fig. 16. CPU Wrapper Cover (related) 4

J Property "<embedded>::top.axi_monitor_1.genStableChks.genStableChksWRInf.slave_b_bvalid_stable:precondition1" (在 vlsicad9) x

Type	Cover
Name	<embedded>::top.axi_monitor_1.genStableChks.genStableChksWRInf.slave_b_bvalid_stable:precondition1
Task	<embedded>
Instance	axi_monitor_1
Expression	axi_monitor_1.genStableChks.genStableChksWRInf.slave_b_bvalid_stable:precondition1
Status	✗ Unreachable
Time	0.1
Engine	N (34)
Filename	/usr/cad/cadence/VIPCAT/cur/tools/abvip/axi4/rtl/cdn_abvip_axi4_slave.svp

```

6166 slave_b_bvalid_stable: assume property (
6167   (bvalid && !bready) |=> $valid)
6168   else $display ("@%t: bvalid should remain stable if bvalid and !bready; ARM IHI 0022F: Section A3.2.2 on pg A3-43", $time);

```

Close

Fig. 17. CPU Wrapper Cover (related) 5

J Property "<embedded>::top.axi_monitor_1.genStableChks.genStableChksWRInf.slave_b_bresp_stable:precondition1" (在 vlsicad9) x

Type	Cover
Name	<embedded>::top.axi_monitor_1.genStableChks.genStableChksWRInf.slave_b_bresp_stable:precondition1
Task	<embedded>
Instance	axi_monitor_1
Expression	axi_monitor_1.genStableChks.genStableChksWRInf.slave_b_bresp_stable:precondition1
Status	✗ Unreachable
Time	0.1
Engine	N (34)
Filename	/usr/cad/cadence/VIPCAT/cur/tools/abvip/axi4/rtl/cdn_abvip_axi4_slave.svp

```

6171 slave_b_bresp_stable: assume property (
6172   (bvalid && !bready) |=> $stable(bresp))
6173   else $display ("@%t: bresp should remain stable if bvalid and !bready; ARM IHI 0022F: Section A3.2.2 on pg A3-43", $time);

```

Close

Fig. 18. CPU Wrapper Cover (related) 6

J Property "<embedded>::top.axi_monitor_1.genStableChks.genStableChksWRInf.genAXI4Full.slave_b_bid_stable:precondition1" (在 vlsicad9) x

Type	Cover
Name	<embedded>::top.axi_monitor_1.genStableChks.genStableChksWRInf.genAXI4Full.slave_b_bid_stable:precondition1
Task	<embedded>
Instance	axi_monitor_1
Expression	axi_monitor_1.genStableChks.genStableChksWRInf.genAXI4Full.slave_b_bid_stable:precondition1
Status	✗ Unreachable
Time	0.1
Engine	N (34)
Filename	/usr/cad/cadence/VIPCAT/cur/tools/abvip/axi4/rtl/cdn_abvip_axi4_slave.svp

```

6238 slave_b_bid_stable: assume property (
6239   (bvalid && !bready) |=> $stable(bid))
6240   else $display ("@%t: bid should remain stable if bvalid and !bready; ARM IHI 0022F: Section A3.2.1 on pg A3-41", $time);

```

Close

Fig. 19. CPU Wrapper Cover (related) 7

J Property "<embedded>::top.axi_monitor_0.genStableChks.genStableChksRDInf.slave_r_rvalid_stable:precondition1" (在 vlsicad9)

Type	Cover
Name	<embedded>::top.axi_monitor_0.genStableChks.genStableChksRDInf.slave_r_rvalid_stable:precondition1
Task	<embedded>
Instance	axi_monitor_0
Expression	axi_monitor_0.genStableChks.genStableChksRDInf.slave_r_rvalid_stable:precondition1
Status	X Unreachable
Time	0.4
Filename	/usr/cad/cadence/VIPCAT/cur/tools/abvip/axi4/rtl/cdn_abvip_axi4_slave.svp

```

5965 slave_r_rvalid_stable: assume property (
5966   (rvalid && !rready) |=> rvalid
5967   else $display ("%@t: rvalid should remain stable if rvalid and !rready; ARM IHI 0022F: Section A3.2.1 on pg A3-41",$time);

```

Close

Fig. 20. CPU Wrapper Cover (related) 8

J Property "<embedded>::top.axi_monitor_0.genStableChks.genStableChksRDInf.slave_r_rdata_stable:precondition1" (在 vlsicad9)

Type	Cover
Name	<embedded>::top.axi_monitor_0.genStableChks.genStableChksRDInf.slave_r_rdata_stable:precondition1
Task	<embedded>
Instance	axi_monitor_0
Expression	axi_monitor_0.genStableChks.genStableChksRDInf.slave_r_rdata_stable:precondition1
Status	X Unreachable
Time	0.4
Filename	/usr/cad/cadence/VIPCAT/cur/tools/abvip/axi4/rtl/cdn_abvip_axi4_slave.svp

```

5970 slave_r_rdata_stable: assume property (
5971   (rvalid && !rready) |=> $stable(rdata_mask))
5972   else $display ("%@t: rdata should remain stable if rvalid and !rready; ARM IHI 0022F: Section A3.2.1 on pg A3-41",$time);

```

Close

Fig. 21. CPU Wrapper Cover (related) 9

J Property "<embedded>::top.axi_monitor_0.genStableChks.genStableChksRDInf.slave_r_rrresp_stable:precondition1" (在 vlsicad9)

Type	Cover
Name	<embedded>::top.axi_monitor_0.genStableChks.genStableChksRDInf.slave_r_rrresp_stable:precondition1
Task	<embedded>
Instance	axi_monitor_0
Expression	axi_monitor_0.genStableChks.genStableChksRDInf.slave_r_rrresp_stable:precondition1
Status	X Unreachable
Time	0.4
Filename	/usr/cad/cadence/VIPCAT/cur/tools/abvip/axi4/rtl/cdn_abvip_axi4_slave.svp

```

5975 slave_r_rrresp_stable: assume property (
5976   (rvalid && !rready) |=> $stable(rrresp))
5977   else $display ("%@t: rrresp should remain stable if rvalid and !rready; ARM IHI 0022F: Section A3.2.1 on pg A3-41",$time);

```

Close

Fig. 22. CPU Wrapper Cover (related) 10

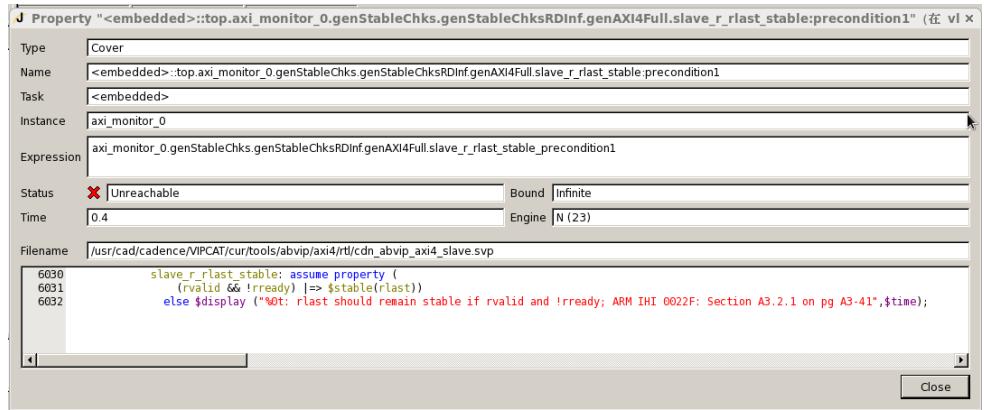


Fig. 23. CPU Wrapper Cover (related) 11

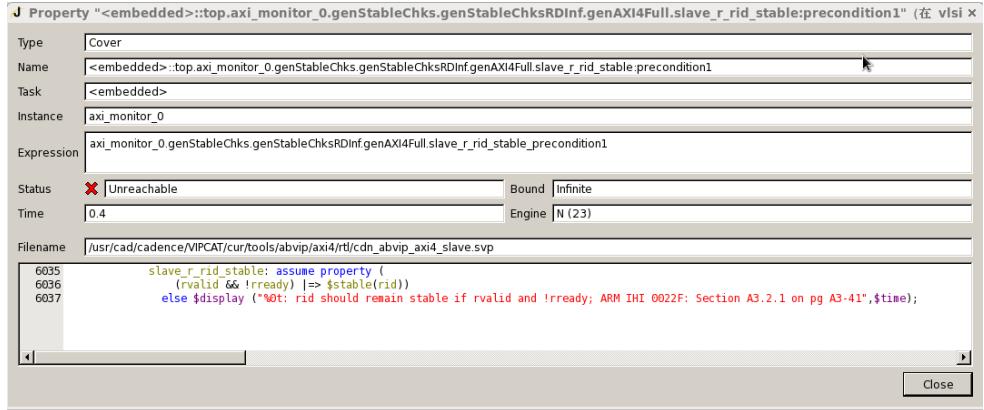


Fig. 24. CPU Wrapper Cover (related) 12



Fig. 25. CPU Wrapper Cover (related) 13

(2) AXI (Bridge)

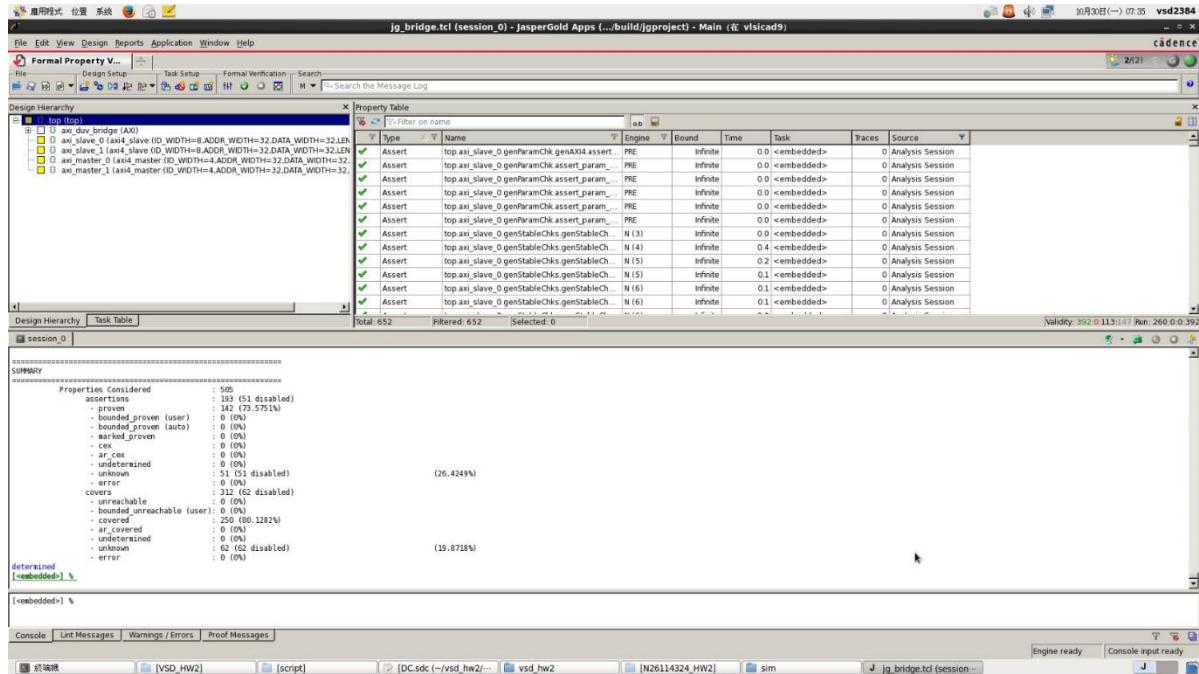


Fig. 26. AXI JasperGold Verification IP

(3) SRAM Wrapper (Slave)

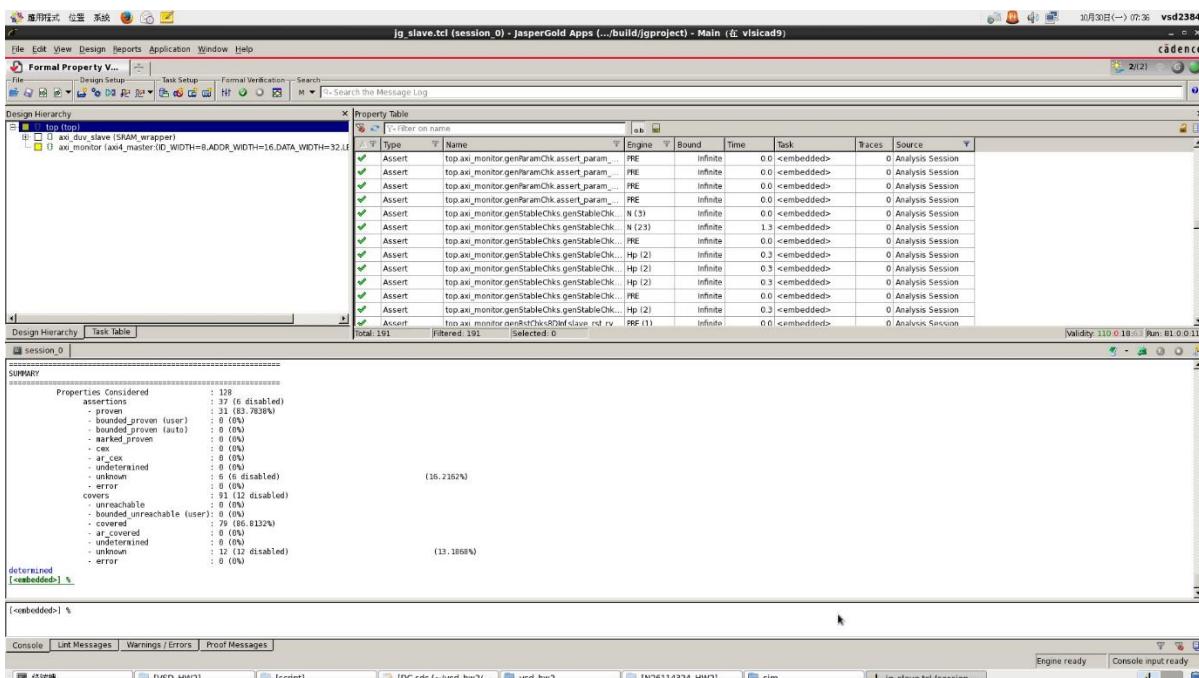


Fig. 27. SRAM Wrapper JasperGold Verification IP

AXI 與 SRAM Wrapper 的 VIP 驗證沒有 Assertion 和 Cover (related) 錯誤。

ii. Problem 2

File Edit View Search Terminal Help

```
DM[ 15] = ffffffcc, pass
DM[ 16] = ffffcccc, pass
DM[ 17] = 000000cc, pass
DM[ 18] = 0000cccc, pass
DM[ 19] = 00000d9d, pass
DM[ 20] = 00000004, pass
DM[ 21] = 00000003, pass
DM[ 22] = 000001a6, pass
DM[ 23] = 00000ec6, pass
DM[ 24] = 2468b7a8, pass
DM[ 25] = 5dbf9f00, pass
DM[ 26] = 00012b38, pass
DM[ 27] = fa2817b7, pass
DM[ 28] = ff000000, pass
DM[ 29] = 12345678, pass
DM[ 30] = 0000f000, pass
DM[ 31] = 00000f00, pass
DM[ 32] = 000000f0, pass
DM[ 33] = 0000000f, pass
DM[ 34] = 56780000, pass
DM[ 35] = 78000000, pass
DM[ 36] = 00005678, pass
DM[ 37] = 00000078, pass
DM[ 38] = 12345678, pass
DM[ 39] = ce780000, pass
DM[ 40] = fffff000, pass
DM[ 41] = fffff000, pass
DM[ 42] = fffff000, pass
DM[ 43] = fffff000, pass
DM[ 44] = fffff000, pass
DM[ 45] = fffff000, pass
DM[ 46] = 1357a274, pass
DM[ 47] = 13578000, pass
DM[ 48] = fffff004, pass
DM[ 49] = 00000000, pass
DM[ 50] = 000013cd, pass

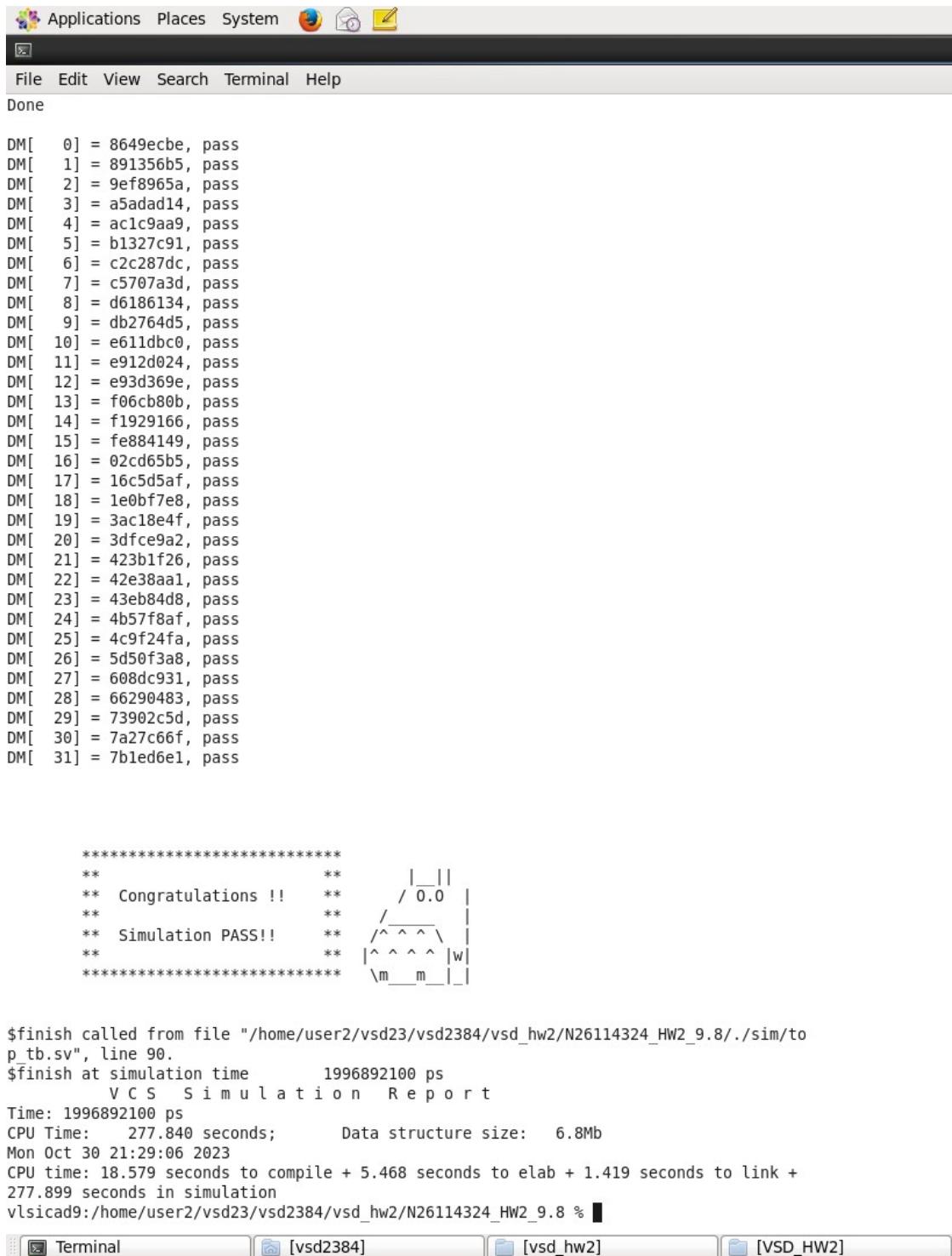
*****
**          **      /_||_
** Congratulations !!  **      / \ 
**          **      / \ 
** Simulation PASS!!  **      | ^ ^ ^ \ 
**          **      | ^ ^ ^ | w |
*****\m__m__|_|
```

\$finish called from file "/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8./sim/top_tb.sv", line 90.
\$finish at simulation time 433860700 ps
V C S S i m u l a t i o n R e p o r t
Time: 433860700 ps
CPU Time: 59.940 seconds; Data structure size: 6.8Mb
Mon Oct 30 21:20:40 2023
CPU time: 22.312 seconds to compile + 5.849 seconds to elab + 1.411 seconds to link + 59.994 seconds in simulation
vlsicad9:/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8 %

Fig. 28. Make syn0 結果

2. Prog 1

Prog1 撰寫排序的 C code，將 array_addr 裡存放的值提取出來存放在 _test_start，根據 array_size 的次數進行比較，並用 bubble sort 演算法排序大小，將數字依大小排序。



```
Done

DM[ 0] = 8649ecbe, pass
DM[ 1] = 891356b5, pass
DM[ 2] = 9ef8965a, pass
DM[ 3] = a5adad14, pass
DM[ 4] = ac1c9aa9, pass
DM[ 5] = b1327c91, pass
DM[ 6] = c2c287dc, pass
DM[ 7] = c5707a3d, pass
DM[ 8] = d6186134, pass
DM[ 9] = db2764d5, pass
DM[ 10] = e611dbc0, pass
DM[ 11] = e912d024, pass
DM[ 12] = e93d369e, pass
DM[ 13] = f06cb80b, pass
DM[ 14] = f1929166, pass
DM[ 15] = fe884149, pass
DM[ 16] = 02cd65b5, pass
DM[ 17] = 16c5d5af, pass
DM[ 18] = 1e0bf7e8, pass
DM[ 19] = 3ac18e4f, pass
DM[ 20] = 3dfce9a2, pass
DM[ 21] = 423b1f26, pass
DM[ 22] = 42e38aa1, pass
DM[ 23] = 43eb84d8, pass
DM[ 24] = 4b57f8af, pass
DM[ 25] = 4c9f24fa, pass
DM[ 26] = 5d50f3a8, pass
DM[ 27] = 608dc931, pass
DM[ 28] = 66290483, pass
DM[ 29] = 73902c5d, pass
DM[ 30] = 7a27c66f, pass
DM[ 31] = 7bled6e1, pass

*****
**          **      |__||_
** Congratulations !!    **      / 0.0   |
**          **      /_____|_
** Simulation PASS!!    **      /^\ ^ ^ \_|
**          **      |^\ ^ ^ ^ |w|_
*****\m___m_|_||

$finish called from file "/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8./sim/to
p_tb.sv", line 90.
$finish at simulation time      1996892100 ps
V C S S i m u l a t i o n R e p o r t
Time: 1996892100 ps
CPU Time: 277.840 seconds;      Data structure size: 6.8Mb
Mon Oct 30 21:29:06 2023
CPU time: 18.579 seconds to compile + 5.468 seconds to elab + 1.419 seconds to link +
277.899 seconds in simulation
vlsicad9:/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8 %
```


Fig. 29. Make syn1 結果

3. Prog2

```
File Edit View Search Terminal Help
if [ -x ./simv ]; then chmod a-x ./simv; fi
g++ -o ./simv -rdynamic -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.dai
dir -Wl,-rpath=/usr/cad/synopsys/vcs/cur/linux64/lib -L/usr/cad/synopsys/vcs/cur/linux
64/lib -Wl,-rpath-link=../ /usr/lib64/libnuma.so.1 objs/amcQw_d.o _9288_archive_1
.so _prev_archive_1.so objs/udps/qndjy.o objs/udps/G0JcM.o objs/udps/Wd2wc.o objs/udps
/keuHx.o objs/udps/Sbaqa.o objs/udps/ySdCA.o objs/udps/xQ3mk.o SIM_l.o rmapats_
mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lvirsim_
-lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/cad/synopsys/
vcs/cur/linux64/lib/vcs tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive
_vcs_pli_stub_.o /usr/cad/synopsys/vcs/cur/linux64/lib/vcs_save_restore_new.
o /usr/cad/synopsys/verdi/cur/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl

..//simv up to date
make[1]: Leaving directory `/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/build/
csrc'
Info: [VCS_SAVE RESTORE_INFO] ASLR (Address Space Layout Randomization) is detected on
the machine. To enable $save functionality, ASLR will be switched off and simv re-exe
cuted.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_IN
FO' to suppress this message.
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64; Oct 30 2
1:30 2023
Doing SDF annotation ..... Done
** MEM_Error: Unknown value occurred ( 4900 ps) in Address of top_tb.TOP.I
M1.i_SRAM.ErrorMessage
** MEM_Error: Unknown value occurred ( 4900 ps) in Address of top_tb.TOP.D
M1.i_SRAM.ErrorMessage

Done

DM[ 0] = cfb90b0a, pass
DM[ 1] = f56a8809, pass
```

```
*****
**                                     **
** Congratulations !!      **
**                                     **
** Simulation PASS!!    **
**                                     **
*****
```

```
$finish called from file "/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8./sim/to  
p_tb.sv", line 90.  
$finish at simulation time      434968100 ps  
          V C S   S i m u l a t i o n   R e p o r t  
Time: 434968100 ps  
CPU Time:    64.450 seconds;      Data structure size:   6.8Mb  
Mon Oct 30 21:31:54 2023  
CPU time: 17.917 seconds to compile + 5.816 seconds to elab + 1.429 seconds to link +  
64.502 seconds in simulation  
vlsicad9:/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8 %
```



Fig. 30. Make syn2 結果

4. Prog3

File Edit View Search Terminal Help

Warning-[NTCDNC] Negative Timing Check Did Not Converge
/usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/orig_lib/fsa0m_a/2009Q2v2.0/GENERIC_CORE/FrontEnd/ver
instance: QDLHN
Negative timing check delays did not converge, trying to solve by setting
minimum constraint to zero.

Notice: Ports coerced to inout, use -notice for details
Starting vcs inline pass...
453 modules and 7 UDPs read.
However, due to incremental compilation, no re-compilation is necessary.
make[1]: Entering directory `/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/build/csrc'
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.* share_vcsobj_*.*
if [-x ../*simv]; then chmod a-x ../*simv; fi
g++ -o ../*simv -rdynamic -Wl,-rpath='\$ORIGIN' simv.daidir -Wl,-rpath=../*simv.daidir -Wl,-rpath=../*simv.o _14231_archive_1.so _prev_archive_1.so objs/udps/qndjy.o objs/udps/G0JcM.o objs/udps/V0_1.o rmar_llvm_0.o -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcnew -lsimp...
o /usr/cad/synopsys/vcs/cur/linux64/lib/vcs_save_restore_new.o /usr/cad/synopsys/verdi/cur...
../*simv up to date
make[1]: Leaving directory `/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/build/csrc'
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detected on the m...
Please use '-no save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_INFO' to...
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64; Oct 30 21:33 :
Doing SDF annotation Done
** MEM_Error: Unknown value occurred (4900 ps) in Address of top_tb.TOP.IM1.i_S...
** MEM_Error: Unknown value occurred (4900 ps) in Address of top_tb.TOP.DM1.i_S...
Done
DM[0] = 00000003, pass

** |__||
** Congratulations !! ** / 0.0 |
** | / |
** Simulation PASS!! ** / \ / \ |
** | ^ ^ ^ |w|
***** \m_m_|_||

\$finish called from file "/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/.sim/to...
p_tb.sv", line 90.
\$finish at simulation time 497031500 ps
V C S S i m u l a t i o n R e p o r t
Time: 497031500 ps
CPU Time: 75.570 seconds; Data structure size: 6.8Mb
Mon Oct 30 21:35:00 2023
CPU time: 21.192 seconds to compile + 5.917 seconds to elab + 1.485 seconds to link +
75.631 seconds in simulation
vlsicad9:/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8 %

Fig. 31. Make syn3 結果

5. Prog4



The screenshot shows a terminal window with the following content:

```

Applications Places System
File Edit View Search Terminal Help

dir -Wl,-rpath=/usr/cad/synopsys/vcs/cur/linux64/lib -L/usr/cad/synopsys/vcs/cur/linux
64/lib -Wl,-rpath-link= ./ /usr/lib64/libnuma.so.1 objs/amcQw_d.o _18877_archive_
1.so _prev_archive_1.so objs/udps/qndjy.o objs/udps/G0JcM.o objs/udps/Wd2wc.o objs/udp
s/keuHx.o objs/udps/Sbaqa.o objs/udps/ySdCA.o objs/udps/xQ3mk.o SIM_l.o rmapats
mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lvirsim
-terrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/cad/synopsys
/vcs/cur/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archiv
e _vcs_pli_stub.o /usr/cad/synopsys/vcs/cur/linux64/lib/vcs_save_restore_new
.o /usr/cad/synopsys/verdi/cur/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ld
l
../simv up to date
make[1]: Leaving directory `/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/build/
csrc'
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detected on
the machine. To enable $save functionality, ASLR will be switched off and simv re-exe
cuted.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_IN
FO' to suppress this message.
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64; Oct 30 2
1:36 2023
Doing SDF annotation ..... Done
** MEM_Error: Unknown value occurred ( 4900 ps) in Address of top_tb.TOP.I
M1.i_SRAM.ErrorMessage
** MEM_Error: Unknown value occurred ( 4900 ps) in Address of top_tb.TOP.D
M1.i_SRAM.ErrorMessage

Done

DM[ 0] = 00375f00, pass
DM[ 1] = 00000000, pass
DM[ 2] = 0000129b, pass

*****
**          **          |__|||
** Congratulations !!    **          / 0.0 |
**          **          /_____\ |
** Simulation PASS!!    **          |^ ^ ^ \ |
**          **          |^ ^ ^ ^ |w|
*****\m___m_|_|
$finish called from file "/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8./.sim/to
p_tb.sv", line 90.
$finish at simulation time 423698100 ps
V C S   S i m u l a t i o n   R e p o r t
Time: 423698100 ps
CPU Time: 55.640 seconds; Data structure size: 6.8Mb
Mon Oct 30 21:38:08 2023
CPU time: 18.317 seconds to compile + 5.873 seconds to elab + 1.444 seconds to link +
55.698 seconds in simulation
vlsicad9:/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8 %

```

The terminal window has tabs at the bottom labeled [vsd2384], [vsd_hw2], VSD_HW2, and Terminal.

Fig. 31. Make syn4 結果

6. Prog5

Warning-[NTCDNC] Negative Timing Check Did Not Converge
 /usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/orig_lib/fsa0m_a/2009Q2v2.0/GENERIC_CORE/FrontEnd/ver
 instance: QDLHN
 Negative timing check delays did not converge, trying to solve by setting
 minimum constraint to zero.

Notice: Ports coerced to inout, use -notice for details
 Starting vcs inline pass...
 453 modules and 7 UDPs read.
 However, due to incremental compilation, no re-compilation is necessary.
 make[1]: Entering directory `/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/build/csrc'
 rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.* so share_vcsobj_*.* so
 if [-x ..simv]; then chmod a-x ..simv; fi
 g++ -o ..simv -rdynamic -Wl,-rpath='\$ORIGIN'/simv.daidir -Wl,-rpath=../simv.daidir -W
 d.o _22910 archive_1.so _prev_archive_1.so objs/udps/qndjy.o objs/udps/G0JcM.o objs/udps/W
 _0_1.o rmar_llvm_0.0.o -lvirsim -lrrorinf -lsnpsmalloc -lvfs -lvcnew -lsimpr
 .o /usr/cad/synopsys/vcs/cur/linux64/lib/vcs_save_restore_new.o /usr/cad/synopsys/verdi/cu
 ..simv up to date
 make[1]: Leaving directory `/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/build/csrc'
 Info: [VCS SAVE RESTORE INFO] ASLR (Address Space Layout Randomization) is detected on the m
 Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_INFO' to
 Chronologic VCS simulator copyright 1991-2023
 Contains Synopsys proprietary information.
 Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64; Oct 30 21:39 2
 Doing SDF annotation Done
 ** MEM_Error: Unknown value occurred (4900 ps) in Address of top_tb.TOP.IM1.i_S
 ** MEM_Error: Unknown value occurred (4900 ps) in Address of top_tb.TOP.DM1.i_S

Done

DM[0] = cfb90b0a, pass
 DM[1] = f56a8809, pass
 DM[2] = cfb90b0a, pass
 DM[3] = 0f95c456, pass

```
*****
**          **
** Congratulations !!   **      |__| / 0.0
**          **      / \_____\ |
** Simulation PASS!!   **      |^\^_\^ |w|
**          **      \m___m_|_
*****
```

\$finish called from file "/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/.sim/top_tb.s
 \$finish at simulation time 392583100 ps
 V C S S i m u l a t i o n R e p o r t
 Time: 392583100 ps
 CPU Time: 53.350 seconds; Data structure size: 6.8Mb
 Mon Oct 30 21:40:53 2023
 CPU time: 18.333 seconds to compile + 5.905 seconds to elaboration + 1.460 seconds to link + 53.396
 vlsicad9:/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8 %

Fig. 32. Make syn5 結果

V. Superlint 檢查及 Code 總行數

The screenshot shows the Cadence JasperGold Apps software interface. The top menu bar includes Applications, Places, System, File, Edit, View, Design, Reports, Application, Window, Help, and Superlint. The title bar indicates the file is superlint.tcl (session_0) - JasperGold Apps (.../build/jgproject) - Main (on vsicad9). The status bar shows the date and time: Tue Oct 31, 5:12 AM vsd2384.

Violation Messages View:

- Description (Order by Category)
 - Category: CODINGSTYLE (3)
 - Category: FILEFORMAT (4)
 - Category: SIM_SYNTH (1)
 - Category: STRUCTURAL (4)

Analysis Browser:

```

45 // ***** READ DATA CHANNEL *****
46     input logic [ AXI_IDS_BITS-1:0] RREADY;
47     output logic [ AXI_DATA_BITS-1:0] RDATA;
48     output logic [1:0]      RRESP;
49     output logic [1:0]      RLAST;
50     output logic [1:0]      RVALID;
51 );
52 );
53 );
54 logic [3:0]    current_state;
55 logic [3:0]    next_state;
56 logic          OE;
57 logic          CS;
58 logic [13:0]   A;
59 logic [31:0]   D;
60 logic [31:0]   DO;
61 logic [31:0]   WEB;
62 logic [3:0]    ARADDR_temp;
63 logic [31:0]   AWADDR_temp;
64 logic [31:0]   WDATA_temp;
65 logic [7:0]    relay_ARID;
66 logic [7:0]    relay_AWID;
67 logic [7:0]    relay_ARID;
68 logic [7:0]    relay_AWID;
69 );
70 // ***** Parameters *****
71 parameter [3:0] IDLE = 4'd0;
72 parameter [3:0] AR  = 4'd1;
73 parameter [3:0] R   = 4'd2;
74 parameter [3:0] AW  = 4'd3;

```

Terminal Window:

```

INFO (ISL014): Started extracting properties for ARY_IS_OOBI,CAS_NO_PRIO checks
INFO (ISL015): Extracted 1 properties of ARY_IS_OOBI,CAS_NO_PRIO
INFO (ISL015): Extracted 0 properties of BUS_IS_CONT
INFO (ISL015): Extracted 0 properties of BUS_IS_CONT
INFO (ISL018): Started extraction of structural checks
INFO (ISL016): Extracted 44 STRUCTURAL checks.
INFO (ISL016): Extracted 7 BASIC LINT checks.
52
[<embedded>] %
[<embedded>] % # Prove
[<embedded>] % set superlint prove_parallel_tasks on
[<embedded>] % set prove_no_traces true
[<embedded>] % # check superlint -prove -time_limit 10m -bg

```

Console Tab:

Console Warnings / Errors Proof Messages

Terminal vsd2384 vsd_hw2 [VSD_HW2] sim Terminal Terminal J superlint.tcl (session_0)

Engine ready Console input ready

Fig. 33. Superlint 檢查結果

在 Superlint 中檢查到的錯誤修正：

- (1) 將所有的 reset 改成 Asynchronous reset。
- (2) 將 Case 的語法都加上 default，已經將 state 寫滿的 case 則不用寫 default。

最後修正完有警告的行數總共為 12 條。

```

vlsicad9:/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/src % wc -l *
    8 Adder.sv
   211 ALU.sv
wc: AXI: Is a directory
    0 AXI
    33 Controller_D.sv
   127 Controller_E.sv
    77 Controller_jb_stall.sv
   92 Controller_M.sv
   79 Controller_W.sv
   583 CPU.sv
  706 CPU_wrapper.sv
   51 CSR.sv
   21 Decoder.sv
   16 Define.sv
   52 Imm_Ext.sv
    6 JB_Unit.sv
   27 LD_Filter.sv
   19 Mux3.sv
   12 Mux.sv
   24 Overlap.sv
   46 Reg_D.sv
  132 Reg_E.sv
   38 RegFile.sv
   86 Reg_M.sv
   25 Reg_PC.sv
   68 Reg_W.sv
   29 Shift_Addr.sv
  170 SRAM_rtl.sv
  506 SRAM_wrapper.sv
   460 top.sv
  3704 total
vlsicad9:/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/src % cd AXI
vlsicad9:/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/src/AXI % wc -l *
  283 AR_channel.sv
  120 AW_channel.sv
  393 AXI.sv
  143 B_channel.sv
  154 DefaultSlave.sv
  226 R_channel.sv
  152 W_channel.sv
  1471 total
vlsicad9:/home/user2/vsd23/vsd2384/vsd_hw2/N26114324_HW2_9.8/src/AXI % █

```

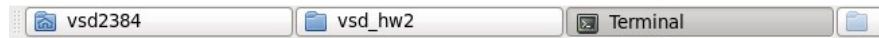


Fig. 34. RTL total lines

RTL code 總行數為 $3704 + 1471 = 5175$ 行

因此沒有出現 Warning 的 code 行數佔總行數百分比為: $\frac{12}{5175} \times 100\% = 99.768\%$

VI.Performance & Area

CYCLE : 9.8 ns

Parameter	Value	Unit
CPU_wrapper/CPU/Reg_M/M_rs2_out_reg[16]/D (QDFFRBN)	0.00	10.53 r
data arrival time	10.53	
clock clk (rise edge)	9.80	9.80
clock network delay (ideal)	1.00	10.80
clock uncertainty	-0.10	10.70
CPU_wrapper/CPU/Reg_M/M_rs2_out_reg[16]/CK (QDFFRBN)	0.00	10.70 r
library setup time	-0.17	10.53
data required time	10.53	

data required time	10.53	
data arrival time	-10.53	

slack (MET)	0.00	

Fig. 35. Synthesize Clock Cycle

MAX : 20376

AREA : 5928000.906064 um²

```
Combinational area:      474397.763585
Buf/Inv area:            66842.596125
Noncombinational area:   109108.642479
Macro/Black Box area:    5344494.500000
Net Interconnect area:  undefined (Wire load has zero net area)

Total cell area:         5928000.906064
Total area:               undefined
1
exit
```

Fig. 35. Report Area

VII. Major problems and resolutions

本次作業遇到的主要問題如下：

- (1) 在 prog0 中，其中有一個指令為特殊的 Load 情形，DM 會需要讀取 IM 位址的資料，此時 Master 0 透過另外 4 個特殊 state 來處理此情形，將 DM 所需要的資料從 IM 讀出，再交由 DM 進行後續的傳輸。
- (2) 在 Register file 由於沒有進行 stall 訊號的處理，因此在連續 Load 指令時 CPU 需要 stall，會把原本暫存的資料洗掉，需要額外進行處理。
- (3) 在 CPU Wrapper 的 Output combinational 電路控制資料傳輸，會出現 assertion 無法通過的問題，因此後續將控制部分全部交給 State control 的部分控制。
- (4) 在 prog1 中當 MAX cycle 不夠用可能會有運算做不完，無法通過模擬的問題，後續將 MAX cycle 調大可解決此問題。

VIII. Lessons learned from this homework

本次作業實作 AXI bus interface，光是理解 AXI 傳輸概念以及大量的訊號線在一開始就讓我非常困惑，花了非常多時間才理解 CPU 和 SRAM 在接上 AXI protocol 後是怎麼透過 bus interface 溝通，整體上有很多細節需要注意，例如：AXI 在進行資料傳輸的時候 CPU 需要 stall 住、Pipelined register 在加入 AXI 後需要多考量 AXI stall 的情形等等，而 CPU Wrapper 與 SRAM Wrapper 除了需要設計狀態以進行資料傳輸，也需要暫存來自 CPU 或 SRAM 的資料，才能夠保證資料傳輸的正確性，而透過 JasperGold VIP 工具的驗證也能夠理解到自己設計的 CPU Wrapper、AXI 與 SRAM Wrapper 有哪些部分是不夠完善的，在這次作業完成後對 AXI 的架構與 bus interface 的機制有了更全面的了解。