CE Amplifier:

An amplifier is used to increase the signal level from small ilp signal without disturbing the frequency and without distortion to make transistor work as an amplifier it should be biased such that emitter base junction is forward biased and collector base junction is reverse biased.

Initially the d.c. quiscent point is set and a.c. signal is superimposed on quiscent point, such that sinusoridally varying base current (Ib) is applied to the circuit.

Since the transistor is in active region, collector current varies B times to that of ilp base curre

the collector current varies above and below its a point values inphase with base current and VCE varies 80° out of phase with base voltage.

Practical CE amplifier:

where ver one cycle of ilp is completed, \ \{\frac{1}{2}}\end{a}, then one cycle for the completed Hence & Rs 0/p also gets the frequency of (6) magnitude increases: signal is constant while Bialing circuit!

nB!

circuit for ce amplifier, which sets proper operations

Ilp capacitor c,:

The ip capacitor blocks any d.c. Component present in the signal and passes only a.c. signal for amplification and hence biasing conditions are maintained constant.

Emitter bypass capacitor CE!

It is connected in parallel with Re to provide tow resistance path to amplified a.c. signal. It it is not connected, then amplified a.c. signal passing through Re will cause voltage drop which in turn decreased of voltage thereby reducing gain of amplifier.

olp coupling capacitor cz:

The phase reversal can be determined

the coupling capacitor c2 couples ofp of amplifier to next stage

phase reversal:

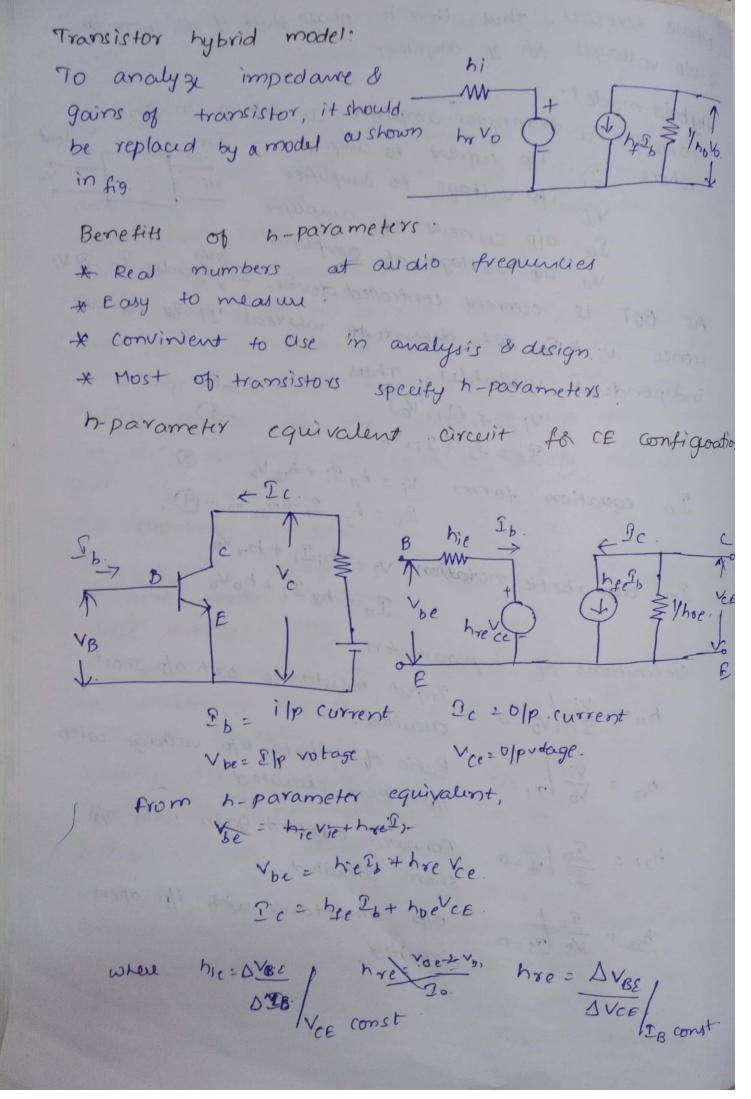
by considering the holf cycle & -ve & Re holf cycle seperately.

Re consider the cycle where terminal A Re consider the cycle where terminal A Re Re consider the with terminal B. Due to this ac & d. c. voltages will be added with each other and hence emitter base junction will be more forward biased and hence base current increases.

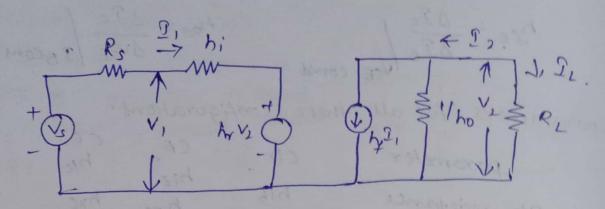
As I's increases, in turn increases Ic as Ic & Bib The Olp Vo is given by Vcc-IcRc. Hence as & increases Vo increases in we direction, executing

phase reversal. Thus there is phase shift of 180° btm its & old voltages for c£ amplifier. Hybrid model: consider a transistor amplifier of shown in fig. where I; ilp current to amp offer In its voltage to amplifier To old current of amplifier Vo Olp voltage of ampufier As ByT is current controlled device, Ii, decides 20.8 Vi Hence V; & To are dependent whereas I; & Vo are independent variables. Thus \_ (D) Vi = f, (Ii, Vo) To= f2 (I1, Vo) In equation form  $V_i = h_{11} \hat{\mathcal{I}}_i^* + h_{12} V_6 - \hat{\mathcal{J}}_i$ 20= h21 Ii+h22 Vo- 9. In alphabetic notation V; = h; I; + h, Vo Io = h = 2; + ho Vo Definitions of h-parameters: his Vi /vo 20. Input resistance with olp short circuited .... niz =  $\frac{V_i}{V_0}\Big|_{T_i} = 0$  Ratio of ilp to olp voltage with ilp open circuited Forward current gain with 0/p h21 = = 10/V6=0. short circuited olp admittance with ilp openh22 = To/2:=0.

circuited



he - DIC / hoe - SIC / IR const h-parameters for all three configurations: CB 21 resistance his Reverse voltage gain hrb Forward current gain. htb hoe. hoc. olp admittance Equivalent circuits for CB & CC are as follows hic amplifier circuit Analysis of transistor using hparameters. To form a transistor amplifier, it is necessary to connect an vs external load, signal source & proper biasing.



Let us analyze hybrid model to find current gain, ilp resistance, voltage gain & olp resistance.

current gain (A;):

for a transistor amplifier A; is the ratio of olp to ilp currents. It is given by

$$P_i = \frac{2L}{I_i} = -\frac{I_2}{I_1}$$

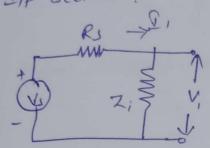
Here  $\Sigma_L$  &  $\Sigma_2$  are equal in magnitude but opp. in direction, hence  $\Sigma_L = -\Sigma_2$ .

From h=parameters we have  $2_{12} = h_{f} \mathcal{I}_{1} + h_{0} v_{2}$ .  $I_{2} = h_{f} \mathcal{I}_{1} + h_{0} (-\mathcal{I}_{2} R_{L})$ .  $I_{2} = h_{f} \mathcal{I}_{1} + h_{0} R_{L} \mathcal{I}_{2} = h_{f} \mathcal{I}_{1}$ 

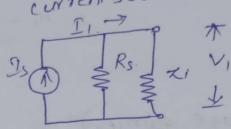
current gain AIs: It is the ratio while considering source resistance ATS = - 12 = -22 II RS

= Ai I;

Ilp section:



Ilp section as current source



According to current diverder equation

$$\begin{array}{ccc}
\Sigma_{1} & & & \Sigma_{3} & R_{5} \\
\hline
\Sigma_{1} & & & & \Sigma_{1} + R_{5} \\
\hline
\Sigma_{3} & & & & & \Sigma_{1} + R_{5} \\
\hline
\vdots & & & & & & & \\
\vdots & & & & & & & \\
\vdots & & & & & & & \\
\vdots & & & & & & & \\
\vdots & & & & & & & \\
\vdots & & & & & & & \\
\vdots & & & & & & & \\
\vdots & & & & & & & \\
\end{array}$$

Input Impedance (Zi):

At ilp terminals, the input resistance R; is

given by Riz VI

From ilp ob h-parameters hybrid circuit we have V, = h; I, + h, V2 Q: Z, = V1 = hi + hy V2

substituting V2 = - 12 R L= A; I, R,

e hitchy AII, RL)

voltage gain (Av)

$$A_{V} = \frac{V_{2}}{V_{i}} = \underbrace{A_{1} \mathcal{I}_{L} R_{L}}_{Y_{i}} = \underbrace{A_{1} R_{L}}_{Z_{i}}$$

Since 
$$\frac{\Omega_i}{V_i} = \frac{1}{Z_i}$$

Voltage gain Aus

It is gain including source.

$$A_{VS} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_S} = A_V \cdot \frac{V_1}{V_S}$$

$$\frac{V_1}{V_2} = \frac{Z_1}{R_2 + Z_1}$$

Substituting  $\frac{V_1}{V_5}$  in above eqn, we get

$$Avs = Av. \frac{Zi}{Rs + Zi} = \frac{AiRL}{Rs + Ri} \quad (:Av = \frac{AiRs}{Zi})$$

output admittance Yo:

It is the ratio of o/p current I, to o/prollage v. It is given by

From h-pprameters we have

$$\frac{\int_{2}^{2} \frac{1}{\sqrt{2}} dx}{\sqrt{2}} = \frac{h_{\xi} \mathcal{I}_{1}}{\sqrt{2}} + h_{0} = \frac{1}{\sqrt{2}} + h_{0}$$

considering Vs = 0 we can write.

$$\frac{2}{V_2} = -\frac{h_r}{R_s + h_i}$$

Power gain:

It is the ratio of average power delivered

er is given by
$$P_2 = \sqrt{2} \mathcal{I}_L = -\sqrt{2} \mathcal{I}_2$$

Relation between Avs & Ais.

we know that

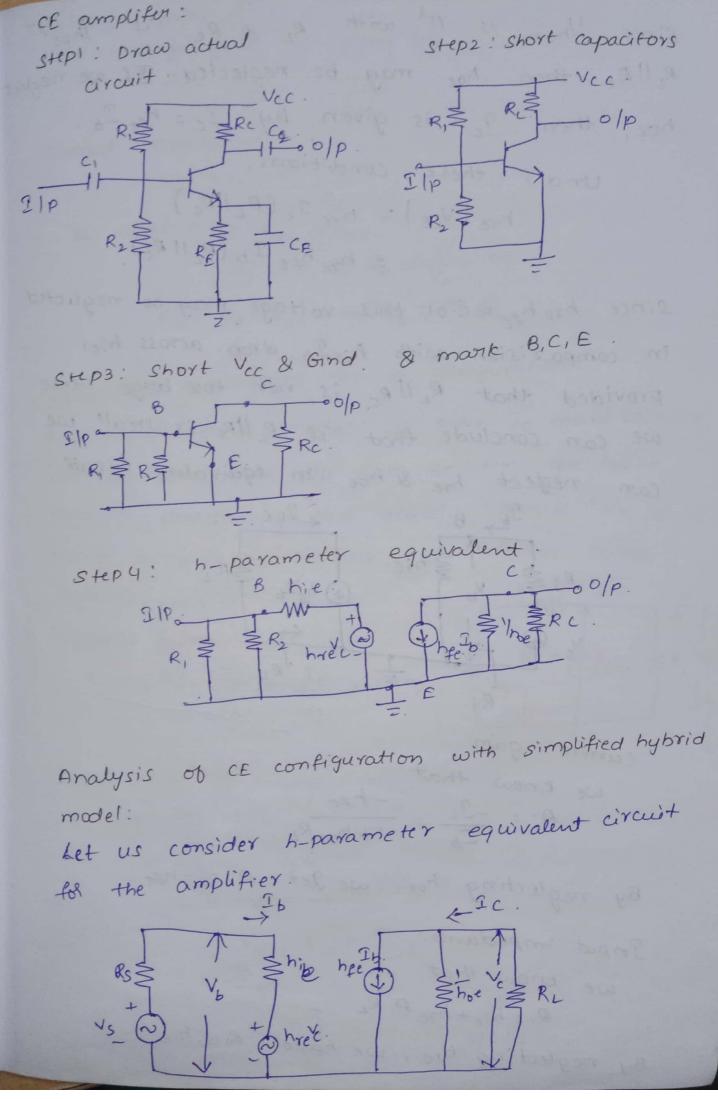
$$\frac{Avs}{Ais} = \frac{RL}{Rs}$$

Typical values of h-parameters:

parameter	CE	CC	CB.
hn2 hi	11002	110052	21.652.
h12=h7	2.2×104	1- 12-1	2.9×10-4
h21=h4	50	-51	-0.98
h22=h0	25 MALV	11 25 MAIN	0.49 MA/v.

Linear analysis of transistor circuit:

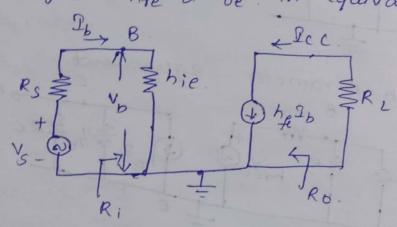
- 1. Draw the actual crt. diagram
- 2. Replace coupling capacitors and emitter by pass capacit by short circuit.
- 3 Replace de source by short circuit (connect Va to ground)
- 4. Mark points B, C, E & mark these points as start of equivalent circuit.
  - 5. Replace transistor by h-parameter model.



Since Those is 11 with RL & Rc if Those Rell Rc, then hoe may be neglected. If we neglected, then hoe, is given by Ic = hee Ib.

Under these conditions,

Since hre he 20.01, this voltage may be neglicted in comparision with hie Ib. drop. across hie, provided that Reller is not too large theree we can conclude that it Reller is small, we can neglect here & hoe in equivalent circuit.



current gain:

By neglecting hoe, we get Ais-hee

Input impedance?

we know that

Richiethre PiRe

By neglecting hre, we have Rishie

voltage gain:

The voltage gain is given by

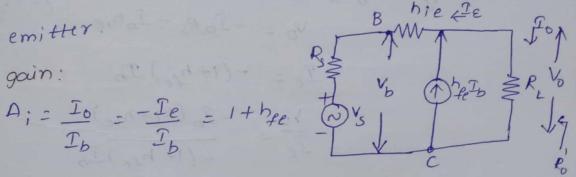
$$Av = AiRL = AiRL$$
 $Ri$ 

hip.

simplified calculations for cc configuration: for simplified cc model, we have to make collector common and take old from emitter. The help current direction is how exactly opposite that of CE model because the current heelb always points towards emitter.

Current gain:

$$A_{i} = \frac{I_{0}}{I_{b}} = -\frac{I_{e}}{I_{b}} = 1 + h_{fe}$$



Input resistance:

Applying KVL we have

$$V_b - I_b h_{ie} - I_0 R_2 = 0$$
 $V_b = I_b h_{re} + I_0 R_L$ 
 $V_b = h_{ie} + I_0 R_L$ 
 $V_b = h_{ie} + I_0 R_L$ 

$$\frac{T_0}{T_b} = \frac{T_e}{T_b} = 1 + h_{fe}$$

voltage gain(Av)

It is given as

Av = 
$$\frac{V_b}{V_b}$$
 =  $\frac{f_0 R_L}{I_b R_i}$  =  $\frac{A_i R_L}{R_i}$  (  $A_i = \frac{Q_0}{I_b}$ )

substituting values of Ai & Ri we get

output resistance Ro

It is the ratio of old voltage vo to old current

Ie with 16=0

Applying KVL

$$V_{S} - I_{B}R_{S} - I_{B}h_{ie} - V_{0} = 0$$

$$V_{0} = -I_{B}R_{S} - I_{B}h_{ie} \qquad ( V_{S} = 0)$$

$$I_{e} = -(1 + h_{fe}) I_{B}$$

$$I_{e} = -(1 + h_{fe}) I_{B}$$

$$\frac{V_b}{\mathcal{I}_e} = \frac{-\mathcal{I}_b(R_s + h_{ie})}{-(1 + h_{fe})\mathcal{I}_b}$$

$$R_0 = \frac{V_0}{Ie} = \frac{R_s + hie}{1 + h_f e}$$

The olp resistance  $R_0'$  of the stage taking the load into account is given as  $R_0' = R_0 I I R_L.$ 

Analysis of CB circuit using simplified Hybrid Here, the input is given to emitter model: Ic and ofp is taken from collector making base common. Current gain: It is defined v. (3) as ratio of olp to ilp currents - TTV  $A_i = \frac{I_0}{I_e} = -\frac{I_c}{T_0} = -\frac{h_e I_b}{T_0}$ - ( 1+ h+ ) Ib A; = hee From above eqn, the current gain of CB is always <1. It is the ratio of ilp voltage to ilp current Input Resistance: ( · · Ve = - hie Ib Ri = Ve = -hie Ib

Te = (1+he) Ib Te = - (1+ hg) In) = hie i+hee From above eqn. Ilp resistance is very low as compared to CE & CC configurations Voltage gain (Av): It is defined at ratio of olp to ilp voltager Av= Vo = IORL = AiRL Ve Ie Ri substituting Ai & Ri we get Av= hee RL = heRL 1+ heeOutput Resistance (Ro):

It is the vatio of old voltage to old current at  $V_s=0$ .

Ro =  $\frac{V_0}{\Sigma_c} / V_s=0$ .

when  $V_s=0$ , current through i/p loop i.e.  $\Sigma_b=0$ , hence  $\Sigma_c=0$ , and  $R_0=\infty$ .

The old resistance Ro, by taking load into account is given by

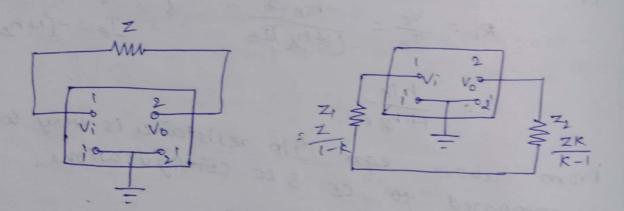
Ro = RollRL = wollRL = RL

Miller's theorem:

Miller's theorem is used to convert any

Circuit of one Configuration (fig 1) to other circuit

of another configuration (fig 2).



Miller's theorem states that an impedance 2 connected between two nodes can be replaced by two impedances Z1 & Z2 where Z1 is connected between model & gnd and Z2 is connected between node 2 & gnd.

The values of z, o z, an oxived from volvi denoted by k.

The values of impedances Z, & Z, are given by , Z1 = Z and Z2 = Zk Proof of Miller's theorem: TT T Z1= Vi where I = Vi- evo = Vissi- No I = Vissi- AVJ. Z1= Z = Z ('' Vo - Av = K) Z2 = V0
I
Where I = V0-Vi
Z

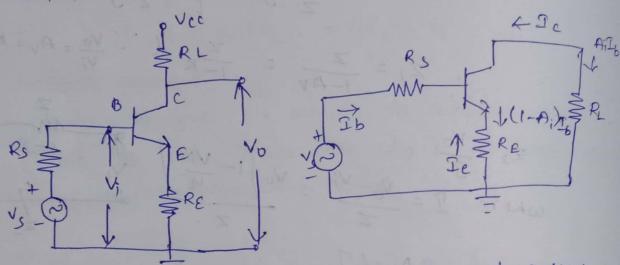
V0 [1-Vi]
V0
Z

T

V0
Z = Vo (AV-)  $Z_{2} = \frac{Z}{Y_{0}} + \frac{Z}{A_{V}-1} = \frac{kZ}{K-1} \left(\frac{1}{V_{1}} \frac{kZ}{A_{V}}\right)$ Dual of Miller's Theorem: If a nlw is considered such that z' is impedance btn. node 3 and ground N. According to dual of Miller's theorem z' can be split into Z1 & X2 such that zi is placed in mesh 1 . & zz in mesh z. and node s is grounded. As:  $-\frac{\Gamma_2}{I}$ ,  $\frac{Z(I-A)}{I}$ ,  $\frac{A_2^2-I}{I}$   $\frac{Z(I-A)}{I}$   $\frac{Z(I-$ 

CE amplifier with emitter resistance:

If the gain provided by single stage amplifier is not sufficient, then it is necessary to careau to next stage. In such case, if first stage is not stable, then instability will be fed and amplified by next stages which is not derived. Hence by next stages which is not derived. Hence emitter resistance has no ob better results on amplifier performance.



A.C. equivalent for c£ with unbypassed emitter resistance.

Approximate analysis:

PC: help

No.

No.

No.

PC: help

RE

PC: help

Fig. Shows approximate equivalent circuit current gain: It is given by  $Ai = \frac{-I_c}{I_h} = \frac{-h_{\neq e}I_b}{T_1} = -h_{\neq e}$ 

Input Resistance:

From the circuit, ilp resistance is given by

The ilp resistance due to factor (It he ) RE may be very much larger than hie thence emitter resistance greatly increases i/p resistance.

voltage gain:

It is given by

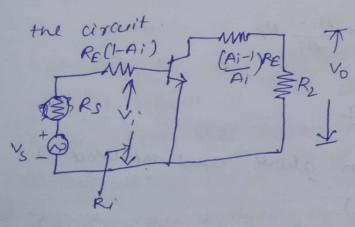
$$Av = \frac{AiRL}{Ri} = \frac{-h_{e}RL}{hie + (1+h_{e})Re}$$

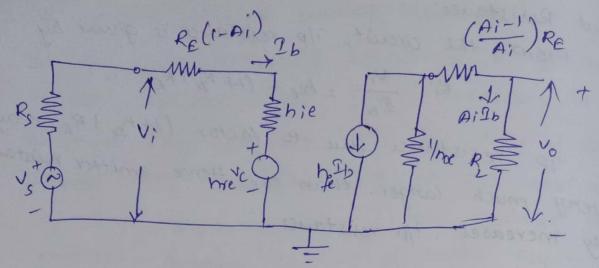
Output Resistance: It is resistance of an amplifier without considering source & load. (i.e. 1500 &R, = 00) -. Ro = Vo Vs=0

when Vs =0 the current through i/p loop 260 hence Ic & To both are zeroes, i. Ro = 00. 1. Ro= Ro 11R1 = 001/R1 = R1.

Exact analysis!

To make analysis of ce amplifier with RE, we have to use dual of Miller's theorem. Using this theorem emitter resistance can be split to obtain





current gain:

$$A_i = \frac{-h_{ee}}{1 + h_{ee}R_i} = \frac{-h_{ee}}{1 + h_{oe}(R_L + \frac{A_i - 1}{A_i}R_e)}$$

Input Resistance (Ri):

From above circuit Re(1-Ai) is in series

Voltage gain (AV):

where Ai & Ri from above egns are used

Output resistance (Ro):

Ro = 
$$\frac{V_o}{T_o} = \frac{1}{hoe} \frac{(1 + h_{fe})R_E + (R_s + h_{ie})(1 + h_{oe} R_E)}{R_E + R_s + h_{ie} - h_{re} + h_{oe}}$$

Note that if 
$$R_E$$
 >7 Rs thie, then

 $R_0 \approx \frac{1 + h_{ee}}{h_{oe}} + \frac{(R_S + h_{ie})(1 + h_{oe}R_E)}{h_{oe}R_E}$ 
 $= \frac{1}{h_{ob}} + \frac{(R_S + h_{ie})(1 + \frac{M}{h_{oe}R_E})}{h_{oe}R_E}$ 

Low frequency response of CE amplifier!

The frequency response of amplifier refers to frequency range at which amplifier operate with regligible effect from capacitors and device internal capacitance. This range of prequency can be called as mid range frequency + At freq. above & below this range, capacitor will effect gain of amplifier

\* At low freq. coupling & bypass capacitors lower gain

\* At high freq. stray capacitances effect gain.

voltage gain outside mid band is given by

Below mid band 
$$A = Amid$$

Above midband

 $A = Amid$ 
 $A = Amid$ 

(I+f14) T(1+(f42))

COUNTING MARCHORN BYPASS CAPACITORS:

Effect of coupling apacitors bypass capacitors:

The reactance of capacitor is  $X_{c} = \frac{1}{2\pi T_{c}}$ . At mid & high freq, the factor of makes  $X_{c}$  very small so that capacitor behaves as short circuit. But at low freq.

X<sub>c</sub> increases. This increase in  $X_{c}$  drops the signal voltage across capacitor & reduces circuit gain.

Low frequency analysis of BJT:

\* CE amplifier has 3 Rc Mw that effect its gain.

-y RC formed at ilp coupling capacitor, & ilp impeda, TRC formed at olp coupling capacitor à olp impeda of amplifier -> RC formed with emitter bypass & resistance at emitte Frin = R, 11 R, 11 hie. (Ilp Rc) f= 1 2TT Rin C, 2TT (R, 11 R, 11 h; 12) C, = 2TT (Rs + Rin) C, il olp RC. Cz FRC FRL VO fc = 2TT (Rc + Ri) (2. iii, By pass capacitor  $R = \frac{V_e}{Te} + \frac{hie}{B}$ = Vb + bie = IBRH + hie z) R= R+n+ hie B. f: 2TT RC: 2TT (R. 11 Re)C. & R+n= R, 11 Rx upon the calculation of 3 frequencies, whichever s nighest will be considered as lower cutoff frequency.

Let us calculate  $R_1$ ,  $A_1$ ,  $A_V$ ,  $R_1$ ,  $A_V$ s &  $A_1$ s if construct parameters are  $R_S = 1$ K,  $R_{C_1} = 15$ K,  $R_{E1} = 100 \Omega$ ,  $R_{C_2} = 4$ K,  $R_{E2} = 380 \Omega$  with  $R_1 = 200$ K &  $R_2 = 20$ K for first stage and  $R_1 = 4$ TK and  $R_2 = 4$ TK for second stage. Assume that  $h_1 = 1.2$ K  $\Omega$ ,  $h_2 = 50$   $h_2 = 2.5$ X $10^{-4}$  and  $h_0 = 2.5$ X $10^{-6}$ A1V.

Analysis of second stage (CE amplifier).

As hoe R<sub>L</sub> = hoe R<sub>C2</sub> = 25 × 10<sup>6</sup> × 4 × 10<sup>3</sup> = 0.1 we use approximate analysis.

- a) current gain  $(A_{12})$ .  $A_{12} = -h_{e} = -50$
- b) Input Resistance (R12)  $R_{12} = hie = 1.2 k \Omega.$
- c) voltage gain (Av2).

$$A_{v_2} = A_{i_2}R_L = \frac{-50 \times 4 \times 10^3}{1.2 \times 10^3} = -166.67$$

Analysis of first stage

 $R_{L}^{1} = R_{C1} ||R_{1}||R_{2}||R_{12}$ = 15 k || 47 k || 4.7 k || 1.2 k = 881.8 \( \infty\)

-' hoe  $R'_{L} = \frac{1}{40} \times 10^{-3} \times 881.8$ = 0.022

As hoe R<sub>L</sub> < 0.1 we can use approximate analysis.

a) current gain = - he = -50.

b) Input resistance (Ri)

Rii = hie = 1.2 k 2.

c) Voltage gain  $(A_{VI})$ :  $A_{VI} = \frac{-50 \times 881 \cdot 8}{R_{II}} = -36.74$ 

overall gain (Av)

 $A_{V} = A_{V_{1}} \cdot A_{V_{2}} = (-166.67) (-36.74)$  = 6123.45

Overall voltage gain (Avs)

Avs = Av. Ril

Rit Rs.

where Ri, = RillR2 || Ri = 200 k || 20 k || 1.2 k.

where  $A_{VS} = \frac{6123.45 \times 1.13 \times 10^3}{1.13 \times 10^3 + 1 \times 10^3} = 3248.6$ 

olp Resistance (Ro):  $R_{01} = R_{01} || R_{01} = \infty || 15 k = 15 k$ .  $R_{02} = R_{02} || R_{02} = \infty || 4 k = 4 k$ .

Different coupling schemes used in Amplifiers.

In multistage amplifiers, the old one stage coupling is fed to next stage by using different elements.

They are 1. Rc coupling 2. Transformer coupling

3. Direct coupling